Bottom-Gate Complementary Inverters on Plastic with Gravure-Printed Dielectric and Semiconductors

Nikolay L. Vaklev, Ying Yang, Beinn V. O Muir, Joachim H. G. Steinke and Alasdair J. Campbell

Abstract—**Organic complementary circuitry combines all the advantages of plastic electronics, such as flexibility, thinness and solution-processability with low power consumption. Here we report organic complimentary inverters fabricated in a carrier-free batch process on plastic foil with dielectric and semiconductor layers patterned using the high-volume gravure contact printing technique. The transistor components have bottom-gate, bottom-contact configuration with aluminium gates and gold contacts, allowing full use of photolithographic processing whilst protecting the semiconductors by depositing them last. Cross-linkable polymer dielectric, p-type small molecule and the n-type polymer semiconductors are printed from inks based on non-chlorinated solvents. Printing instability is observed for capillary numbers approaching 1. The 430 nm thick dielectric affords relatively-low operational voltage and it is the thinnest printed organic dielectric reported in the literature for organic inverters to date. Both p- and n-type transistors have a mobility of 0.01–0.04 $cm^2V^{-1}s^{-1}$. The device parameters for the n-type transistors show less variation than the p-type transistors, which can be related to the more isotropic charge transport in polymer films compared to the small-molecule polycrystalline films. The resultant inverters have an average gain of 4.5±1.5 and a maximum gain of 8 at V_{DD} = −20 V. The combination of conventional photolithographic processing and gravure contact printing can therefore be used to fabricate bottom-gate organic complementary circuitry on plastic.**

Index Terms—**printing gravure, complementary inverters, organic transistors**

I. Introduction

Organic electronic circuits on plastic substrates have the potential advantages of flexibility and thinness. High-volume low-cost printing methods such as gravure printing can be used to fabricate uniform layers over large areas. There are two types of inverters — unipolar and complementary — based on the type of semiconductors they use. Unipolar inverters[1] require only one semiconductor whereas complementary logic need both p- and n-type semiconductors. Complementary inverters consume power only during switching between states. They also have much higher noise margins (NMs), which is advantageous for designing digital circuits, and improves device yield.

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RFID tags[2] in packaging, flexible displays[3], wearable electronics[4], [5], optical[6] and biomedical[7], [8] sensors have been demonstrated with transistors based on organic materials. A microprocessor based on unipolar circuits was reported on plastic foil fabricated using standard photolithography and thermally evaporated p-type semiconductor.[9] Schmidt *et al.*[10] also showed fully-printed unipolar p-type inverters and ring-oscillators reaching 1.0 kHz. On the other hand, there has been a delay in the development of complementary organic circuits due to the lack of commercially-available n-type organic semiconductors (OSCs) other than fullerenes and their derivatives. In 2009, Yan *et al.*[11] demonstrated an n-type polymer based on a naphthalene diimide monomer and it is used in this work.

Organic electronics opens the possibility to partially or fully print devices and circuits. Printing techniques are especially advantages in the fabrication of complementary inverters, because they allow direct patterning of the semiconductors. In the case of organic inverters two organic semiconductors have to be deposited onto the same substrate. This requirement presents a particular limitation for blanket-coating techniques such as spin-casting, zone-casting and blade-coating. It is possible to establish a process flow based on additive and subtractive steps to pattern semiconductors, but increasing the number of processing steps is inefficient and leads to low yields. Printing techniques such as ink-jet, gravure, and offset-lithography allow one or more inks to be selectively printed onto the same substrate. Kempa et al.[12] reported fully-printed complementary inverters and ring oscillators with gain around 5 and 1.5 µm thick dielectric printed using flexography and semiconductors printed using gravure. Jacob et al. [13] provided another example of fully-printed complementary inverters with screen-printed dielectric and printed semiconductors with a gain of 15–20.

We reported recently high-performance flexible bottom-gate bottom-contact (BGBC) organic field-effect transistors.[14] The dielectric was gravure-coated over the whole substrate and defined by photopatterning. Here we use gravure printing to directly structure the dielectric and both semiconductors to build complementary inverters on plastic foil, which eliminates the need for additional patterning. All inks are based on industry-compatible non-chlorinated solvents and give appropriately defined features. Unlike previous complementary circuits[11-13], we use a bottom-gate configuration. This configuration is preferred by industry because it allows full use of photolithographic processing whilst protecting the semiconductors from UV light and

aggressive chemicals by depositing them last. Devices are fabricated in a carrier-free sheet-to-sheet batch process flow. The resultant inverters achieve average gain of 5 at low operating voltage of −20 V. This work demonstrates also one of the thinnest printed dielectrics (430 nm) for complementary inverters and BGBC transistors (Fig. 1) with short channel lengths of 5–25 μm (Table A.1), both of which lower drive voltages and improve circuit speed. General device fabrication is described elsewhere[14] and brief summary of the fabrication process is provided in Supplemental Materials.
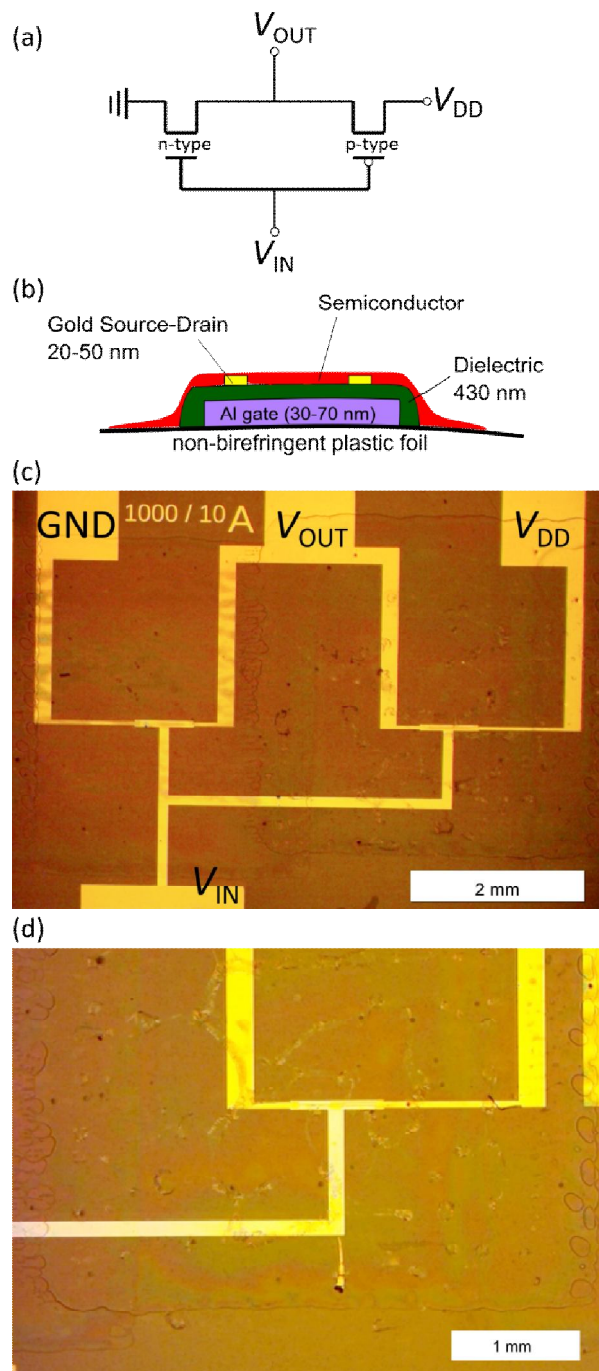

Fig. 1. (a) Diagram of a complementary inverter; the drive voltage is connected to the p-type. (b) Diagram of transistor cross-section. (c) Optical micrograph with annotations of a complementary inverter on plastic substrate. (d) Optical micrograph of p-type transistor.

Achieving printed uniform and functional films is one of the main questions for printed electronics. In this study, print speed and screen density were varied, and, viscosity and surface tension investigated. Print screen density is defined as the number of ink cell lines per unit length on the printing plate. The printing parameters were aggregated in capillary (Ca) and Reynolds (Re) numbers and compared (Fig. A.1). The Ca number is associated with the liquid meniscus formed between substrate and cliché around the nip during ink transfer[15], whereas the Re number represent the balance between inertial and viscous forces.

II. MATERIALS AND METHODS

A proprietary non-birefringent plastic foil from Asulab (Switzerland) with pre-deposited transparent conducting oxide (TCO) was used. The glass-transition temperature of the material was 215 °C and the maximum processing temperature was 180 °C. The substrates were cleaned by sonication and the TCO was etched away. The gate electrode was made by thermal evaporation of aluminium (30–70 nm) followed by photolithographic patterning and etching. The dielectric was gravure printed on top, annealed and cross-linked with UV radiation. The dielectric formulation is a proprietary material from BASF which contains an acrylate cross-linker (42 wt%), a high molecular weight poly(methyl methacrylate) (4.2 wt%) as a viscosity modifier and two high-boiling-point solvents. The radical photoinitiator Irgacure 369 from BASF was added to the dielectric formulation at 10 mg mL^{-1} prior to printing. The films were dried at 115 °C for 5 min in ambient air and cross-linked under nitrogen in Novascan PSDP-UV for 10 min. Contacts and interconnects were fabricated on top by thermal evaporation of gold (30–90 nm) and patterning via photolithography and bilayer lift-off. The printed semiconductors were 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene, High Force Research, UK) and P(NDI2OD-T2) n-type (ActiveInk N2200, Polyera Corporation, USA). The n-type OSC was printed first and annealed for 30 s at 115 °C, followed by printing the p-type. All solvents were purchased from Aldrich. Printing was done with a Schlaefli Maschinen Labratester 1 at 160±40 N cm^{-2} nip pressure. This process flow uses carrier-free batch processing, which is compatible with many industrial processes and photolithography of the metal electrodes is a standard industrial technique. Viscosity and surface tension for the different inks were measured with PAC VISCOlab 4000 and Krüss DSA 100, respectively. Printing specifications and ink parameters are reported in Table A.2.

III. RESULTS AND DISCUSSION

The dielectric was printed at three different print speeds in the range 12–44 m/min while keeping the other parameters constant. Print screen density was fixed at 40 lines cm^{-1} to achieve the necessary film thickness. Continuous film coverage was obtained only at 12 m/min (Fig. 2), which was the lowest speed possible with the printer. At higher print speeds, there was a regular pattern of holes in the dielectric films, which correlated with the pits of the print screen. The organic dielectric layer used in the inverters (print speed 12 m min^{-1}) was 430±17 nm thick as measured by contact profilometry and the relative permittivity was 3.2 based on

impedance spectroscopy[14]. The root-mean-square surface roughness was 14 nm as measured by optical interferometry over an area of 1×1 mm^2 (Fig. A.2). The off-currents for all transistors were 1–10 pA demonstrating the quality of the printed dielectric and the on/off ratio was in the range 10^4–10^6 (Fig. A.3 and Fig. A.4). The Ca and Re numbers were found to be in the range 0.2–1 and 0.04–0.2, respectively, with the most uniform printed films used in the inverters having the lowest values (Fig. A.1). For comparison, Li *et al.* reported recently gravure-printing 300 nm thick organic semiconductor in diodes.[16] The dielectric reported here is exposed to higher electric field in the transistors.

TIPS-pentacene was printed from 10 mg mL^{-1} (ca. 1 wt%) solution in anisole:decane (99.5:0.5 v/v%) solvent mixture. Print screen density was fixed at 250 lines cm^{-1} to achieve thin TIPS-pentacene films with a low transistor off-current. This ink gave continuous coverage whereas the equivalent ink based on pure anisole produced incomplete coverage at 12 m min^{-1} and separate TIPS-pentacene crystals at 44 m min^{-1} (Fig. 3). The surface tension of decane and anisole is 23 and 35 mN m^{-1} at room temperature, respectively.[17] Decane accumulates at the liquid-air interface and lowers the surface tension of the solvent mixture, which is driven by a decrease in the Gibbs free energy of the system.[18] Experimentally, adding decane lowered the surface tension from 30 ± 2 to 26 ± 2 mN m^{-1} (Table A.2) in pendant-drop measurements. The estimated Ca numbers during printing were in the range of 0.01. The TIPS-pentacene ink with decane gave continuous films with crystalline domains. The viscosity was ca. 1 cP for these inks, which is approximately the intrinsic viscosity of the pure organic solvents. Therefore, their properties were determined by surface tension and the way it affected meniscus formation and stability around the nip. This result confirms again that printing at low capillary numbers stabilises ink transfer. The Reynolds number appears to have less of an effect in the investigated range of 0.01–10.
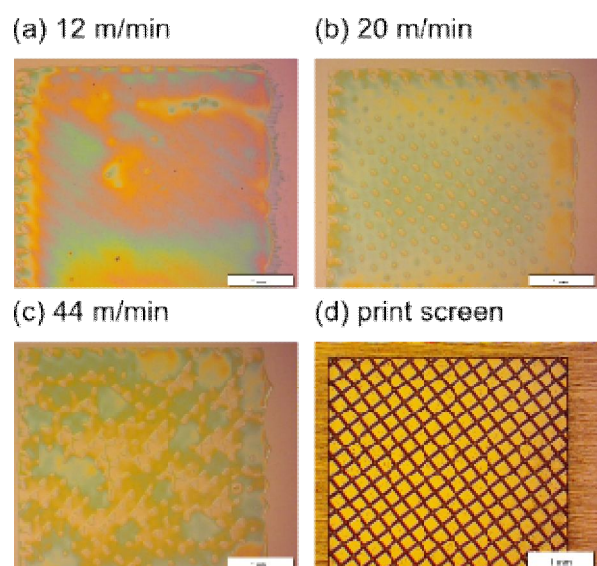

Fig. 2. Optical micrographs of (a, b, c) the dielectric ink printed at three different print speeds with (d) 40 line cm^{-1} print screen. Scale bar 1 mm.
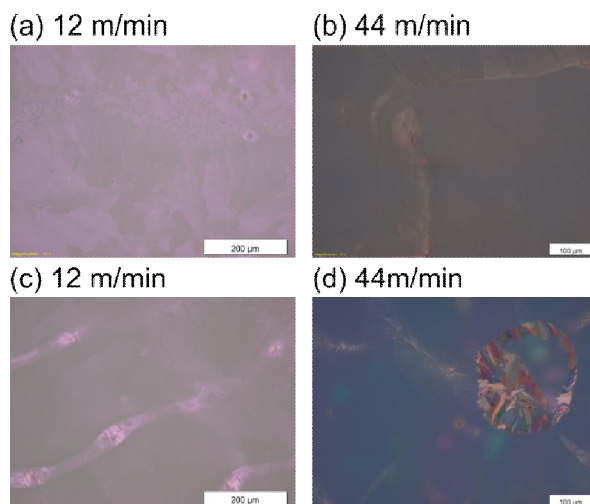

Fig. 3. Optical micrographs of the TIPS-pentacene printed from (a, b) anisole:decane (99.5:0.5 v/v%) mixture and (c, d) pure anisole at 12 and 44 m min^{-1} print speed on the dielectric. Decane improved ink transfer and afforded continuous coverage at all speeds.

The n-type polymer OSC P(NDI2OD-T2) was deposited from a solvent mixture of tetrahydronaphthalene:indane (50:50 v/v%) at a concentration of 20 mg mL^{-1} (ca. 2 wt%). A higher printing speed of 40 m/min, similar to that used with the successful TIPS-pentacene inks, was used. The print screen density at constant speed was varied. The different ink loading per area was used as a characteristic length to calculate the Re number for the different print screens. Hence, changing the screens for the n-type ink at constant speed resulted in the same Ca number but different Re values. At Ca and Re of ca. 1 and 0.1, respectively, the prints exhibited patterns of "cascade" instability[19], [20] (Fig. 4), which is associated with the meniscus formation and stability around the nip region; the ink forms a wetting meniscus between cliché and substrates during printing.[21], [22] The n-type and the dielectric inks have similar Re numbers but differ in their loading with the dielectric having ca. 20-times higher solid content by mass and the 5-times lower capillary number. These results show that when Ca approaches 1 the ink transfer becomes unstable, resulting in non-uniform films and cascade patterns. However, surface roughness and non-uniformity of the semiconducting films are not an issue for BGBC transistors as long as the coverage is a few nanometres thick to allow a complete accumulation layer to form between source and drain; this property is a strong advantage of the BGBC architecture. Films printed using a screen density of 250 lines cm^{-1} were used in devices, combining complete coverage with a low transistor off current.
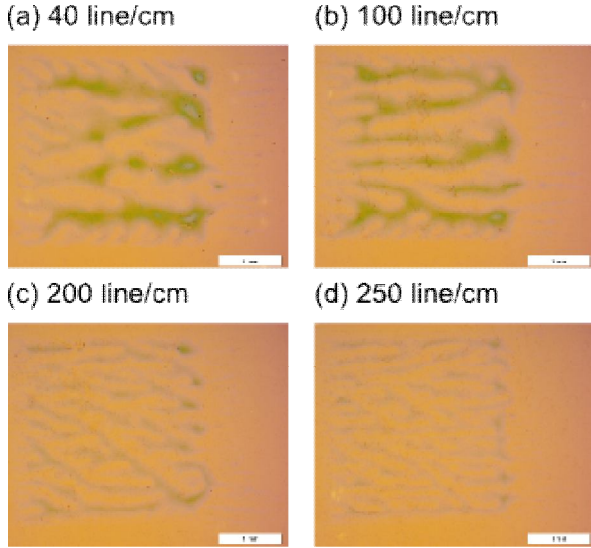
Fig. 4. Optical micrographs of the n-type ink printed with four different print screens on PC-TCO. The micrographs show inhomogeneous ink pattern known as "cascade instability". The print direction is from left to right. Scale bar 1 mm.

Fig. 5. Transfer curves of OFETs with (a) p- and (b) n-type semiconductors. The V_{ds} for linear and saturation regimes were ±5 and ±20 V, respectively. Voltage polarity depended on the semiconductor type. Optical micrographs of the printed (c) p- and (d) n-type in the transistor channel obtained with cross-polariser. Scale bar 50 µm.

OFETs with both semiconductors had negligible hysteresis in the transfer curves (Fig. 5). Charge-carrier mobility and threshold voltage in the saturation regime were extracted from the linear fit to V_{gs} vs. $(I_{ds})^{1/2}$ (Table A.1).[14] The hole and electron mobilities were on average 0.036 and 0.013 $cm^2V^{-1}s^{-1}$, respectively. The spread though for TIPS-pentacene was an order of magnitude higher than for the n-type. This is most likely a result of the crystalline nature of TIPS-pentacene (Fig. 5c), which is known to have anisotropic transport.[23], [24] The n-type is a semi-crystalline polymer[25] and the average transport properties should be isotropic. These results underline the necessity for precise control of the crystallinity for small molecules. Nevertheless, the upper limit for the p-type mobility was ca. 0.1 $cm^2V^{-1}s^{-1}$ which is comparable to the best examples in the literature for BGBC devices with TIPS-pentacene.[26] The P(NDI2OD-T2) n-type showed ambipolar behaviour clearly seen in the eleveated off-currents in the saturation regime (Fig. 5b), which has been observed by other authors.[27], [28] The inverters were stored and measured in a nitrogen glovebox (0.1 ppm oxygen and water) otherwise the n-type had mobility $<10^{-4}$ $cm^2V^{-1}s^{-1}$ or no transistor performance altogether. A typical inverter curve is shown on Fig. 6. The averaged maximum gain was 4.5±1.5 at V_{DD} = −20 V based on 12 inverters (60 % yield). The highest maximum gain achieved was 8 (Fig. A.5a). However, there was scatter in the NM values (Fig. A.5b). This can be related to the spread in mobility and threshold voltage values for the p-type combined with the ambipolar transport of the n-type.
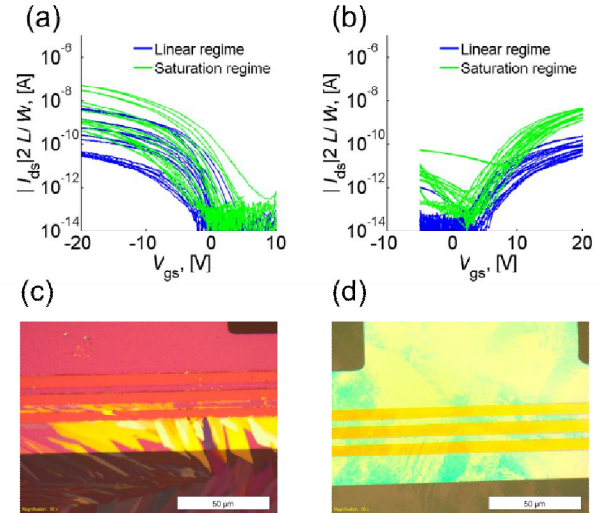
IV. Conclusions

In conclusion, we fabricated bottom-gate inverters on plastic with gravure-printed dielectric and semiconductors. Printing instability increases for capillary numbers approaching 1; the Reynolds numbers had no appreciable effect on the printing process within the investigated range. The dielectric layer is 430 nm thick and exhibited ultra-low leakage levels; it is the thinnest printed dielectric reported in the literature to date in inverters. The p-type small-molecule semiconductor OFETs had a large parameter spread and the n-type exhibited ambipolar behavior, which resulted in a large spread of noise margin values. However, an average gain of 4.5 at relatively low drive voltage of 20V was achieved, with a peak gain value of 8. These results show the potential of gravure printing and this bottom-gate batch process flow for the fabrication of flexible complementary inverters. Gravure was used to print inks with variable solid content and viscosity demonstrating its versatile nature.
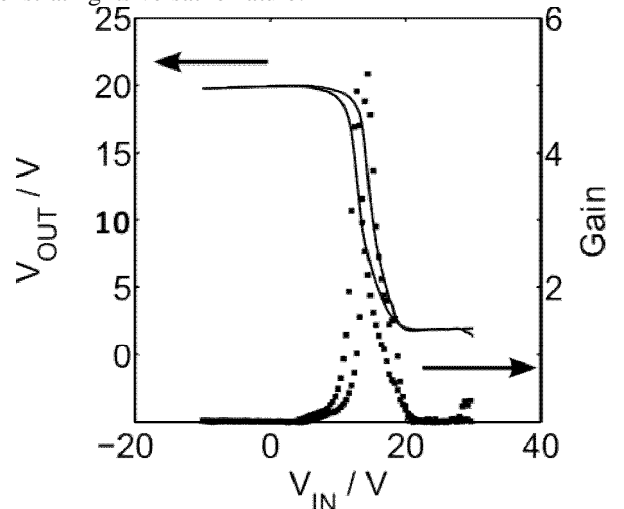

Fig. 6. Inverter characteristic of an average device with low and high noise margins of 10 and −5 V at V_{DD} = −20 V.
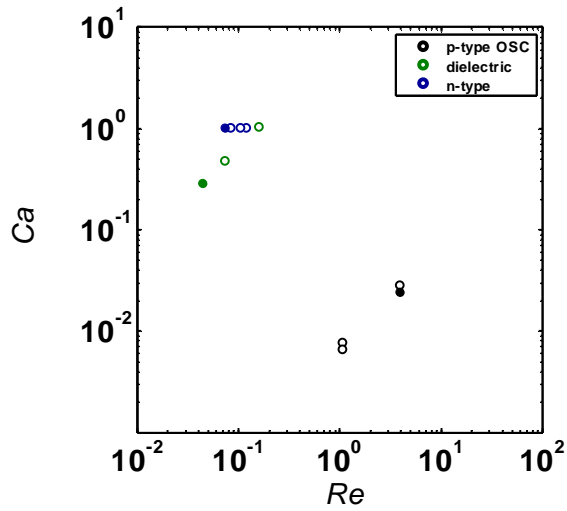
Appendix A. Supplementary information

Fig. A.1. Capillary (*Ca*) vs. Reynolds (*Re*) numbers for the prints shown on Fig. 2, Fig. 3 and Fig. 4. The filled circles correspond to the different inks printed in the inverters. A summary of all printing parameters for the final inks is given in Table A.2.
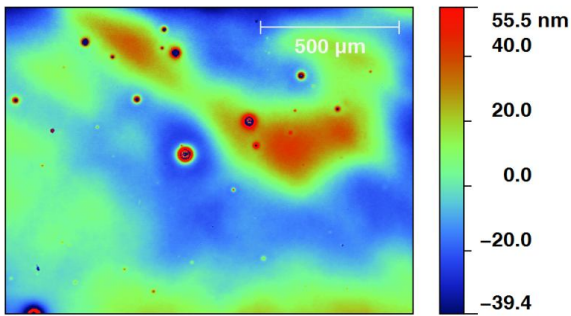

Fig. A.2. Optical-interferometry micrograph of the dielectric ink printed at 12 m min^{-1}. The rounds dots are from particle contamination on the foil. The rms surface roughness was 14 nm, excluding artifacts due to particle contamination.
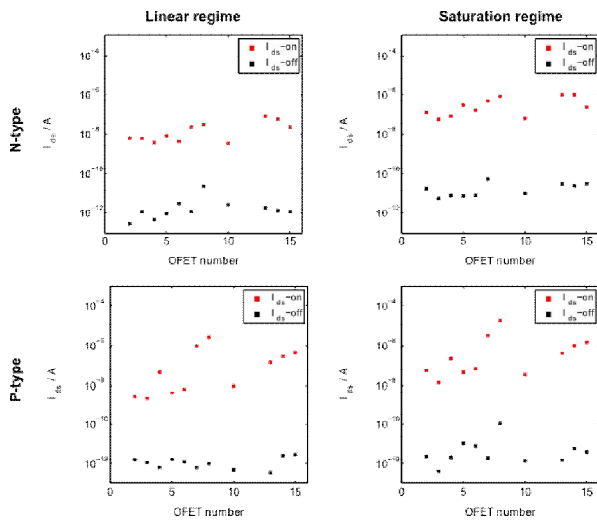

Fig. A.3. Source–drain current in on- and off-state for linear and saturation regimes for OFETs with gravure printed p- and n-type semiconductors and dielectric. The current is not adjusted for the *W/L* ratio of the transistors.
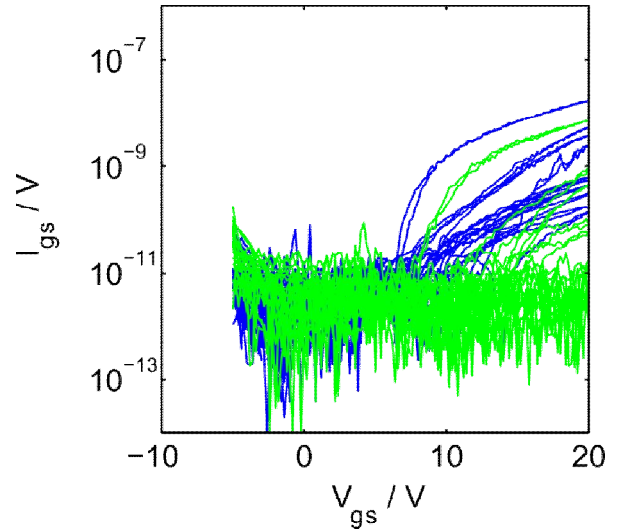

Fig. A.4. Gate–source current for linear and saturation regime for n-type OFETs.
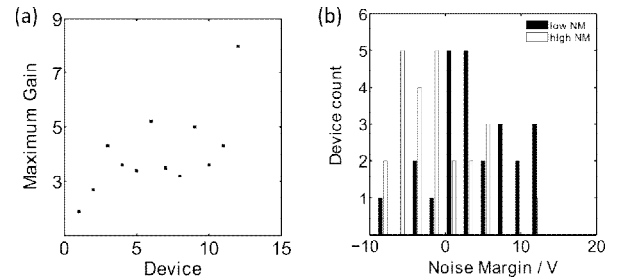

Fig. A.5. (a) Maximum gain and (b) their noise margins for 12 inverters. The noise margins are calculated as described in Ref. [29] at −0.5 gain.

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Table A.1. Comparison between the present work and a selection of literature sources. The inverters are compared in terms of transistor architecture, logic type, hole (μ_h) and electron (μ_e) mobility, drive voltage (V_{DD}), gain, dielectric thickness (d) for the p- and n-type semiconductors where appropriate.

Ref.	OFET	Logic type	μ_h /cm^{2}V^{-1}s^{-1}	μ_e/ cm^{2}V^{-1}s^{-1}	V_{DD} /V	Gain	d /μm	Dielectric deposition	OSC deposition
here	BGBC	complementary	0.001–0.1[b]	0.01–0.06[b]	−20	2–8	0.43	gravure	gravure
[2]	BGBC[a]	unipolar	0.15	NA	10	–	–	spin-casting	spin-casting
[10]	TGBC	unipolar	0.2	NA	>48	–	2	gravure	screen print
[11]	TGBC	complementary	0.02–0.1	>0.1	20	50	1	gravure	gravure
[12]	TGBC	complementary	0.004	0.003	−60	5.3	1.5	flexography	gravure
[13]	TGBC	complementary	1.5	0.55	40	15–20	0.75	screen print	unknown

[a] The devices had a top gate as well, which allows control of the threshold voltage.
[b] Measured in saturation regime.
BGBC = bottom-gate bottom-contact; BCTG = bottom-contact top-gate

Table A.2. Summary of ink and printing parameters: solvent composition, surface tension (γ), viscosity (η), print speed, print screen density, ink loading of the print screen and, Re and Ca numbers.

V. Ink	Solvent 1	Solvent 2	γ /mN m^{-1}	η[d] /cP	Print speed[a] /m min^{-1}	Print Screen /line cm^{-1}	Ink loading[c] /nL mm^{-2}	Re	Ca
n-type (20 mg mL^{-1})	Indane (50 v/v%)	THN (50 v/v%)	32±2	48	40	250	5.3	0.073	1.0
TIPS-pentacene (10 mg mL^{-1})	Anisole	–	30±2[b]	~1[b]	44	250	5.3	3.9	0.024
TIPS-pentacene (10 mg mL^{-1})	Anisole (99.5 v/v%)	Decane (0.5 v/v%)	26±2[b]	~1[b]	44	250	5.3	3.9	0.028
Dielectric ink	–	–	28	40	12	40	8.7	0.043	0.29

[a] preferred print speed
[b] pure solvent mixtures
[c] Ink loading per print screen was used as a characteristic length to calculate the Re numbers.
[d] measured at 21–23 °C.
Ink density was assumed 1 g mL^{-1} for all inks, which is a typical value for the used organic solvents.