An Improved Fast Transient Response Low Drop-out Voltage Regulator

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***Abstract*—A design of fast transient response low drop out voltage regulator (LDO) is presented. The requirement of fast transient response is dependent on the loading condition. In high speed applications, chips runs at MHz frequency, so the load current changes from zero to full value and so forth in a very small time. In such cases circuit with fast transient response is a definite requirement. This LDO is implemented in 0.18um generic CMOS technology; it generates fixed 1.6V from a supply of 3.6V which on discharging goes down to 1.9V. The buffer stage used is a wide band OTA capable of providing rail-to-rail swing and full current for charging and discharging the large driver transistor capacitance, that enables fast slewing. Simulation result shows that the proposed circuit provides full load transient response of less than 44ns settling time and less than 15mV undershoot.**

I. INTRODUCTION

The requirement for low drop-out voltage regulator is continuously being driven by portable electronics market and is used extensively in products like cameras, cellular phones, DSL/Cable modems, mp3/CD players, etc [1-7]. Since electronic equipments are very susceptible to load transient so stable supply voltage is always required that establishes a stable point used for generating predictable results. This reference source should not fluctuate significantly under various operating conditions such as changing power supply voltages, temperature variations and transient loading events. The purpose of this paper is to present a design of a Fast Transient Response low dropout voltage regulator. The technology used is 180nm generic CMOS technology.

II. COMPLETE WORKING OF A LDO

A LDO is a type of linear voltage regulator that uses a metal oxide semiconductor field effect transistor (MOSFET) to subtract excess voltage from the applied input voltage, producing a regulated output voltage. Low dropout refers to the smallest difference between the input and output voltages that allow the LDO IC to still regulate the output voltage [1-7]. That is, the LDO device continues to regulate the output voltage until its input and output approach each other within dropout voltage. Ideally, the dropout voltage should be made as low as possible to minimize power dissipation and maximize efficiency. And because of this LDO voltage, the LDO extends battery life by permitting the battery to be discharged all the way down to a few hundred milli-volts of the desired output voltage. For MOS device to operate in strong inversion, overdrive needs to be at least 100mV, but such smaller overdrive result in larger device size to generate same current level. And in voltage regulator where large load current is to be provided, even a 100mV will result in a lot of saving in the driver MOS size.

The LDO's main components are a power semiconductor (pass transistor), error amplifier, and voltage reference (see Figure 1). One input to the error amplifier, set by resistors, monitors a percentage of the output. The other input is a stable voltage reference (Vref). If the output voltage increases relative to Vref, the error amplifier (connected in negative feedback configuration) controls the pass-transistor's output to maintain a constant output voltage (Vout).

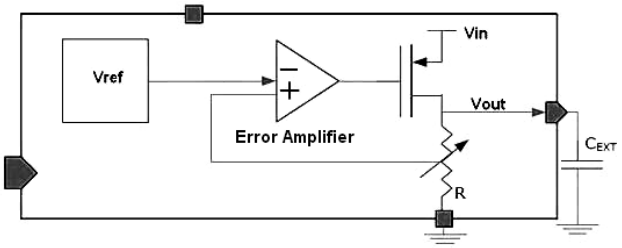

Figure 1. Block diagram representation of a Low Drop out Voltage regulator (LDO).

III. TOPOLOGY SELECTION FOR FAST TRANSIENT RESPONSE LDO

Diagram for a fast transient response LDO is shown in the Figure 2 [8]. For any fast transient response LDO topology the critical part is the design of the buffer stage. Simplest buffer

implementation can be the source follower configuration. Major drawback with this buffer implementation is that it consumes one threshold voltage plus overdrive voltage that is required by the NMOS to operate in saturation and narrows down the output swing which deteriorates the signal to noise ratio (SNR), and also the power supply rejection becomes bad due to body effect (also called back gate effect)[8]. The power supply rejection can be improved considerably by making use of triple well technology where the bulk of the NMOS can be tied separately, but that is an expensive approach and problem of reduced output swing still remains. Another possible solution is to use an unbuffered operational amplifier (OPAMP) in a unity gain configuration [8]. The output resistance of the unity gain buffer is equal to the output resistance of the OPAMP divided by loop gain which can be made very high to get smaller output resistance. This small output resistance generates smaller time constant at the gate of the PMOS which allows faster charging and discharging of the large load capacitance (parasitic gate capacitance of the large PMOS driver); hence the LDO can respond faster to the changing load conditions. This buffer stage is capable of providing rail to rail output so the maximum current can be used for charging or discharging of the parasitic capacitance CP that improves slewing [8].

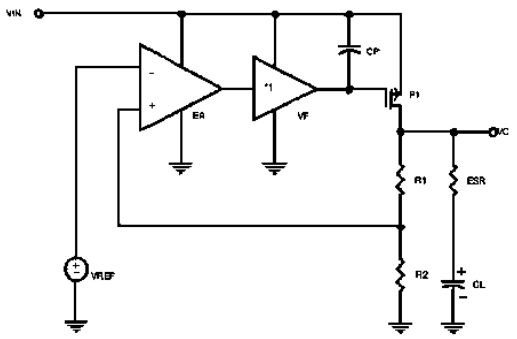

Figure 2. Topology for fast transient response LDO.

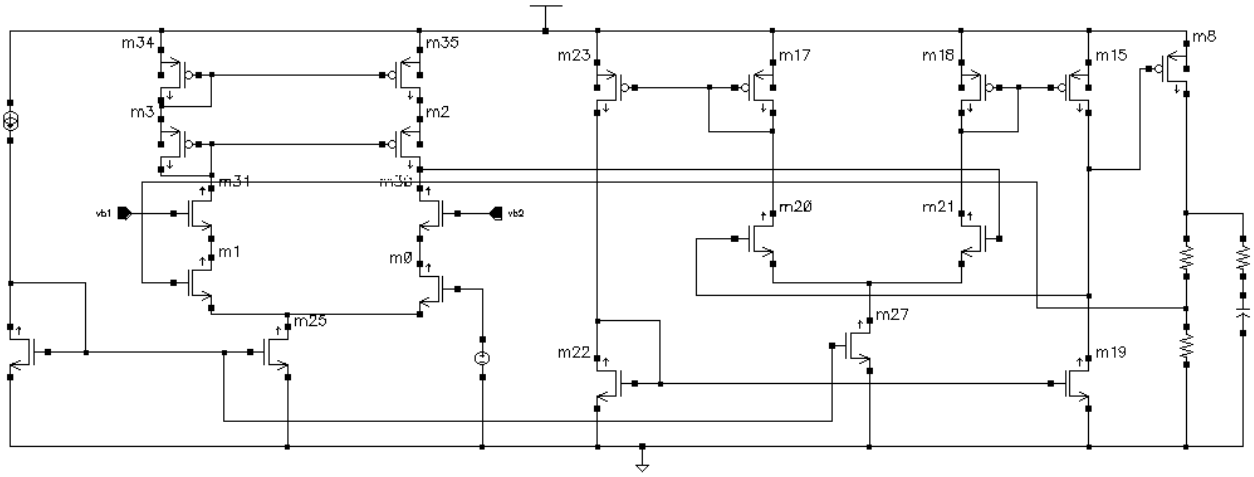

Figure 3. Complete schematic of the fast transient response LDO with single stage differential amplifier used as an error amplifier.

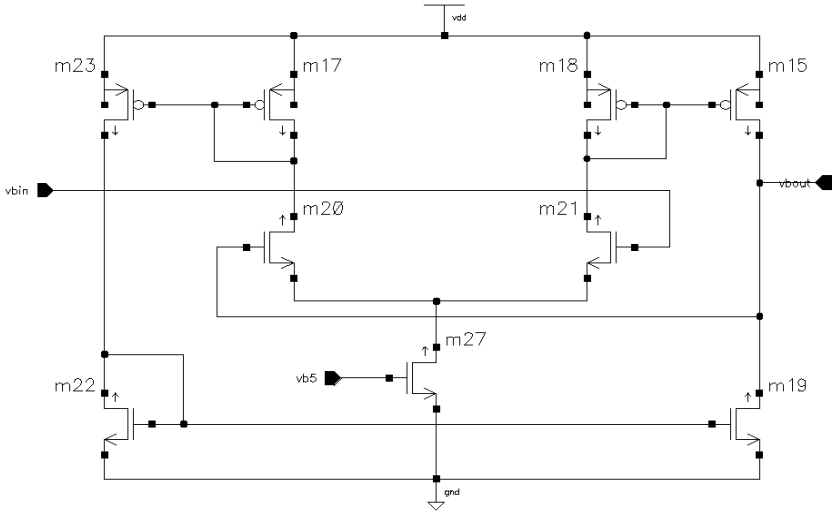

Figure 4. The two stage wide-band OTA used as a Buffer.

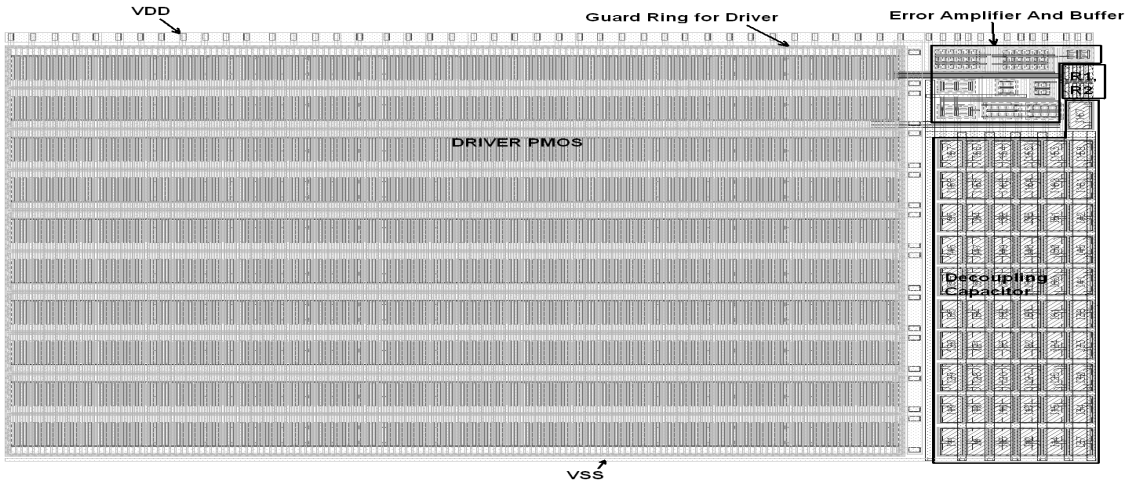

Figure 5. Layout of the Proposed LDO.

IV. Final Implementation of the LDO

The complete schematic of the proposed LDO is given Figure 3. This is a very simple implementation unlike to the reference design which is far more complex [9]. For producing large gain from a single stage, telescopic differential amplifier is used as an error amplifier [2]. The large gain is needed for a good load regulation. Like in implementation of [8] where NMOS used in buffer stage are low-threshold devices, here the design has been done by using generic CMOS technology, so all the devices are of standard threshold. In implementation [8] extra PMOS device is used in the buffer stage between PMOS m23 and NMOS m22 (see Figure 4), but the channel length used here is 0.2um which can introduce drain current variations due to channel length modulation effect. So to avoid this problem we can remove the extra PMOS used in [8]. The design has been implemented on a die of size $290\,\mu \times 180\,\mu$ (see Figure 5).

V. Simulation Results

The key parameters that characterize a LDO are line regulation, load regulation and output voltage variation due to temperature change.

A. 5.1. Load Regulation

The load regulation can be described by the following equation and can be defined as output resistance of the regulator [1]:

$$Load - regulation = \frac{\Delta Vo}{\Delta Io} = \frac{Ro - pass}{1 + Ao\beta} \quad (1)$$

Calculated value of the load regulation (for Vin = Vout + 0.3) is : 0.0055 %/mA (see Figure 6).

B. 5.2. Line Regulation

The line regulation is the measure of the capability of the LDO to maintain constant output voltage in spite of change in the input voltage and is described by [1]:

$$Line - regulation = \frac{\Delta Vo}{\Delta Vin} \quad (2)$$

Calculated value of the line regulation for this LDO (for Vin > Vout + 0.3 and Iload = 0) is : 1.2mV/V (see Figure 7).

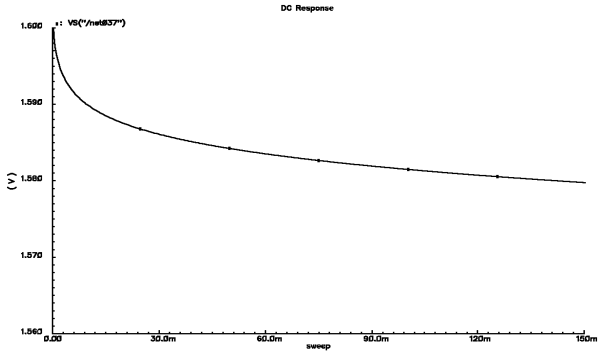

Figure 6. Load regulation of the LDO measured by sweeping load current from 0mA to 150mA.

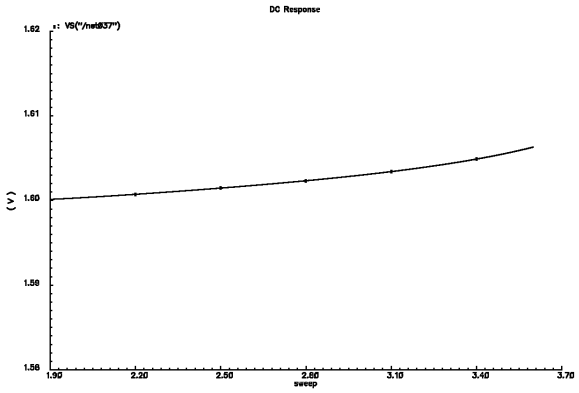

Figure 7. Line Regulation measurement of the LDO.

C. 5.3. Temperature Sweep

Output voltage variations due to temperature has been recorded by sweeping the temperature from $-50\,°C$ to $150\,°C$, the output voltage has been changed from 1.6V to 1.592mV, a change of just 8mV (see Figure 8).

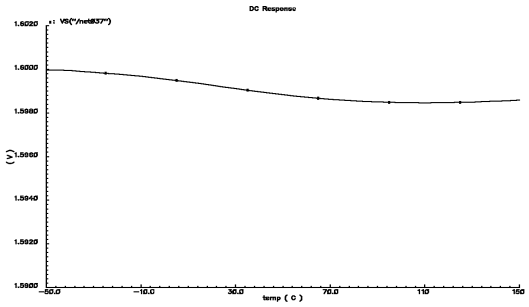

Figure 8. Variation of output voltage across temperature.

D. 5.4. Transient Simulation

The transient simulation was carried out by varying the load current from 0 to 150mA in 1ns back and forth (see Figure 9). The output capacitor used is 2.2uF with ESR of 100milli-ohms. The maximum undershoot seen in the simulation is -14mV when changing load current from 0mA to 150mA and the settling time is a mere 44ns much faster than the reference designs [8][9]. At zero load current the phase margin is $99.1°$ which goes down to $51.4°$ at a load current of 150mA.

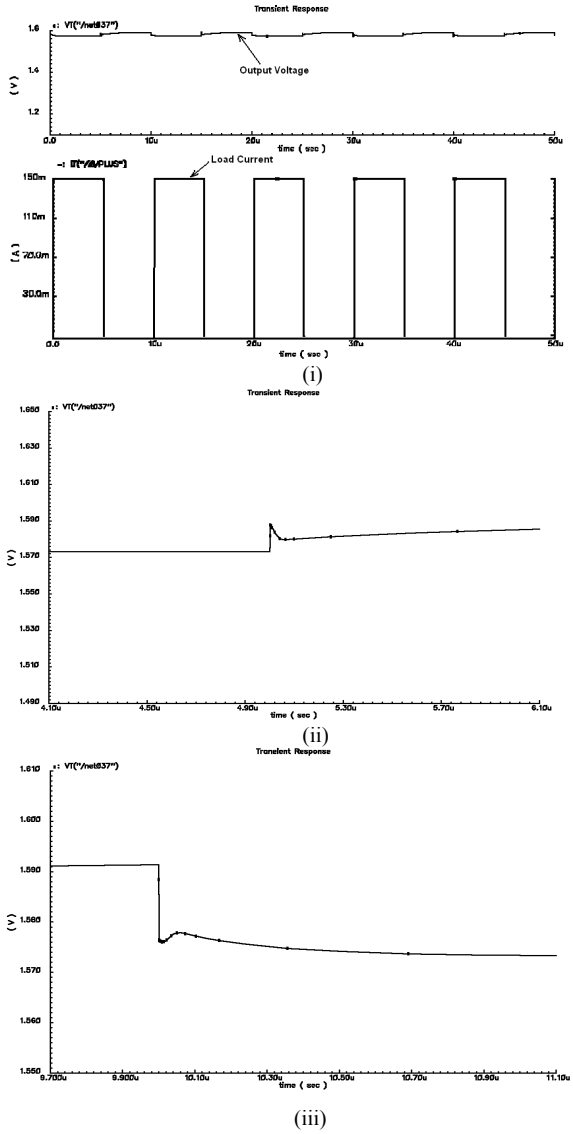

Figure 9. Transient response (Load current is varied from 0mA to 150mA in 1ns back and forth). (i) complete transient simulation result; (ii) load current changing from 150mA to 0mA; and (iii) load current changing from 0mA to 150mA.

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REFERENCES

[1] Gabriel Rincon-Mora, Phillip E. Allen, "A Low-Voltage, Low Quiescent Current, Low Drop-out Regulator". IEEE journal of Solid-State circuits. January 1998

[2] Behzad Razavi. Design of Analog CMOS Integrated Circuits. Boston,MA: McGraw-Hill inc. 2001.

[3] Paul R. Gray, Paul J. Hurst, Robert G. Meyer. Analysis and design of Analog Integrated Circuits. Fourth Edition.

[4] Walt Jung, "Voltage Reference And Low Dropout Linear Regulators". In "Analog-Digital Conversion Handbook"; Analog Devices

[5] P. R. Gray and R. G. Meyer, "MOS operational amplifier design—A tutorial overview," IEEE J. Solid-State Circuits, vol. SC-17, no. 6, pp. 969–982, Dec. 1982.

[6] "Linear and Switching Regulator Handbook", ON Semiconductor.

[7] Findlay Shearer, "Power Management in Mobile Devices" Elsevier Inc. 2008.

[8] C. Stanescu, "Buffer stage for fast response LDO", Semiconductor Conference, 2003. CAS 2003. International, page(s): - 360 Vol. 2.

[9] Chung-Wei Lin Yen-Jen Liu , "A Power Efficient and Fast Transient Response Low Drop-Out Regulator in Standard CMOS Process", VLSI Design, Automation and Test, 2006 International Symposium on.