

Cell Capacitor Sizing in Modular Multilevel Converters and Hybrid Topologies

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Keywords

«HVDC», «Voltage Source Converter (VSC)», «Multilevel converters», «Energy storage», «Modelling».

Abstract

This paper presents a method to calculate the minimal size of cell capacitors in multilevel VSCs which meets a maximum voltage deviation criterion under ideal conditions. This method is applied to the Modular Multilevel Converter (MMC), the Alternate Arm Converter (AAC) and the hybrid multilevel converter with ac-side cascaded H-bridge cells (AC-CHB). The results show that the newer VSC topologies exhibits smaller energy deviation in their stacks, leading to an overall smaller volume of cell capacitors for the converter station but often accompanied by some compromises such as higher power losses or degraded DC current waveform quality.

Introduction

Over the last decade, VSCs and especially modular multilevel topologies have become the new standard in HVDC [1]. The first topology of this last class of VSC is the Modular Multilevel Converter (MMC) [2], illustrated in Fig. 1, and was the first to provide both low switching losses and low AC current distortion. These features contributed to the higher power efficiency and the significant reduction in the size of the AC filters. Recently, hybrid topologies have emerged [3-8], some of them exhibiting DC-side fault blocking capability. These topologies have also been used in DC/DC conversion applications [9] and have been shown to have a better distribution of temperature between the IGBT modules [10]. Reduced Dynamic Models have also been developed [11-12]. However, all these converter topologies rely on charged capacitors inside the numerous cells constituting their stacks in order to generate the required converter voltage. Even when the conditions to keep the average voltage of these cell capacitors at their nominal value are met, the cell voltages will inherently fluctuate during the course of each fundamental cycle because of the current passing through them. As presented in [2-9], [13-16], the main solution to prevent these cell capacitors from either overcharging or undercharging consists in sizing them big enough in order to limit their voltage deviation during a fundamental cycle. This paper presents a method to calculate the minimal size which ensures that these cell capacitors have their voltage kept within pre-determined voltage boundaries under ideal steady state normal conditions. This method is then applied to the half-bridge MMC [2] and two recently presented hybrid VSCs, namely the Alternate Arm Converter [3-5] (AAC), shown in Fig. 2, and the hybrid multilevel converter with ac-side cascaded H-bridge cells [6-8] (AC-CHB), shown in Fig.3. A comparison between these topologies is then drawn and discussed with the potential trade-offs summarized.

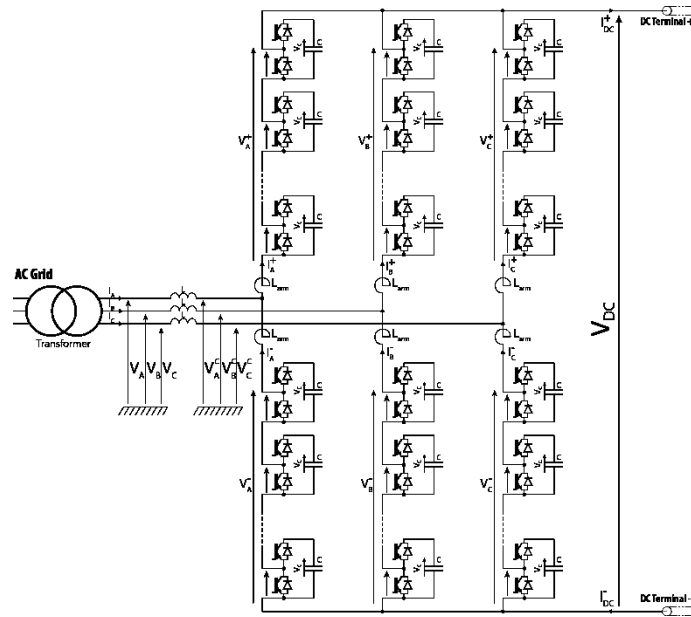


Fig. 1 – Half-bridge Modular Multilevel Converter topology

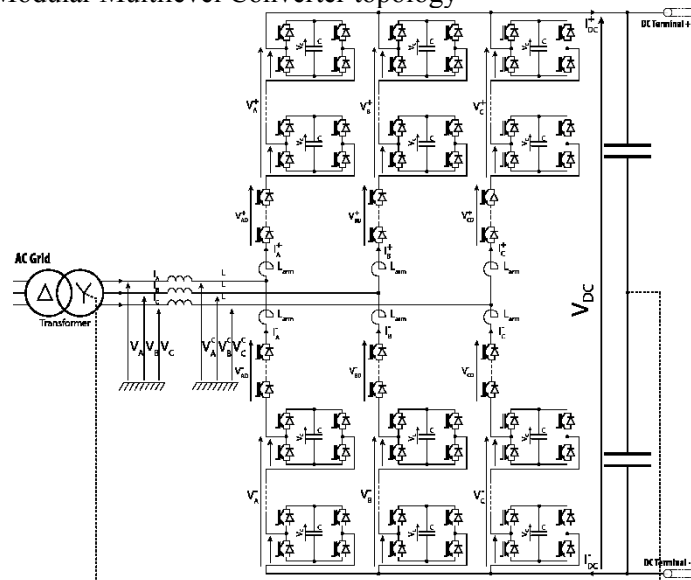


Fig. 2 – Alternate Arm Converter topology

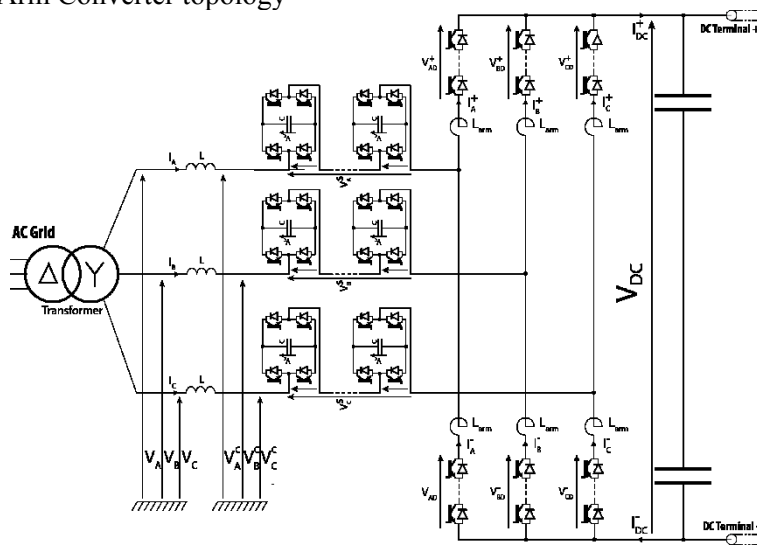


Fig. 3 – AC-side Cascaded H-Bridge Converter topology

Cell Capacitor Sizing

Assumptions and Objectives of the Cell Capacitor Model

In order to limit the extent of this study and keep the simplicity of its results as well as its generality, a number of assumptions have been set on the mathematical model of the studied topologies. First, the cells in the stacks are considered as loads meaning that, in the load convention, a positive power denotes power going in the stacks, hence its energy will be positive and the cell capacitors will exhibit increasing voltage magnitudes, and vice-versa. Second, only the theoretical voltage and current waveforms during steady state operation are considered. This implies that the voltage of the stacks does not present the staircase shape which is characteristic of the multilevel converters but is rather assumed to be smooth and as close as possible to its ideal waveform. Third, the stored energy in the different inductors of the converters is neglected as would have a marginal but complex influence on the final solution. Indeed, in transmission applications, this inductive energy is usually small, being between 1 and 2 orders of magnitude smaller than the stored energy in all the cell capacitors. Fourth, the mathematical model developed for this study assumes that the duty of the cells is perfectly distributed between them, meaning that all the cell capacitors in a stack share the same voltage level at any point in time. Voltage deviation between the cell capacitors is not discussed in this study and is the topic of cell rotation algorithms. Finally, the results provided by these study correspond to the bare minimal size that the cell capacitors should be designed at to achieve the desired maximum voltage deviation and do not take into account any additional margin that a manufacturer may request to meet some requirements or situations, e.g. transients, faults.

Voltage and Energy Deviation

The average voltage of a cell in a stack is dependent of the total energy stored in this stack, as described in (1). By designing the energy controller which is in charge of managing the average energy level in the stack such that the cell capacitor voltages exhibit as much positive voltage deviation as negative voltage deviation around the nominal cell voltage value, then it can be proven [14] that the nominal energy storage of the stack (3) is proportional to the total energy deviation (2) divided by the maximum allowed voltage deviation (in per unit, e.g. 0.1).

$$E_{\text{stack}}(t) = N_{\text{cell}} \frac{C_{\text{cell}}}{2} V_{\text{cell}}^2(t) \quad (1)$$

$$\Delta E_{\text{stack}} = \Delta \hat{E}_{\text{stack}} - \Delta \check{E}_{\text{stack}} \quad (2)$$

$$E_{\text{stack}_{\text{nominal}}} = \frac{\Delta E_{\text{stack}}}{4 \Delta V} \quad (3)$$

The size of a cell capacitor can thus be derived (4) using the energy storage definition (1). Equation (4) shows that the cell capacitor value and the resulting cell voltage deviation are linked linearly, meaning that doubling the cell capacitor value will result in halving the cell capacitor voltage deviation for the same operating condition.

$$C_{\text{cell}} = \frac{\Delta E_{\text{stack}}}{2 N_{\text{cell}} V_{\text{cell}_{\text{nominal}}}^2 \Delta V} \quad (4)$$

The total energy deviation (2) is defined by the difference between the maximum and minimum energy deviations which occur within the course of a fundamental cycle. The main method to describe the energy deviation equation consists in integrating the power of the stack which is calculated from the product of its voltage and current waveforms as in (5).

$$E_{\text{stack}}^+(t) = \int_0^t V_{\text{stack}}(t) I_{\text{stack}}(t) dt \quad (5)$$

The converter voltage waveform is assumed to be an ideal sine wave whose magnitude is optimally chosen to fit the studied topology. The AC current waveform is also a sine wave with a phase delay Φ with the AC voltage waveform. Depending on the studied topology, the voltage waveforms may differ significantly, as shown in Fig. 4, and Fourier analysis will be performed to keep the continuity of the mathematical model.

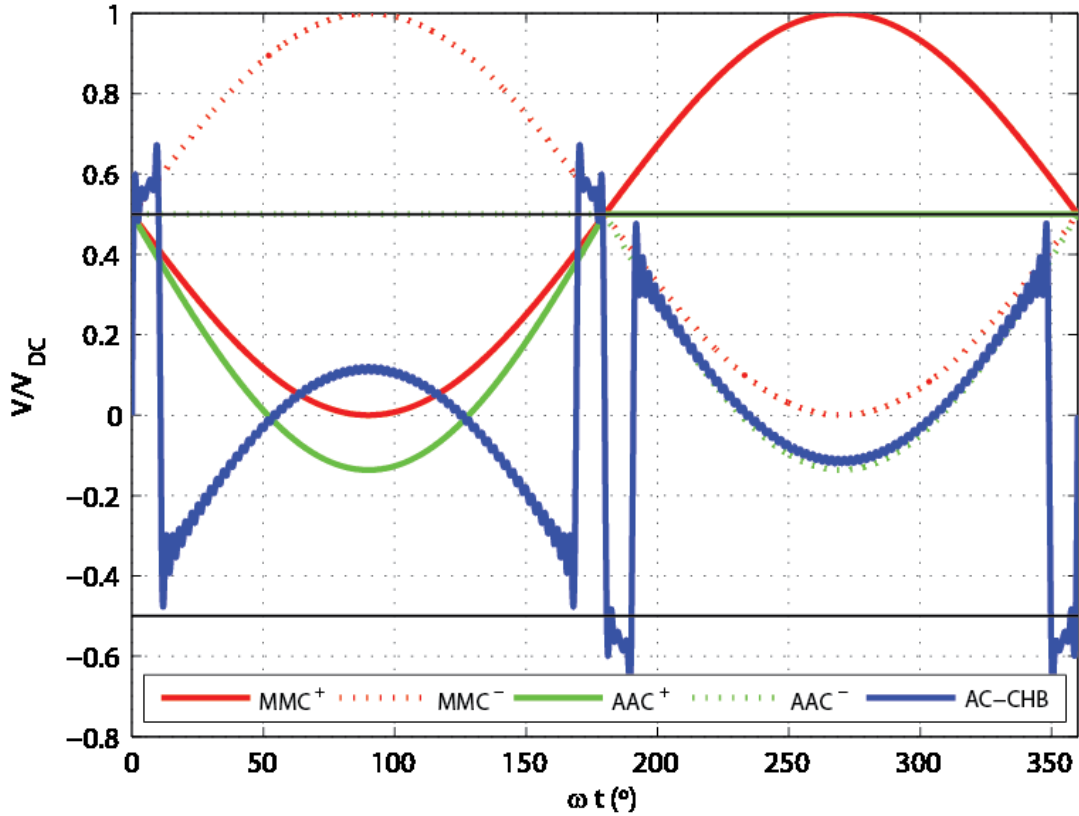


Fig. 4 - Stack voltage waveforms for the stacks of the MMC, AAC and AC-CHB

Case of the MMC

The MMC is the most well-known multilevel VSC as it exhibits very interesting characteristics such as almost distortion-free current waveforms on both the AC and DC sides. Since the half-bridge MMC is largely favoured over its full H-bridge counterpart, the former version is exclusively considered in this study. Despite the attractive lower power losses of the half-bridge MMC, this variant has several shortcomings, one of which consisting in the inability from its stacks to generate negative voltage levels. This implies that the AC peak voltage has to be constrained by the DC terminal voltages, thus giving the definitions (6) and (7) of respectively the AC peak voltage and the number of cells in a stack, when no triplen harmonic voltage injection is involved.

$$\hat{V}_{AC} = \frac{V_{DC}}{2} \quad (6)$$

$$N_{cell_{MMC}} = \frac{V_{DC}}{V_{cell_{nominal}}} \quad (7)$$

By using (5), the energy deviation of the top arm can be expressed as in (8) which is remarkably proportional to the energy exchanged per fundamental cycle. The bottom arm has a similar energy deviation equation but with both an opposite sign and reversed time. This can be explained by the nature of the voltage waveform of the MMC stacks as illustrated in Fig. 4.

$$E_{stack}^+(t) = \frac{|S|}{3\omega} \frac{1}{4} \left(-\cos(\omega t - \Phi) - 2 \cos(\Phi) + (3 - \sin(\omega t)) \cos(\omega t + \Phi) \right) \quad (8)$$

When plotting in time the energy deviation obtained from (8) for different operating points, as shown in Fig. 5, one can observe that the MMC stack exhibit slightly more energy deviation during pure reactive power operation as opposed to active power operation. The different operating points also show a certain symmetry with the time axis.

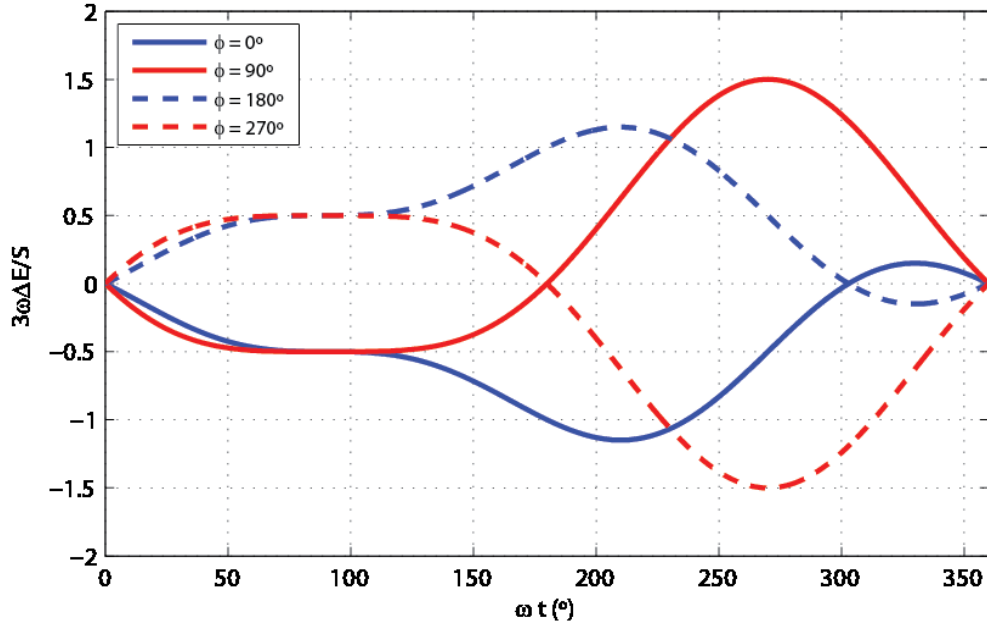


Fig. 5 - Energy deviation of the top stack in the MMC

Case of the AAC

The Alternate Arm Converter (AAC) is one of the proposed hybrid VSC topologies presented in [3-5] and illustrated in Fig. 2. This converter offers the same level of power efficiency as the half-bridge MMC but also the DC-fault blocking capability of the full bridge MMC [4]. The AAC operates by alternating the working periods of its arms resulting in (i) a reduction in the maximum voltage of its arms and (ii) a direct rectification of the AC current into a DC current with a 6-pulse ripple. The AAC operates at its best at its sweet spot (9) where the AC and DC energy quantities match, which is defined by a linear relationship between the AC and DC voltage magnitudes. Using both the sweet spot definition (9) and the fact that the stacks have to support the full AC voltage during a DC-side fault, the number of cells per stack can be expressed as in (10).

$$\hat{V}_{AC} = \frac{2}{\pi} V_{DC} \approx 0.637 V_{DC} \quad (9)$$

$$N_{cell_{AAC}} = \frac{2}{\pi} \frac{V_{DC}}{V_{cell_{nominal}}} = 0.637 \frac{V_{DC}}{V_{cell_{nominal}}} \quad (10)$$

Equation (5) applied to the top arm of an AAC yields (11) with $0 \leq \omega t \leq \pi$. The bottom arm has the same energy deviation equation but only time shifted since its working period is during the other half of the fundamental cycle as opposite to the top arm.

$$E_{stack}^+(t) = \frac{|S|}{3\omega} \frac{1}{2} (\cos(\omega t + \Phi)(\pi - 2 \sin(\omega t)) - \cos(\Phi)(\pi - 2\omega t)) \quad (11)$$

When looking at the energy deviation of the top arm during the course of a cycle for different operating points, as illustrated in Fig. 6, it can be observed that the top arm only exchange energy during the first half of the fundamental cycle as it corresponds to its working period. Furthermore the highest energy deviations occur during reactive power operations of the AAC although the energy deviation relative magnitude is lower than the MMC.

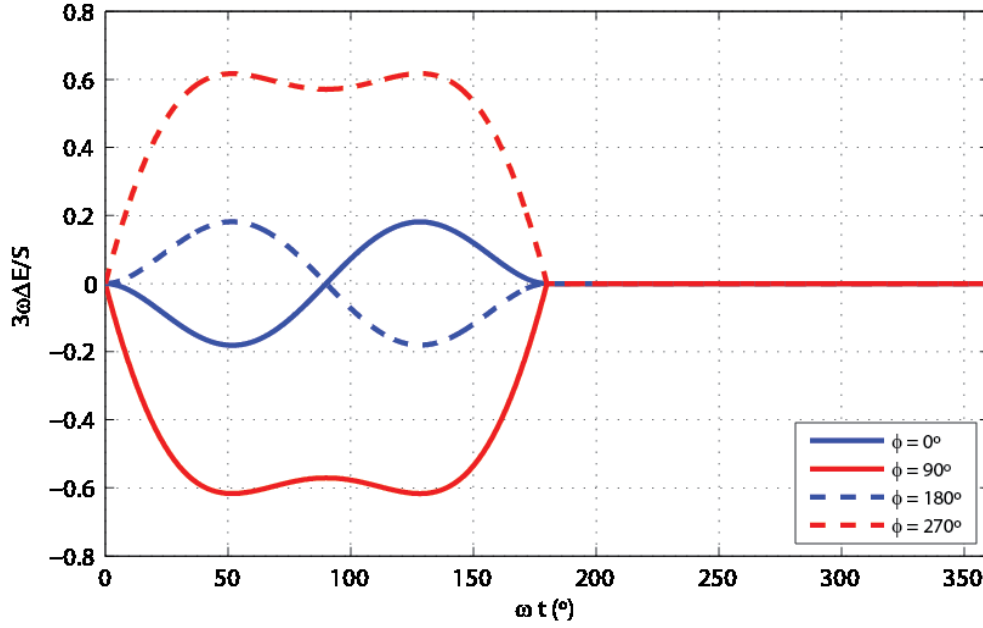


Fig. 6 - Energy deviation of the top stack in the AAC

Case of the AC-CHB

The hybrid multilevel converter with ac-side cascaded H-bridge cells (AC-CHB) is another hybrid topology suggested in [6-8] and illustrated in Fig. 3. As for the AAC, the AC-CHB offers DC fault blocking capability but uses even fewer cells compared to AAC because it has only one stack per phase leg, although it has been shown in [8] that the power efficiency of the AC-CHB is not as high as either the half-bridge MMC or the AAC. The AC-CHB operates by connecting its stacks of cells either to the positive or negative DC terminal through a string of series-connected IGBTs with a rapid period of alternations around the mid-cycle point for a period defined by the angle α . The value of the angle α is chosen to ensure a perfect match between the AC and DC energy quantities exchanged during the conversion process as defined in (12).

$$\frac{2}{\pi} V_{DC} (2 \cos(\alpha) - 1) = \hat{V}_{AC} \quad (12)$$

As the DC fault blocking is also a desired feature of the AC-CHB, the stacks have to be able to support the full AC grid voltage which provides (13). Together with (12), it gives the AC voltage magnitude definition (14), hence the number of cells (15) remarkably close to the number of cells in the AAC (10).

$$\hat{V}_{AC} (1 - \sin(\alpha)) = \frac{V_{DC}}{2} \quad (13)$$

$$\hat{V}_{AC} = k_{ACCHB} V_{DC} \approx 0.614 V_{DC} \quad (14)$$

$$N_{cellACCHB} = k_{ACCHB} \frac{V_{DC}}{V_{cellnominal}} = 0.614 \frac{V_{DC}}{V_{cellnominal}} \quad (15)$$

The study of the energy deviation of the stack using (5) yields (16) which can be found by performing a Fourier series analysis of the stack voltage waveform.

$$E_{stack}(t) = \frac{|S|}{3\omega} \sum_{n=1}^{\infty} \frac{2}{\pi n k_{ACCHB}} \frac{1 - (-1)^n}{n^2 - 1} (1 - 2 \cos(n\alpha)) (\cos(\omega t + \Phi) \sin(n\omega t) - n \sin(\omega t + \Phi) \cos(n\omega t) + n \sin(\Phi)) \quad (16)$$

Energy deviation waveforms have been plotted in Fig. 7 for different operating points. The rapid changes in connection between the positive and negative DC terminals are easily identifiable by the sharp changes in directions of the curves around the half-period points. Compared to the AAC, the magnitudes are generally even smaller, indicating that the AC-CHB requires smaller energy storage in its stacks.

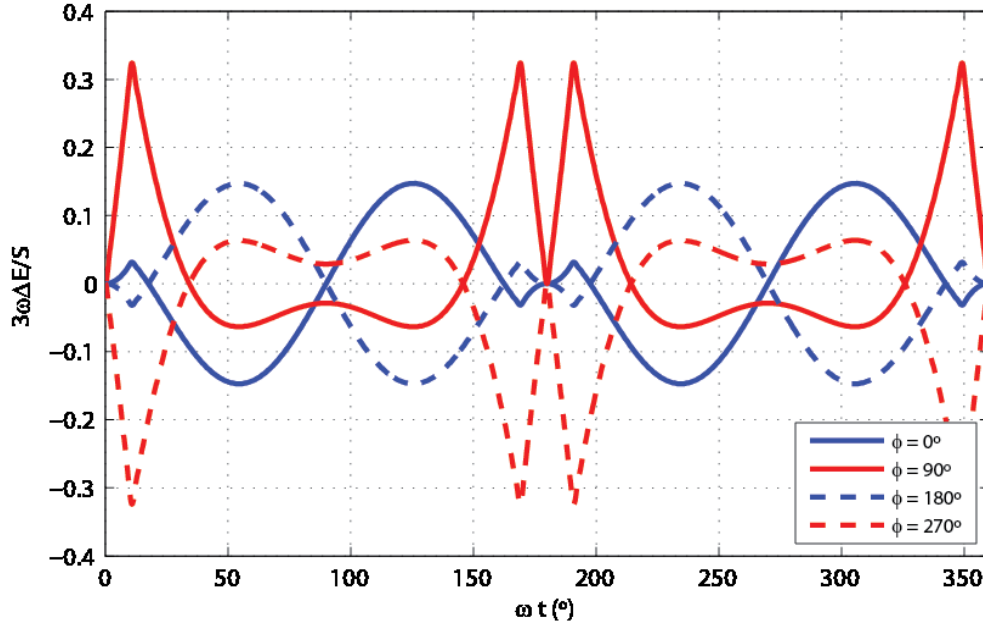


Fig. 7 - Energy deviation in the stack of the AC-CHB

Comparison between the Different Topologies

Energy Deviation

As shown in (3) and (4), the total energy deviation is the main relevant parameter when sizing the energy storage in the stacks, i.e. the cell capacitors. Numerous numerical computations have been performed on the parts of equations (8), (11) and (16) which does not depend on the amount of energy transferred per cycle, i.e. $|S|/3\omega$ since all the energy deviation equations (8), (11) and (16) are linear to the amount of energy processed per cycle. The minimum and maximum values were found, then the maximum total energy deviation for different values of the phase angle Φ were computed and put in Fig 8.

From these values, the MMC clearly exhibits the highest level of total energy deviation per stack, followed by the AAC then the AC-CHB. This fact is further supported by Equations (17), (18) and (19) which give the maximum total energy deviation found for each topology and at which phase angle Φ .

$$\Delta E_{stack_{MMC}} \approx 2.000 \frac{|S|}{3\omega} \text{ at } \Phi = 90^\circ \quad (17)$$

$$\Delta E_{stack_{AAC}} \approx 0.643 \frac{|S|}{3\omega} \text{ at } \Phi = 74^\circ \quad (18)$$

$$\Delta E_{stack_{AC-CHB}} \approx 0.427 \frac{|S|}{3\omega} \text{ at } \Phi = 65^\circ \quad (19)$$

All three topologies have their lowest amount of energy deviation when converting only active power, and increased energy deviation when more reactive power is involved in the conversion process.

Capacitor Sizing

Using the maximum energy deviation that each topology can exhibit, i.e. (17), (18) and (19), and by putting this equations into (4), the minimum cell capacitor sizing guidelines (20), (21) and (22) can be established respectively for the MMC, AAC and the AC-CHB for operation under normal conditions.

$$C_{cell_{MMC}} \geq \frac{|S|}{3\omega V_{DC} V_{cell_{nominal}} \Delta V} \frac{1.000}{\Delta V} \quad (20)$$

$$C_{cell_{AAC}} \geq \frac{|S|}{3\omega V_{DC} V_{cell_{nominal}} \Delta V} \frac{0.505}{\Delta V} \quad (21)$$

$$C_{cell_{AC-CHB}} \geq \frac{|S|}{3\omega V_{DC} V_{cell_{nominal}} \Delta V} \frac{0.348}{\Delta V} \quad (22)$$

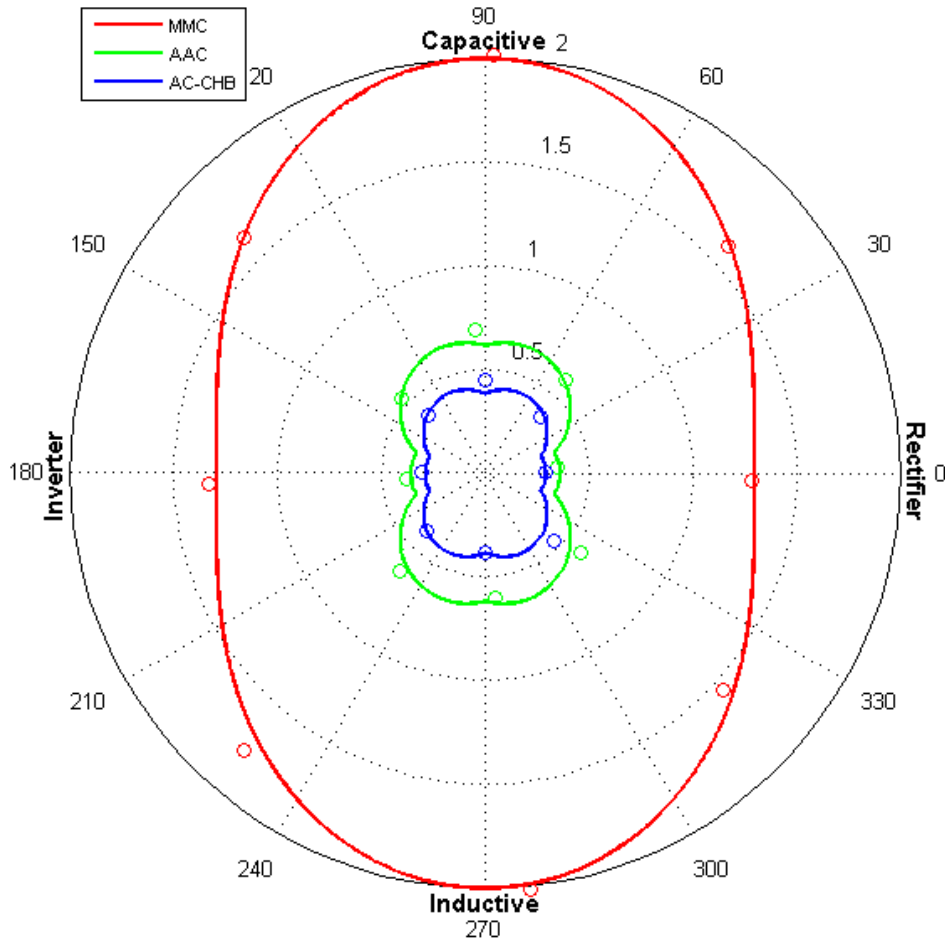


Fig. 8 - Total relative energy deviation of one stack in the MMC, AAC and AC-CHB (the solid lines represent the theoretical value and the small circles show the measured values in simulations)

Simulation Results

In order to appreciate the consequences of the cell capacitor sizing equations derived in the previous section, i.e. (20), (21) and (22), each of the three converters have been modelled with their main parameters listed in Table I together with a quick summary of the features associated with each topologies studied in this paper. First the total energy deviation for each topology has been measured for different operating points. The data gathered in these simulations are plotted on Fig. 8 and show a good match with the developed mathematical models. Second, the average voltage deviation waveforms are also compared to what the mathematical models predict with one operating point shown for the MMC, AAC and AC-CHB, respectively in Fig. 9, Fig. 10 and Fig. 11. Again the good match between the simulation results and the prediction provides confidence in the developed models.

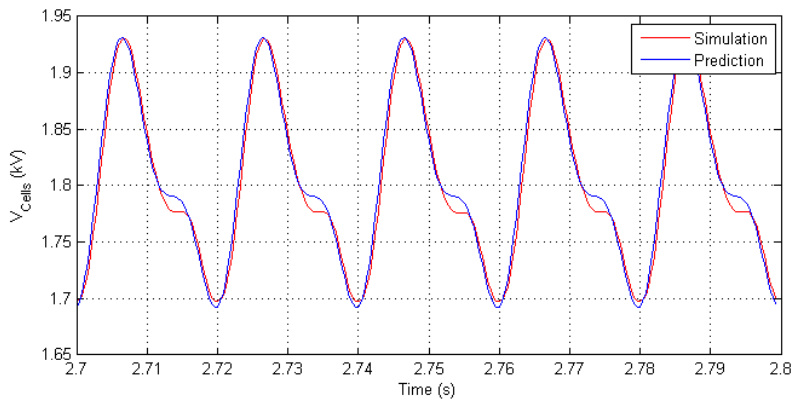


Fig. 9 - Average cell capacitor voltage in an MMC at unity power factor

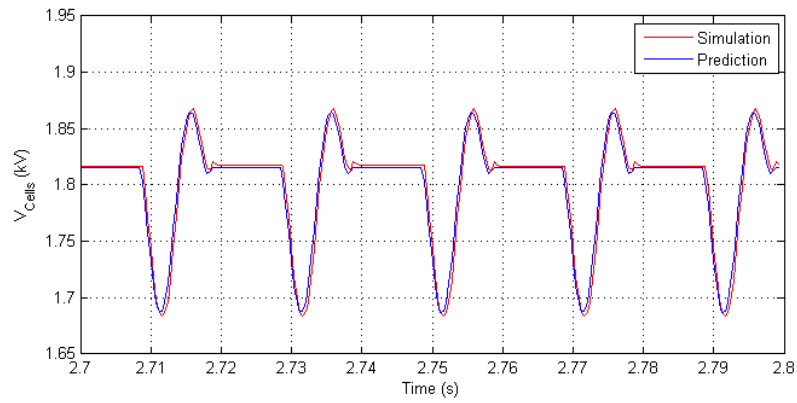


Fig. 10 - Average cell capacitor voltage in an AAC at unity power factor

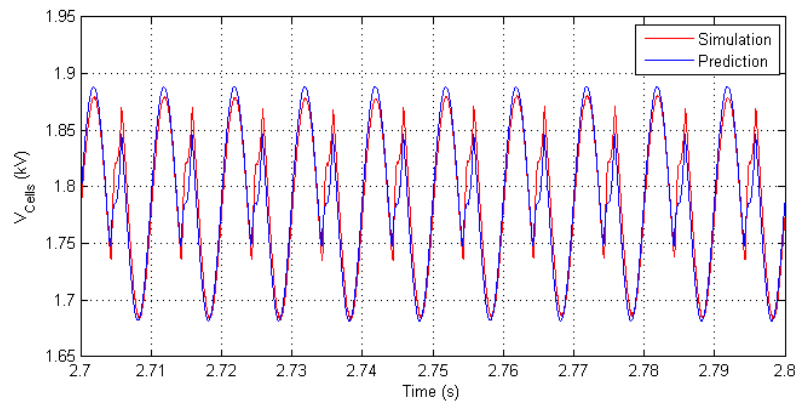


Fig. 11 - Average cell capacitor voltage in an AC-CHB at unity power factor

Table 1 – Parameters of the Simulation Models

	MMC	AAC	AC-CHB
Power	120 MW	120 MW	120 MW
DC bus	±50 kV	±50 kV	±50 kV
AC line	61.2 kV	78.0 kV	75.2 kV
Cell voltage	1.8 kV	1.8 kV	1.8 kV
Number of cells per stack	56 (6 stacks)	36 (6 stacks)	35 (3 stacks)
Cell capacitor @$\Delta V = 10\%$	7.02 mF	3.51 mF	2.38 mF
Total stored energy	3.82 MJ	1.23 MJ	0.40 MJ
DC filter	Very small	Large	Large
DC fault blocking	No	Yes	Yes
Power efficiency	High	High	Moderate

Conclusion

The mathematical model described in this paper has permitted to derive simple design rules aiming at determining the minimal size of the capacitors in the cells of multilevel converters, such as the MMC, AAC and AC-CHB, under normal operation. Simulation results on 120 MW converters were also provided and confirmed the fact that the AC-CHB has a total cell capacitor size 3 times smaller than the AAC and almost 10 times smaller than the MMC. However, the AC-CHB suffers from very high power losses making this topology more suitable for applications when space constraints are the most important issue. The AAC is also a good compromise as its total cell capacitor volume is equivalent to a third of the volume of the MMC and still offers DC side fault blocking. However, both hybrid topologies generate non smooth DC current waveforms which may require additional DC-side filtering.

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