UNIVERSITY OF LONDON

FACULTY OF ENGINEERING

High Speed ~~Accurate~~ Quantization of Voltage Signals.

A Thesis presented for
the Degree of Doctor of Philosophy
by

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ABSTRACT

A quantizer is described, the present prototype of which is capable of performing 6000 analogue-to-digital conversions per second with a precision of ±0.5% of full scale. The apparatus was built to investigate a new type of potentially adaptive circuit usable in the design of highly flexible laboratory equipment; it illustrates a principle by which a high speed self-adjusting voltage reference can follow the variations of an input signal within one quantization interval.

A detailed analysis is presented of problems arising in the use of tunnel diodes in long chains to generate accurately defined staircase waveforms intended to serve as a stepping reference in the quantizer. It is shown that as many as 2000 voltage levels could be defined in this way with a combination of six chains; a tolerance of ±11% on the driving pulse amplitude is acceptable for chains containing ten tunnel diodes, provided that the rise time of these pulses is longer than some 20 nanoseconds. The chains can be operated continuously at repetition rates up to ten million pulses per second. A complete voltage reference, using four chains and defining 200 levels, is shown to offer a high speed of operation and a very low thermal drift owing to a temperature compensation effect between the chains.

The switching action of a tunnel diode is described qualitatively and a relaxation oscillator is analysed using a linear approximation of the tunnel diode characteristic. From this analysis, a general method is developed for the design of various tunnel diode-transistor hybrid switching circuits; it gives a timing precision better than ±5% for operating frequencies up to about 20Mc/s. Application of the method to the design of one-tunnel diode flip flops, monopulsers, relaxation oscillators and an adjustable voltage level discriminator is illustrated.

It is maintained that the technique, which is applied successfully throughout the quantizer, provides a simple though powerful tool for the design of tunnel diode switching circuits. Complete specifications for the prototype of the quantizer built in the laboratory, are included and it is argued that the remarkable flexibility inherent in the technique employed should encourage further investigations along these lines in view of a possible extension to a new class of circuits with a significant degree of adaptability.

ACKNOWLEDGMENTS

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Introduction.

The work described here has been carried out in the Engineering in Medicine laboratory of Imperial College and has been intended to assist current research in bio-physics. One of the most striking features of bio-physical research is probably that it covers a large variety of widely differing problems. This situation arises from the complexity of the subject under study and it creates a need for correspondingly versatile laboratory equipment capable of coping with a variety of often unforeseeable operating requirements.

The problem was presented a few years ago, in conjunction with the requirements of the laboratory, of investigating the potentiality of adaptive circuit techniques in the design of highly flexible laboratory equipment intended primarily for physiological measurements. In the present context, the term "adaptive" was used to describe a class of circuits in which the mode of operation or the transfer characteristic can be altered according to the behaviour of an input signal. Furthermore, it was decided to couple this study of a new potentially adaptive circuit to an investigation of the possibility of employing tunnel diodes to generate accurately defined staircase waveforms which would constitute a stepping reference in the new system and would permit a considerable reduction of the

circuit complexity. The fundamental idea was to use such a voltage reference to track an input variable at a speed depending on some dynamic characteristic of the signal itself and with an easily controlled accuracy. It is easy to imagine that such a system could find many applications in measurements, control as well as transformation of electrical signals. Indeed, an ultimate purpose of this entire study would be to assess the potentiality of such a scheme as the basis of more specifically adaptive operations on signals.

In order to demonstrate some of the salient features of this technique, a new analogue-to-digital converter was designed. The reasons for the choice of this particular application are explained in Chapter 1. It will be shown in that chapter that an adaptive analogue-to-digital converter can prove most useful in a bio-physical laboratory and how it is proposed to build such a converter. Chapter 2 will be devoted entirely to the design of a tunnel diode stepping reference unit. Finally, the remaining part of the thesis will be concerned with the auxiliary circuits completing the quantizer and with a description and evaluation of the over-all performance of the system.

C H A P T E R 1.

Introduction to the Purpose and Design of an Analogue-to-Digital Converter.

1.1. A Note on Electronic Computers.

The well established independent techniques of analogue and digital computation have been supplemented in recent years by techniques simultaneously drawing upon both procedures for the solution of appropriate problems.

It has been common practice to classify electronic computers into two separate groups[1]. Those operating basically on continuous signals are referred to as analogue computers[2], and sequential machines capable of manipulating quantized information are generally called digital computers[3]. A more fundamental approach, advocated by McLeod in 1962[4], was well illustrated in an earlier paper by Glinski[5]. According to his argument, Glinski considered all computers as "processors" and defined the so-called analogue computers as "parallel sequence analog processors with continuous information". Similarly, what is popularly known as digital computers were: "serial sequence analog processors with digitized information". One important characteristic of this classification is that it stresses the complementary aspects of the two methods.

1.2. Needs for Analogue-to-Digital Converters.

Once the concept of complementarity of analogue and digital computers has been introduced, it follows that a true hybrid machine combining the desirable features of both systems, could become a versatile and powerful tool. Various attempts to achieve this goal have been described in the literature[6,7,8,9,10]. Another way of attaining the same results is to utilize each type of computer to solve those parts of one problem for which their characteristic procedures are best suited[11,12]. In this case, some means of interconnecting the analogue and digital computers must be devised as the two units are not directly compatible. The equipment performing the transformation of an analogue (continuous) signal into a digital (quantized) form is known as an analogue-to-digital converter (A-D converter). The inverse operation is effected with a digital-to-analogue converter. Similar occasions for conversion arise whenever a digital computer is introduced into a physical system[13]. In its broadest sense, this last comment applies also to many cases of data handling where the information is available in an analogue form (for instance, continuous voltage signals from a transducer) and when it is desired to take advantage of the special storage facilities offered by digital systems. The utility of digital computers in most of these applications is therefore conditioned by the ability of the A-D converters to meet the various requirements imposed by the input signals.

1.3. Survey of Literature on A-D Converters.

The large volume of technical literature accumulated over the last few years on the description of new A-D converters is one indication of the significance of such devices to the ever increasing versatility of digital computers. Long lists of existing converters have been published already[14,15]. Sorting out such a mass of information is not an easy task. A possible method of classification of all types of A-D converters, whether mechanical, electrical or else, can be found in volume II of "Analogue Computation" by Fifer[16].

1.3.1. Classification of Voltage-to-Digital Converters.

The present work, however, is concerned only with those A-D converters accepting electrical inputs. A comparative survey recently published[17], classified all such converters into four main groups according to their rate of analogue-to-digital conversions per second. The four divisions were listed as follows:

Low speed - up to 10 conversions/second
Medium speed - 10 to 1000 conversions/second
High speed - 1000 to 100000 conversions/second
Video speed - 100000 to 10000000 conversions/second

A description of the various techniques achieving these different speeds is given in the above reference and will not be repeated here.

However, the number of conversions/second is a measure which does not contain sufficient information by itself and the associated precision must be known before much can be said about the performance of a given converter. The present state of the art in analogue-to-digital conversion can be summarized as follows. A precision of 0.01% of full scale is possible at a speed as high as 20,000 conversions/second with converters using successive approximation techniques[17]. For a precision of the order of 0.1% of full scale, speeds between 50,000 to 100,000 conversions/second can be attained[18,19,20]. Much higher conversion rates have been reported[21,22]. Reference 22, for instance, describes a scheme working on a combined serial-parallel principle, operating at a clock frequency of 300Mc/s. As many as 50 million conversions can be carried out every second at a precision of 1.5%. Between these extremes of speed and precision, a number of converters have been developed to satisfy the needs created by a large array of applications[23,24,25,26,27,28].

1.3.2. General Remarks.

It is not the purpose of the present discussion to establish the relative merits of existing converters as a fair comparison can only be based on an adequate knowledge of the intended applications. On the other hand, certain general conclusions can be drawn after a careful study of

the literature.

Firstly, for any given technique, a higher conversion rate is normally possible at the cost of reduced precision. ~~speed~~.

Secondly, most high speed accurate A-D converters can be represented as refined versions of the unit described by the basic block diagram of figure 1. The function of every unit should be evident from its name and only a brief explanation needs to be given. The comparator produces an error signal, e_o, which is dependent on the relative amplitudes of the input signal, E_{in}, and the reference signal, E_r. That error signal operates a digital control unit which uses an accurate reference supply to produce a certain digital code. The feedback action from the decoder tends to reduce e_o. A digital representation of E_{in} is obtained whenever E_r approaches E_{in} within less than the equivalent of the least significant digit of the system.

Finally, no single A-D converter is likely to best solve all problems. To a certain extent, a converter must be tailored in accordance with the characteristics of the signal to be transformed; this is of course the main reason for the large variety of converters already available or under development. As for all engineering problems, the design of analogue-to-digital conversion equipment must take into account such features as flexibility, performance,

BASIC BLOCK DIAGRAM
OF ELECTRONIC A-D CONVERTERS

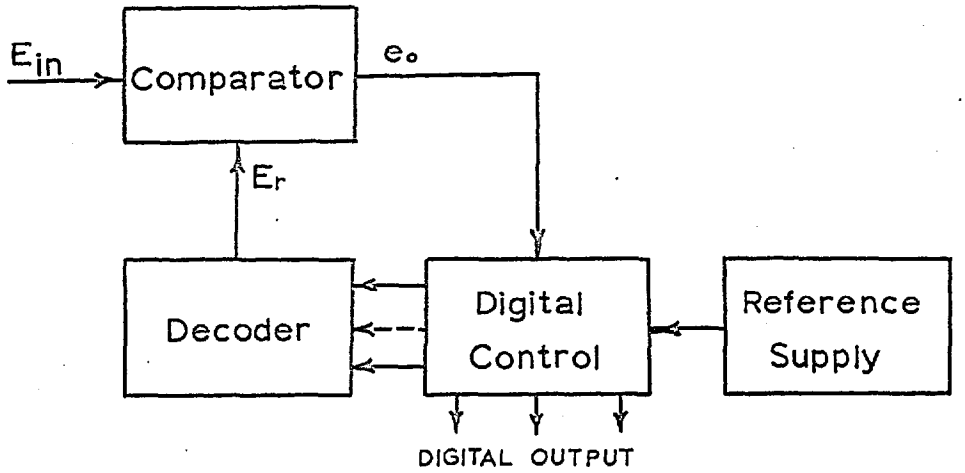


Fig. 1.

BASIC BLOCK DIAGRAM
OF PROPOSED CONVERTER

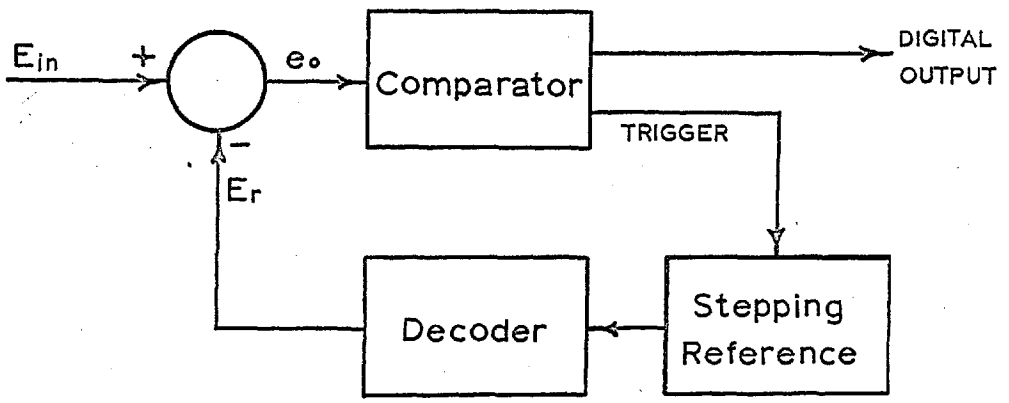


Fig. 2.

reliability, cost, size and maintenance. The final choice involves a number of compromises depending on the order of priority assigned to these various factors.

These basic considerations will now be used as a guide in establishing the specifications for a new A-D converter.

1.4. Proposed Analogue-to-Digital Converter.

1.4.1. Specifications.

It is often necessary to handle large quantities of information presented as analogue electrical outputs, say, of transducers; this situation arises particularly, for example, in bio-physical research. This application is of special interest in the context of the laboratory where the present work has been conducted. A most powerful method of tackling such problems is to express these signals into a digitally coded form and to use a digital computer to analyse the results. A suitable A-D converter to serve such a purpose would be required to meet the following specifications.

(a) The frequency range should extend from very low, i.e. a fraction of a cycle per second, to approximately 10Kc/s.

(b) A precision better than 1% should be maintained up to about 1Kc/s.

(c) Low speed operation at 0.1% precision may be needed in certain cases and should not exceed the absolute limit imposed by the method used.

(d) Facilities for trading precision for speed would represent a significant advantage as it would allow for higher conversion rates when necessary.

(e) The converter should accept positive and negative input signals of a fraction of a volt as well as tens of volts full scale amplitude. It means that the lower limit for the least significant digit should be equivalent to no more than a few millivolts.

(f) Provision to balance out large DC components from the input signal and to shift the zero level at the input over the full dynamic range may also prove useful.

From the survey outlined in section 1.3., it can be concluded that in principle, specifications similar to those mentioned should lie within the potentiality of existing A-D converters. In practice, however, it is difficult to select a unit combining all of these properties. In order to obtain the desired performance, it is necessary to resort to complex and

expensive devices which for many purposes would be utilized in a very inefficient way. Even so, the rigidity of the practical scheme would often limit the range of possible uses.

It was therefore felt desirable to consider the possibility of designing an A-D converter especially suited to the conditions just described. The particular interest of the Engineering in Medicine laboratory in physiological measurements has dictated that special attention be paid to the feasibility of trading speed with precision for various purposes; many biological measurements demand low precision (5%) and high speed while, for others, a precision of one or two orders better, at low speed is desirable. Indeed, it became clear that such an instrument could be not only of real value in biological engineering but would prove equally useful in a number of similar situations. It was thus decided to conceive the new A-D converter as a piece of general laboratory equipment i.e. which could be utilized flexibly for various purposes requiring different speeds and precision. The specifications already established were consequently orientated towards achieving maximum system flexibility while reducing complexity, maintenance and cost to a minimum. The argument leading to the proposed form of solution will now be outlined.

1.4.2. Proposed Solution.

Before pursuing the detailed development of the A-D converter, certain decisions were required regarding the choice of a method of approach.

In the light of the experience gained from a survey of the literature, it seemed that a converter of the asynchronous and incremental type offered the possibility of an interesting solution. It was realized that such a system would be inherently compatible with the special emphasis on flexibility. This point can be clarified by a brief description of the fundamental properties of incremental devices. In an incremental converter, a single signal event indicates when the input variable has changed by one quantum interval corresponding to the smallest unit of measure in the system. These events are then added through pulse counting or similar techniques and the excursions of the controlled variable are time integrals of these data pulses. The level reached by the input signal at the instant a pulse is generated, becomes automatically the zero reference level for the next displacement.

A block diagram representation of the proposed A-D converter is given in figure 2. Its operation is easy to explain on an incremental basis. Whenever the

error signal, e_o, obtained from the difference between the input variable, E_{in}, and the feedback voltage, E_r, reaches a given positive or negative amplitude, the comparator generates an output pulse of the corresponding polarity. At the same time, the reference is adjusted by one quantum interval, returning e_o to zero and establishing the next level of operation. The advantages of this technique will be discussed in detail in Part II of the thesis but certain points must be elucidated here.

It was recognised that to avoid using a fixed clock pulse frequency and to adopt a completely asynchronous system would minimize restrictions on the flexibility of the resulting apparatus. Some design problems may be simpler in synchronous machines but it is believed that the extra difficulties were outweighed by the advantages of having a converter capable of adjusting its pace to the characteristics of the input signals. In this respect, the proposed converter may be described as a true quantizer because the input signal is transformed according to equal increments of amplitude rather than being sampled at fixed time intervals. The number of conversions per second is high for a rapid rate of change, $\Delta V/\Delta t$, of the input signal and decreases for slowly varying inputs. It will be seen later that this property provides a simple means of trading precision for speed and

vice versa. It is to be emphasized that in this trading capability lies much of the significant potential of a scheme of this type.

The problems related to the design of the comparator also had an important bearing on the choice of the particular layout shown in figure 2. As already mentioned (section 1.3.2., figure 1), most A-D converters employ a comparator of some kind. Certain methods use only one comparator operating over a large dynamic range (serial methods) while others replace this by a number of comparators each acting at a different level (parallel methods). Serious objections could be raised against both approaches for the present application. A large number of parallel units would increase the complexity and the cost of the system. On the other hand, a high speed comparator with an expanded dynamic range would be difficult to build and would have a limited accuracy. In order to avoid these obstacles in an incremental machine, the feedback from the decoder can be applied to a differential input stage, allowing the comparator to operate from an error signal over a fixed amplitude range. This expedient simplifies considerably the design of the comparator. Any error introduced at that stage represents only a fraction of one quantum interval and is likely to be smaller than the quantization error itself. Furthermore, if the polarity

of the reference is opposite to that of the input signal, a simple summing junction effectively replaces the difference unit. Any subsequent amplification of the error signal is free from linearity problems as only one level on each side of zero is detected by the comparator. The decoder itself is usually a network of accurate weighing resistors. One is therefore left with the stepping reference as the only unit in the converter required to maintain its accuracy over a large dynamic range.

1.4.3. Comparison with Delta Modulation.

Before studying the requirements imposed on the reference circuit, an interesting parallel can be established between the system just described and another existing type of A-D converter.

With the simple addition of a clock pulse generator, the block diagram of figure 2 would illustrate the principle of delta modulation. This appellation normally refers to a pulse code modulation technique primarily intended for the transmission of audio[29] or video[30] signals. It employs a one-digit code and therefore makes the sampling frequency equal to the clock pulse repetition rate. The method is well known and adequate descriptions may be found in the above references. For the sake of comparison, the present converter can be

regarded as a case of delta modulation with a clock rate proportional to the slope of the input signal. Apart from this important difference and its logical consequences, both systems operate in a similar fashion generating a one-digit code representation of the input signal. Furthermore, the mathematical expression for the maximum input frequency as a function of amplitude for a delta modulation system[29], is identical to the corresponding equation to be derived later for the present converter. In this case, the clock frequency must be replaced by the maximum pulse repetition rate of the reference level generator.

The absence of a fixed clock pulse frequency in the converter under study, prevents the comparison from being pursued further. Another significant difference between the two systems arises out of the distinctive ways of generating the reference signal. It will be seen later that the output from the decoder is not obtained from the integration of the output pulses as in delta modulators. In fact, with the new reference generator, problems of instability in the closed loop are practically nonexistent.

A few general remarks on analogue-to-digital conversions will now lead to the basic requirements for the reference unit.

1.4.4. Basic Requirements for the Reference Unit.

The instantaneous accuracy of a given quantization process depends on the magnitude "q" of the quantization interval. The quantization error at any point can be defined as $\pm q/2$, suggesting that the quantized signal will always lie at or within these limits from the exact value. If it is desired for some reason, to keep the quantization error to a small fraction of the full scale, the number of defined levels must be increased sufficiently. It should be remembered that good filtering is necessary in order to recover the signal if only a few levels are used. The instantaneous accuracy is of prime importance whenever the quantized signal is utilized as such with little filtering. Many analog-to-digital converters, used in conjunction with computers, must introduce negligible quantization errors. However, dividing a given dynamic range into a greater number of intervals in order to reduce the quantization error can impose severe limitations on the speed of the converter. A simple example will demonstrate the implications of this statement.

Example: Suppose that a quantizer divides a given voltage range into 1000 intervals. Theoretically, the quantization error can be as small as $\pm$ 1 part in 2000 or $\pm$ 0.05% of full scale. If a

comparison method is used, as in the present case, the number F of steps available from the reference per unit time limits the maximum voltage variation per unit time ($\Delta V/\Delta T$) acceptable at the input. The steps must be equal to the full scale amplitude divided by one thousand and the following inequality must be satisfied at all times.

$$F \times (\text{full scale amplitude})/1000 \geq \Delta V/\Delta T$$

If the maximum slope of a sinewave is expressed as πfA, where f represents the frequency and A the peak-to-peak amplitude, the maximum frequency of a full scale sinewave that the quantizer will follow can be deduced from the above inequality. A 1kc/s signal, for instance, would require the reference to operate at a speed greater or equal to $1000\ \pi f$ or $F \geq 3.14 \times 10^6$ steps/sec.

This result points out the need for a high value of F (steps/sec available from the reference), even for relatively low frequencies of the input signal, if the quantization error is to be very small. Fortunately, trading accuracy for speed and vice versa is normally possible with such a system. If the number of quantization intervals is

decreased for a fixed dynamic range, the amplitude of the steps consequently increases. Assuming that the speed F (step/sec) of the reference remains the same, the maximum slope acceptable by the quantizer is proportionally larger. The quantization theory shows that in many cases, a small number of levels is perfectly adequate as long as certain conditions are satisfied. This theoretical point will be considered in a later study of the system as a whole.

The ultimate performance of the quantizer therefore depends on the extent to which the reference staircase generator can meet the speed and precision requirements. It is now intended to enumerate the problems related to the design of this most important part of the system and to explain in detail the various steps leading to their solution.

PART I

Design of the High Speed Stepping Reference.

CHAPTER 2

Design of a Building Block.

2.1. Preliminary Remarks.

The first question to be answered at an early stage was how to define between one hundred to one thousand voltage or current levels extending on both sides of zero with the facilities to step up or down one level at a time at a speed possibly extending to ten million levels per second.

A number of methods were envisaged, making use of pulse counters, coincidence detecting circuits, integrators, etc... Most of these approaches were discarded in view of the further requirement for any one level to be kept as an accurate reference for long periods of time. It was finally decided to interconnect multistable circuits through weighing impedances to define the necessary levels. This principle has been applied in most of the existing digital voltmeters where binary circuits are combined to reproduce a given numerical code.

To obtain a large number of levels using binary circuits as the building block necessitates many of these units. As long as they are simple and inexpensive units, this solution is acceptable. In the present case however, the problem was slighly different from the example of the relatively slow digital voltmeter. The higher speed required (10 Mc/s p.r.r) would have called for expensive switching components together with careful design procedure if transistors had been used.

In the light of these remarks, the high switching speed possible with tunnel diode circuits seemed to be an interesting proposition for the reference staircase generator. Furthermore, tunnel diodes lend themselves to simple multi-stable circuits as will be shown later. Their use simplified considerably the design of the building block to be introduced in this chapter.

2.2. The Tunnel Diode.

The tunnel diode is a heavily doped semiconductor junction diode. Its characteristic shows a voltage-controlled negative resistance.

This behaviour has been explained by Esaki as being due to quantum-mechanical tunnelling of carriers through a narrow p-n junction[31]. The tunnel effect is a process wherein particles can disappear from one side of

a potential barrier and appear almost instaneously on the other side. According to the laws of quantum theory, the space charge depletion region of a p-n juntion must be made extremely thin before the probability of tunnelling becomes significant.

A simple way of explaining qualitatively the generation of the tunnel current in a diode is to consider the effect on the characteristic of a p-n junction, of increasing the concentration of the free carriers in the semiconductor crystal. A direct consequence would be to decrease the breakdown voltage of the junction in the reverse direction. The extent to which the breakdown voltage can be reduced, is limited by the solubility of the impurities determining the carrier concentration. For many semiconductor materials, this limit is greater than what is needed to reduce the breakdown voltage to zero. In these cases, the junction can still be in the reverse breakdown condition at a slight forward bias. Application of a larger forward voltage would bring the junction out of the breakdown condition and the current would fall to a smaller value. The junction would finally behave in a similar fashion as a normal diode taking into account the difference in construction.

Qualitative physical description of the tunnel diode junction in terms of electron energy band theory,

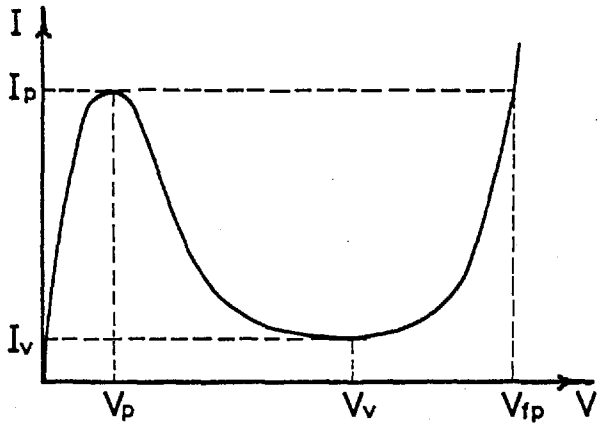
can be found in the literature[32] and will not be included here. References 31-33 and 34 present a more rigorous analysis of the tunnel diode junction. These theoretical derivations will not be unnecessarily reproduced here and the device will now be investigated as a circuit element.

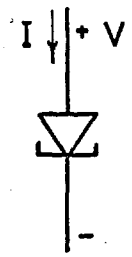
2.2.1. The Tunnel Diode as a Circuit Element.

Figure 3 shows the static characteristic of a tunnel diode. This I vs V curve is voltage controlled and is made up of two positive resistance regions separated by one negative slope. It is worth noting that the characteristic of figure 3 has been obtained from accurate measurements taken on a 1N2941 tunnel diode. All subsequent figures representing the tunnel diode curve or its linear approximation, have been derived equally from these results. Whenever possible, the same scales have been preserved on the co-ordinates in order to permit direct comparison between the figures of different sections. The curve of figure 3 can be described by the following points:

I_p = peak point current, the maximum tunnel diode current to the left of the negative resistance region.

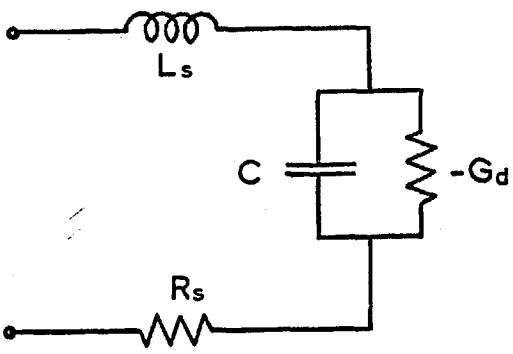
V_p = peak point voltage, the voltage across the diode when $I = I_p$, to the left of the negative resistance region.





Symbol

Fig. 3.



SMALL SIGNAL EQUIVALENT CIRCUIT FOR NEGATIVE REGION

Fig. 4.

I_v = valley point current, the minimum diode current to the right of the negative resistance region.

V_v = valley point voltage, the voltage at which $I = I_v$ to the right of the negative resistance region.

V_{fp} = forward peak point voltage, the voltage across the diode for $I = I_p$ in the high voltage region (to the right of V_v).

The peak point current, I_p, is controlled by an etching process and can be held to within ±2.5% or better on a production basis[32 (page 12)]. Tunnel diodes can be made with peak currents anywhere from a few microamps to several amperes. When the peak current is less than about 50 μA, the device is often called a "backward diode" and is used in the reverse direction as a rectifier in conjunction with tunnel diode circuits because of its low voltage drop.

The peak point voltage, V_p, the valley point voltage, V_v, and the forward peak point voltage, V_{fp}, are fixed to a certain extent by the semiconductor material. Table I compares between typical voltages obtained with germanium, silicon and gallium arsenide tunnel diodes.

Material	V_p mv	V_v mv	V_{fp} mv
Ge	55	350	500
Si	75	450	750
GaAs	150	500	1200

TABLE I

The higher voltages obtainable with GaAs combined with a possibly greater I_p/I_v ratio, seems to suggest the choice of this material as being more advantageous. At the present, however, germanium diodes are generally cheaper and are available from a large number of firms. This situation is due mainly to special difficulties encountered in the production of reliable GaAs tunnel diodes.

It appears from the previous description of the tunnel diode characteristic, that the slopes in the three regions are directly related to the magnitude of the peak current I_p. The negative resistance in particular is nearly inversely proportional to I_p, imposing certain limitations on the design of tunnel diode oscillators and amplifiers[32-33]. A useful linear approximation of the negative resistance can be computed as 0.4 times the resistance joining the peak point, (I_p, V_p), to the valley point, (I_v, V_v).

Before analysing the switching action of a tunnel diode, one more question is worth answering. What parameters will limit the speed of a tunnel diode as a circuit element? The tunnel effect is responsible for the generation of the negative resistance. This basic conduction mechanism has a theoretical frequency limit of the order of 10^7 megacycles per second. This figure cannot fail to strike the imagination of circuit designers familiar with the many times slower mechanisms of drift or diffusion involved in conventional diodes and transistors. However, the equivalent circuit of the tunnel diode operating in the negative resistance region (fig. 4.), can be used to demonstrate the drastic effect of some parameters on the frequency response of the practical device.

In this diagram, R_s represents the total series resistance determined mainly by the bulk of the semiconductor material. The inductance, L_s, is limited by the minimum inductance of the leads or the package. The capacitance, C, is the summation of the capacitance of the junction and the capacity introduced by the package and the leads. Finally, $-g_d$ is the slope of the characteristic at the particular bias point under consideration and can be assumed independent of frequencies.

If the impedance of the tunnel diode in the negative region is computed from the equivalent circuit,

two significant cut off frequencies can be derived. One is the resistive cut off frequency, f_{ro}, and is defined as the frequency at which the real part of the tunnel diode impedance goes to zero. The device will not amplify above this frequency. The second point of interest is the self-resonant frequency, f_{xo}, and it occurs when the imaginary part of the diode impedance goes to zero. No oscillation can be sustained above this frequency. Expressions for f_{ro} and f_{xo} are easily derived[32] (page 14).

$$f_{ro} = \frac{|g_d|}{2\pi C}\sqrt{\frac{1}{R_s|g_d|} - 1} \qquad .. (1)$$

$$f_{xo} = \frac{1}{2\pi}\sqrt{\frac{1}{L_s C} - \left(\frac{g_d}{C}\right)^2} \qquad .. (2)$$

For a typical 1N2941 germanium tunnel diode in a TO-18 package, manufactured by General Electric, the relevant parameters given in the data sheet are as follows: C = 15 to 50 pf; L_s = 6 to 19 x 10^{-9} henries and $|-g_d|$ = 0.03 mhos. In this case, with the minimum values of C and L_s, f_{ro} = 2.58 KMc/s and f_{xo} = 420.3 Mc/s.

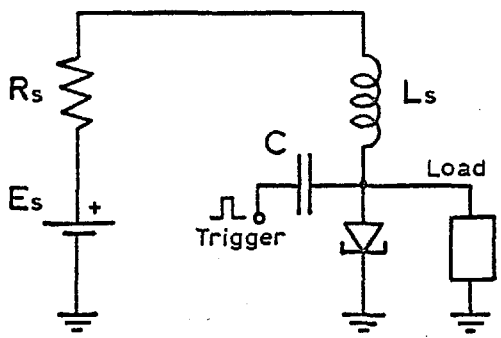
In practice, the cut off frequencies are circuit dependent and may be considerably smaller unless great care is taken to keep the inductance of the leads and the external parallel capacitance to a minimum. It should

therefore be remembered that operation above a few hundred megacycles is not always possible with all tunnel diodes. On the other hand, it can be said that most tunnel diodes are fast enough to be used advantageously in circuits operating at frequencies up to some twenty to fifty megacycles per second without any special difficulties. It will be seen later on that switching from one side of the negative resistance region to the other side can readily be effected in less than 10 nanoseconds with a 1N2941 tunnel diode loaded by a transistor.

2.2.2. Basic Circuit.

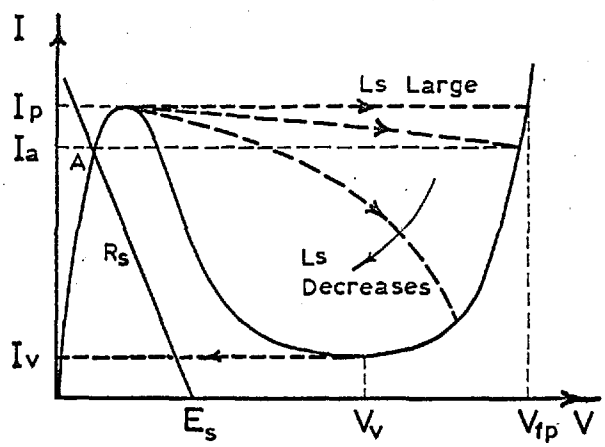
A study of the simple tunnel diode circuit of figure 5, will provide enough information for the design of all subsequent circuits required by the staircase generator.

This basic circuit consists of a voltage source, E_s, in series with a resistance, R_s, an inductance, L_s, and the tunnel diode itself. It is assumed for the moment that the parallel load can be neglected. Figure 6 represents the static characteristic of the tunnel diode with possible values of the supply voltage, E_s, and of the series resistance, R_s, drawn as a load line. Reference to figure 6 is sufficient to establish the remarkable flexibility of this circuit. Suppose, for instance, that the tunnel diode is initially biased at point A and that



BASIC CIRCUIT

Fig. 5.



SWITCHING CHARACTERISTIC

Fig. 6.

a trigger signal increases the current above the peak, I_p. Provided that certain conditions are satisfied, switching occurs in a manner illustrated by the trajectories of figure 6, depending on the magnitude of the inductance, L_s. Adjustment of the bias voltage, E_s, and of the series resistance, R_s, (and of the inductance, L_s, in certain cases) would suffice to transform the circuit into an astable, a monostable or a bistable unit. It can therefore become a sinewave oscillator, a monostable trigger circuit, a bistable flip flop, a level detector, etc.. The analyses for the cases of the sinewave oscillator and of the amplifier can be based on the equivalent circuit of figure 4 and are derived in chapters 3 and 4 of reference 32.

However, the present work is concerned entirely with the tunnel diode as a switching element. It is now intended to consider in detail the switching action of a tunnel diode in order to acquire a better understanding of all the switching circuits based on the diagram of figure 5 and to define their operating conditions. This study will be carried out as part of a general description of the tunnel diode chain.

2.3. The Tunnel Diode Chain.

If a chain of tunnel diodes is connected to a constant current source as illustrated in figure 7, a

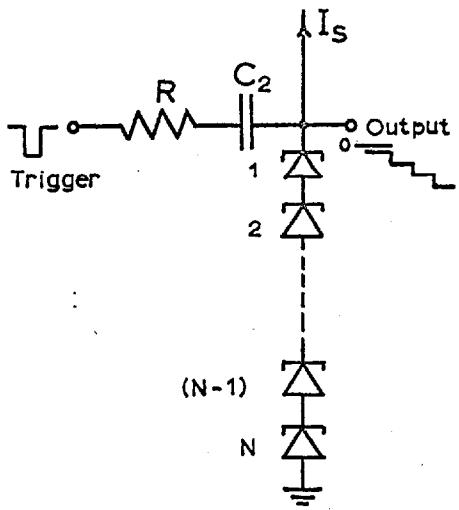


Fig. 7.

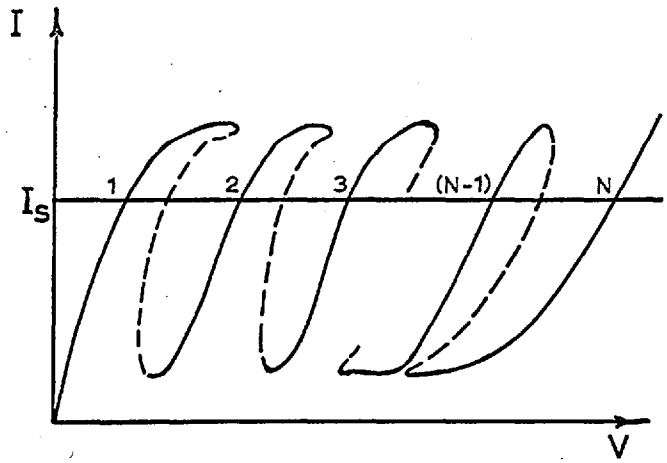


Fig. 8.

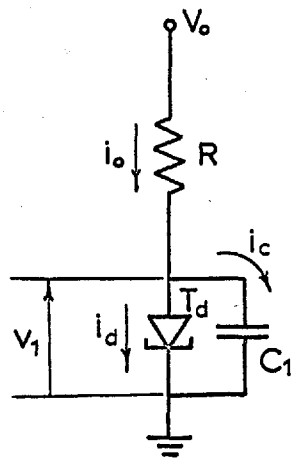


Fig. 9.

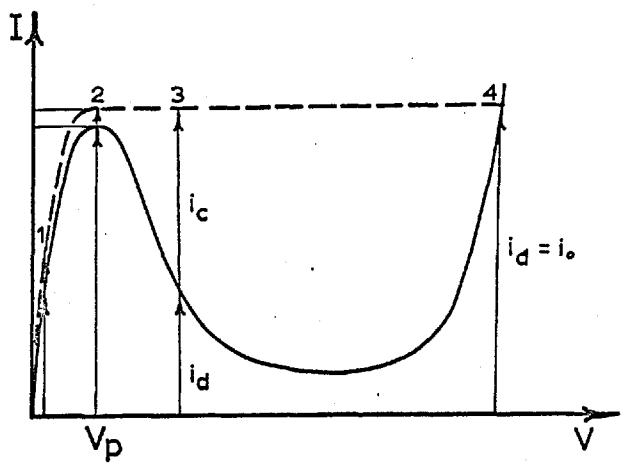


Fig. 10.

multistable circuit is obtained. The over-all static characteristic of the chain is shown in figure 8, assuming that all tunnel diodes are identical. The standing current, I_s, is adjusted to a value below the minimum peak current, I_p, in the chain and all the diodes are initially in their low voltage state. If a series of pulses switches the diodes one at a time to their high voltage state, a staircase voltage waveform is generated at the output.

It can be shown experimentally that, for a given range of input pulse amplitudes, only one tunnel diode can be triggered at a time. It is now proposed to establish the conditions to be met both by the tunnel diodes in the chain and by the trigger pulses for this situation to prevail. To do so, the behaviour of a single tunnel diode operated from a current source and then from a voltage source will first be analysed qualitatively. The switching of two tunnel diodes in series will then be studied. Finally, equations will be derived giving the limits of acceptable trigger pulse amplitudes for a series of N diodes biased from a constant current source.

2.3.1. Switching of a Single Tunnel Diode.

In the circuit of figure 9, i_d represents the current flowing through the ideal tunnel diode, T_d, at any instant. The voltage v_1 across the diode is given by

the static characteristic of the device at a point corresponding to a current, i_d. The capacitor, C, represents the total capacitance appearing across the diode and i_c is the instantaneous current taken by that capacitance.

2.3.1.1. Current Drive.

In the case of a current drive, the resistance, R, is made arbitrarily large. Assume that the voltage, V_o, is initially standing at zero and starts increasing positively. The input current, i_o, also increases from zero and is divided between i_d and i_c in a manner illustrated by figure 10. The following equalities must be satisfied at all times.

$$i_o = i_d + i_c \qquad .. (3)$$

$$\Delta i_o = \Delta i_d + \Delta i_c \qquad .. (4)$$

Equation (4) expresses the fact that any change in i_o per unit time must be reflected as corresponding variations of i_d and i_c.

Referring to figure 10, the complete transition from point zero to point 4 can be described as follows. For the first part of the characteristic to the left of the peak, the magnitude of the capacitor current, i_c, depends on the rate of rise of V_o and is kept small by the shunting effect of the low dynamic resistance of the

tunnel diode in that region. As the peak is approached, the diode begins to look like a very large impedance and any further increase in the current, i_o, is taken almost entirely by the capacitor, C, i.e. the voltage, v_1, starts increasing faster for a given rate of rise of i_o. The presence of the charging current, i_c, causes the voltage, v_1, across the capacitor, C, to exceed the peak point voltage, V_p, producing a decrease of the tunnel diode current, i_d. From that moment on, the negative resistance initiates a regenerative action and no additional increase in i_o is needed to ensure complete switching of the tunnel diode to the high voltage state. Suppose, for instance, that the input current, i_o, is maintained constant, ($\Delta i_o = 0$), as soon as the peak point is passed. From Eq. (4), $\Delta i_c = - \Delta i_d$ and, as the tunnel diode current is decreasing, Δi_d is negative, giving a positive value for Δi_c. The increasing capacitor current causes the voltage, v_1, to become still larger, producing further decrease of the diode current, i_d. After the valley point, (V_v, I_v), is passed, the diode impedance becomes positive again and the increase of v_1 produces an increase in the current, i_d, which in turn asks for an equivalent reduction of i_c, slowing down the rate of change of v_1. Switching is completed when the capacitor current, i_c, has been reduced to zero and the diode current, i_d, is equal to the input current, i_o.

The same argument holds in the general case when the input current, i_o, is not kept constant during the switching action of the diode. If i_o increases much above the peak current, I_p, the available capacitor current is larger and the switching time becomes shorter. In the case of a significant reduction of i_c taking place during the switching, it is only necessary for i_c not to fall to zero until the valley point is passed. The final value of i_c must obviously be greater than the valley current, I_v, if the tunnel diode is to remain in the high voltage state at the end of the switching process.

In practice, the tunnel diode would be biased from a constant current source, I_s, and an additional current pulse would bring the operating point above the peak. In this case, the triggering pulse must not be removed before the tunnel diode current has fallen to a value below the standing current, I_s, otherwise, the capacitor current would be reduced to zero at a point on the negative resistance and the diode would return to the low voltage state.

2.3.1.2. Voltage Drive.

The circuit of figure 9 can also be used to describe the switching of a single tunnel diode driven from a low impedance source. In this case, the resistance, R, is very small and it is important to emphasize the fact

that it represents the total dynamic as well as static impedance in series with the diode. In other words, any inductive effect must be minimized such that the impedance, R, remains the same even during the very fast switching transients.

Two different conditions may prevail when the voltage, V_o, is increased from zero depending on whether the resistance, R, is smaller or greater than the negative resistance, $|-R_d|$, of the tunnel diode.

In the circuit of figure 9, the resistance, R, is effectively in parallel with the tunnel diode. This fact becomes self-evident if the voltage source, V_o, in series with the resistance, R, is replaced by its equivalent current source, V_o/R, in parallel with R. If the resistance, R, is smaller than $|-R_d|$, their parallel combination can never present a negative resistance to the current source, V_o/R, and no regeneration can take place. The circuit is therefore stable at all points and the tunnel diode can be said to possess a voltage-stable characteristic. The behaviour of the tunnel diode under these conditions is illustrated by figure 11, when the voltage, V_o, is increased from zero to a value, V_{o3}. The exact trajectory depends on the timing of the transition of the voltage from zero to V_{o3} but a possible example is given by the dotted line 0-1-2 and 3. It should be

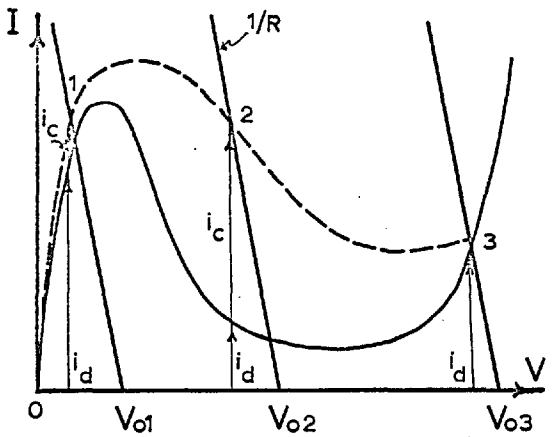


Fig. 11.

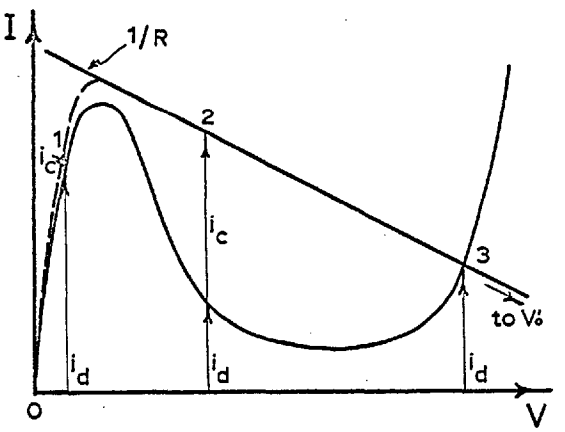


Fig. 12.

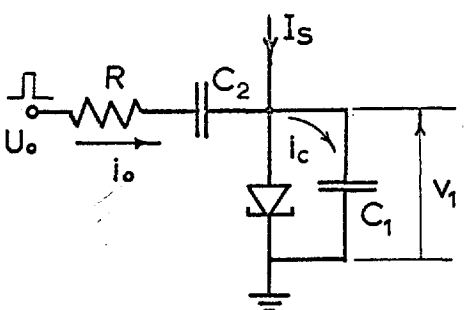


Fig. 13.

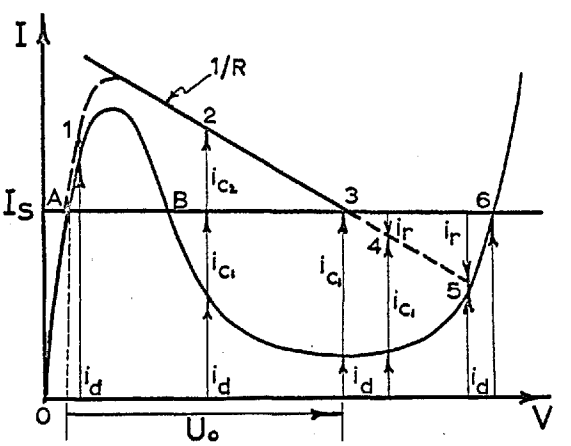


Fig. 14.

remembered that V_o may be stopped anywhere such that the resistance, R, intersects the diode characteristic at any point and the circuit would remain stable. No switching can occur as long as R is smaller than $|-R_d|$.

If on the other hand, the resistance, R, is made greater than $|-R_d|$, the switching action is similar to the case of current drive already explained. Figure 12 shows the trajectory, 0-1-2-3, followed by the input current, i_o, when the voltage, V_o, is increased from zero to a final value, V_o'. It is seen that the current, i_o, is divided between the tunnel diode and the parallel capacitance in exactly the same way as in the case of current drive. The same equations (3) and (4) are valid and the description of the switching process need not be repeated.

2.3.1.3. Practical Case.

In practice, the tunnel diode is biased with a standing current, I_s, as in figure 13. The current, I_s, can be obtained from a voltage source in series with a large resistance or from a smaller resistance in series with an inductance providing a large dynamic impedance for faster switching. Assume that a voltage pulse is fed through a resistance, R, connected to the diode via a capacitor, C_2. The tunnel diode is initially resting at

point A (figure 14.). For complete switching to occur from the low voltage to the high voltage state, the trigger pulse must be large enough to increase the voltage across the diode from point A to point B. As soon as point B is reached, the standing current, I_s, continues to charge up the capacitances, C_1 and C_2, until switching is completed, regardless of the magnitude of the resistance, R. It is assumed for the moment that the duration of the input pulse is longer than the switching time. Point 6 in figure 14 is therefore the new operating point by the time the trailing edge of the triggering pulse applies a signal of the reverse polarity across the diode. Whether the tunnel diode resets to the low voltage state or not at that moment depends on the magnitude of I_s relative to the valley current, I_v, and on the amplitude of the input pulse. If a diode gate is employed at the input, the effect of the trailing edge may be controlled independently of these factors and the pulse may be removed immediately after point B is passed without fear of resetting the diode.

The minimum amplitude of the trigger pulse, $\underline{U_o}$, to ensure reliable switching depends on the magnitude of the resistance, R. If R is smaller than the negative resistance, $|-R_d|$, $\underline{U_o} \geq V_B - V_A$ must be satisfied. The trajectory from point A to point B depends on the rise time of U_o and can be deduced as was done for the corresponding

theoretical case (see figure 11.). The presence of I_s in this region of the curve merely acts as a constant term and does not influence the transition from A to B.

The situation met when R is greater than $|-R_d|$, is not significantly different. However, it lends itself to a clear graphical representation, as shown in figure 14, and will be used to explain the influence of the resistance, R, and of the capacitor, C_2, on the switching process. In this case, the minimum input pulse amplitude is given by $\underline{U_o} \geq V_p - V_A + R(I_p - I_s)$. Suppose an input pulse $U_o = V_3 - V_A$ is fed into the circuit. The transition from A to point 6 in figure 14 takes place as follows. It is assumed for the moment that the input pulse width is much longer than the complete switching transient. Until point B is reached, the capacitor charging current, i_c, and the part of the tunnel diode current lying above I_s, are supplied entirely by the trigger pulse. From point B to point 3, the standing current, I_s, supplies the tunnel diode current, i_d, and part i_{c1} of the charging current, i_c. By the time point 3 is reached, the trigger current, i_o, has been reduced to zero by an increase in the voltage, v_1, equal to U_o and both i_c and i_d are due entirely to I_s. The further increase of v_1 due to the current, i_c, produces a reverse current, i_r, to flow across the resistance, R, until point 5 is reached. The charge building up across the coupling capacitor, C_2,

gradually decreases the current, i_r, shifting the operation towards point 6, the final quiescent condition. This effect can be illustrated graphically if it is noted that the voltage appearing across C_2 is in series with U_o, and is effectively moving point 3 towards point 6 along the I_s line until the dotted part of the load line, 1/R, intersects the diode characteristic at point 6. Another approach is to consider the reduction of i_r to be due to an increase of the effective driving impedance as seen by the diode. The graphical representation would then be a rotation of the dotted part of the load line about point 3 until point 5 coincides with point 6. The effect of the removal of the input pulse has been explained above and is of no concern here as diode gates are normally introduced at the input. The time needed for the operating point to move from 5 to 6 depends mainly on the time constant $(R + R_{d2})C_2$.

The switching of a single tunnel diode has been thoroughly investigated thus far for the cases of current and of voltage drive. The results will now be utilized to study the behaviour of a series of two tunnel diodes under similar conditions.

2.3.2. Switching of a Series of Two Tunnel Diodes.

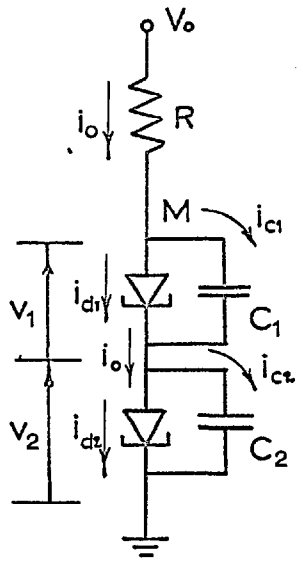
The switching of a series of two tunnel diodes

will be investigated using the same approach as above. True current drive of the pair will be explained at first. The next case, the low impedance drive, will then be subdivided in two parts depending on whether the peak currents, I_{p1} and I_{p2}, are equal or different. Finally, the standing current will be introduced in order to elucidate the practical implications of the results.

2.3.2.1. Current Drive of the Tunnel Diode Pair.

Suppose that in the circuit of figure 15, the two diodes differ only by a slight change in their peak currents such that $I_{p1} < I_{p2}$. The total static characteristic seen at point M is given in figure 16. If the resistance, R, is very large and V_o is increased slowly from zero, a current, i_o, starts to flow. As soon as i_o becomes greater than I_{p1}, the first diode switches to the high voltage state, quite independently of the presence of the second diode. The switching takes place at constant current because i_o is defined by a large resistance, R. The second diode does not switch until $i_o \geq I_{p2}$.

In this case of true current drive, the interaction between the two diodes is nil because the driving current, i_o, is not influenced by the changes in either v_1 or v_2. This is to say that if the peak currents were



THE TUNNEL DIODE PAIR

Fig. 15.

COMBINED STATIC CHARACTERISTIC

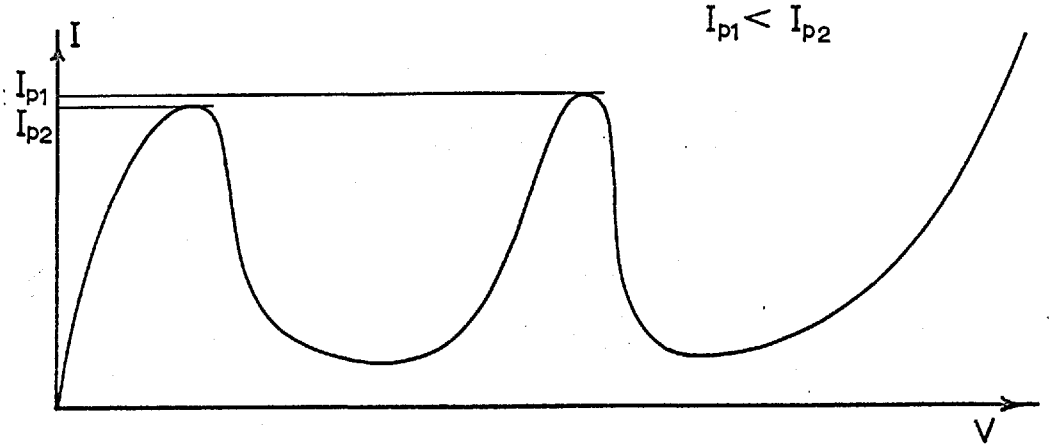


Fig. 16.

identical, the two diodes would always switch together to their high voltage state.

Therefore, this driving mode relies on a difference between the peak currents in order to achieve sequential triggering of the diodes. In practice a driving current ramp could be used and the switching of the first diode could be detected as a rapid voltage change at point M by an auxiliary circuit which could stop the drive before the next peak is reached. This method necessitates the operation of the control circuit every time a tunnel diode is switched and over-all speed may be seriously impaired.

2.3.2.2. Voltage Drive of the Tunnel Diode Pair.

If the resistance, R, in the circuit of figure 15, is given a very low value, and the voltage, V_o, is increased from zero, the behaviour of the tunnel diodes depends on whether their peak currents are equal or not. Regardless of the prevailing conditions, the following equations must be satisfied at all times.

$$i_o = i_{c1} + i_{d1} = i_{c2} + i_{d2} \quad .. (5)$$

$$V_o = Ri_o + v_1 + v_2 \quad .. (6)$$

2.3.2.2.1. Different Peak Currents $I_{p1} < I_{p2}$.

If I_{p1} is smaller than I_{p2}, the first tunnel diode passes its peak point before the other one. Assume at first that the resistance, R, is smaller than $|-R_d|$, the negative resistance of one tunnel diode. For the same reasons as those given for a single diode, no regeneration can occur and a voltage-stable characteristic displaying two peaks (as in figure 16) could be plotted point by point by slowly increasing V_o over a sufficient range.

Suppose on the other hand, that the resistance, R, is larger than $|-R_d|$, such that switching can occur. In this case, the first tunnel diode would switch to the high voltage state in a manner similar to that illustrated in figure 12 and already explained for a single diode. The presence of the second diode in its low voltage state can be regarded as a mere increase of the resistance, R, by an amount equal to R_{d1}. Further increase of V_o would then bring the operating point above I_{p2} and the second diode would switch in exactly the same way. Graphical representation of this case can be seen in figure 17. In order to ensure that the second peak is not passed before the switching of the first diode is completed, the rate of rise of V_o during that time must not be greater than that of v_1 across the switching diode. In fact, it can be

THE TUNNEL DIODE PAIR

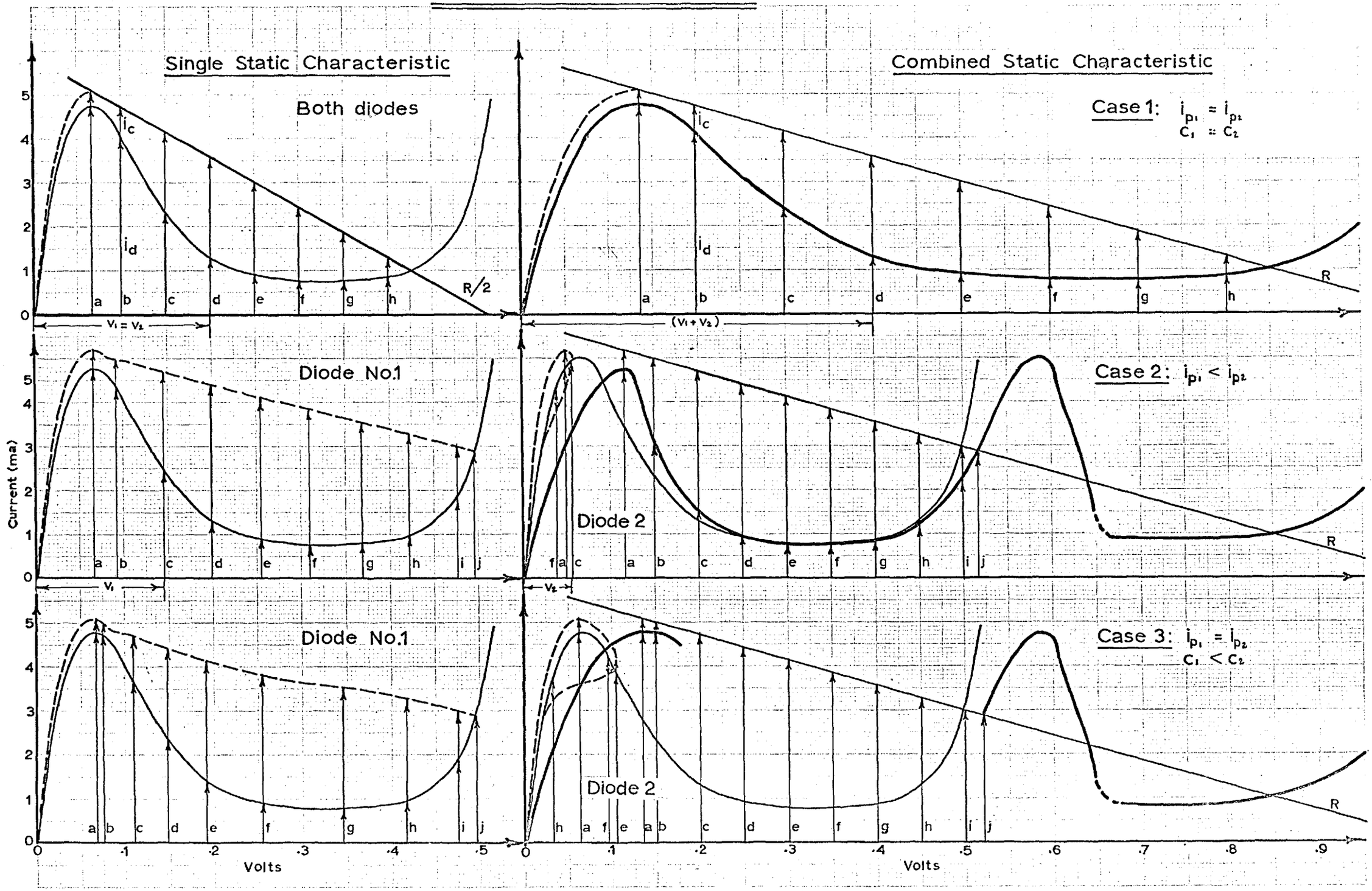


Fig. 17.

seen from Eq. (6), that as long as v_1 is increasing as fast or faster than V_o while v_2 is not changing appreciably, the current i_o must remain constant or decrease. This limitation imposed on the rise time of the driving signal will be used to great advantage later on in order to ease the tolerance requirements on the amplitude of the trigger pulses fed to long chains of tunnel diodes.

2.3.2.2.2. Identical Peak Currents $I_{p1} = I_{p2}$.

One important question has remained unanswered so far. Is it possible to use tunnel diodes with identical peak currents and still trigger them one at a time?

It has been shown earlier that, for a current drive, the answer would be no. However, provided certain conditions are satisfied in a low impedance circuit, two tunnel diodes, as in figure 15 for instance, can pass their peaks simultaneously and during the regeneration that follows, one of them can return to the low voltage stage while the other one completes its switching. In order to explain this operation, the circuit of figure 15 can be assumed to contain two identical tunnel diodes except for a slight difference in their parallel capacitances $C_1 < C_2$. The resistance, R, is larger than $|-R_d|$ by a small amount and V_o increases slowly. As soon as the peak currents

are passed, both diodes begin to switch and $v_1 + v_2$ increases rapidly. At first, the conditions of both diodes are identical and $i_{c1} = i_{c2}$. However, C_1 is smaller than C_2 and the voltage v_1 increases faster than v_2. Consequently, the current, i_{d1}, decreases more rapidly than the current, i_{d2}, for identical negative resistances. It follows from equation (5), that i_{c1} is getting larger than i_{c2} favouring some further advance of the voltage, v_1, on v_2. This regenerative action has been described before and will not be repeated. Meanwhile, assuming that V_o changes very little during the switching time of a tunnel diode, the current i_o is decreasing as equation (6) must be satisfied at all times. Because the voltage, v_2, is not changing as rapidly as v_1, it is possible that the reduction of i_{d2} may not be sufficient to account for the lowering of i_o and the capacitor current, i_{c2}, starts to decrease. For small values of the resistance, R, this action may be rapid enough for i_{c2} to become zero at a point on the negative resistance of the second diode. At that moment, i_{c1} is still greater than zero ($i_{c1} > i_{c2}$) and the voltage, v_1, is increasing. The first diode is then getting closer to the valley point and therefore entering a region of very large negative resistance. It means that even a small decrease of the current, i_{d1}, (or of i_o, because of the very large

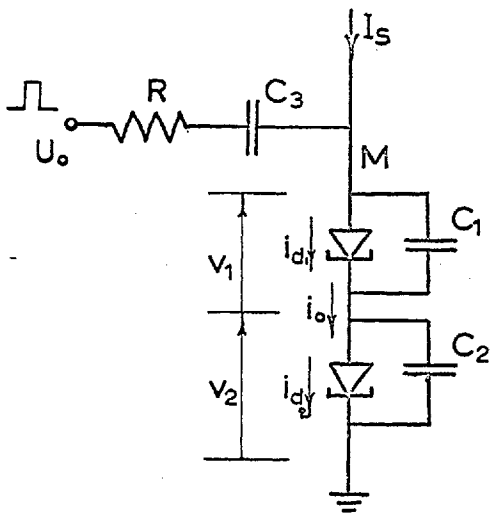
negative resistance in parallel with C_1) would cause a large increase of the voltage, v_1. It can be seen that, for equation (6) to be satisfied under these conditions, the changes in the voltage, v_2, must be negative. A current, i'_{c2}, begins to discharge the capacitor, C_2, in order to reduce v_2 while the voltage, v_1, continues to increase. The action is again regenerative and the first diode completes its switching while the second one resumes its low voltage state. Figure 17 gives a graphical representation of this case.

The experience gained during the theoretical study of the tunnel diode pair, will now prove valuable in establishing the operating conditions of the practical circuit of figure 18.

2.3.2.3. Practical Cases.

2.3.2.3.1. Different Peak Currents.

The description already given for the case of two different peak currents, $I_{p1} < I_{p2}$, is still perfectly valid. Owing to the presence of the current, I_s, the trigger pulse needs to shift the operating point only from A to B, (figure 19.), and one diode switches while the other one remains below its peak. The switching action is very similar to that illustrated by figure 14. for a single unit except that the small nonlinear resistance



TUNNEL DIODE PAIR

(practical case)

Fig. 18.

COMBINED STATIC CHARACTERISTIC

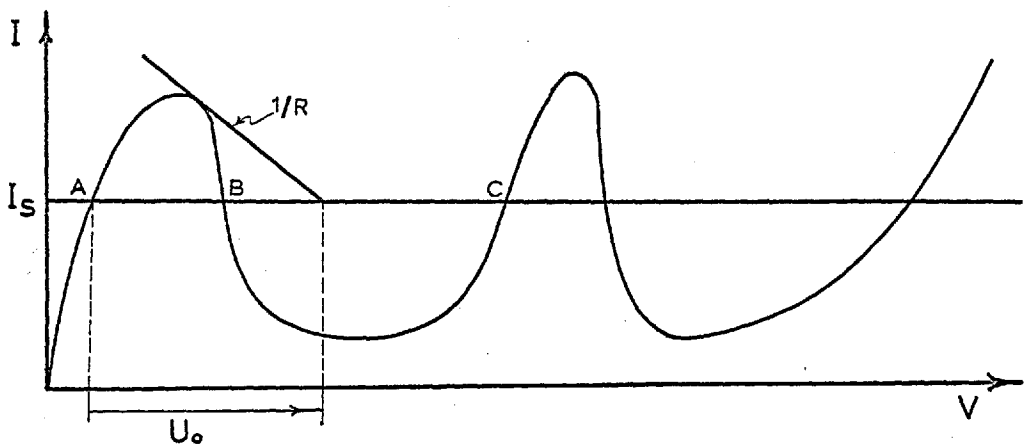


Fig. 19.

introduced by the second diode alters slightly the shape of the characteristic. The minimum trigger pulse amplitude is given approximately by $\underline{U_o} \geqq 2V_p - V_A + (I_p - I_s)R$ directly from figure 19. Provided that the rate of rise of the leading edge of the input signal is slower than the switching speed of a tunnel diode, the amplitude, U_o, may be larger than the minimum, $\underline{U_o}$, by as much as the full voltage step generated by the first diode, before the two units can be switched together. If the risetime of U_o is shorter than this limit, it was shown earlier that the input current, i_o, is still increasing after the first diode has passed its peak and the second diode may be triggered with the same pulse unless the difference between the peaks is widened. The tolerance requirements on U_o become correspondingly more stringent and unless the extra speed is essential, this condition should be avoided. The 1N2941 tunnel diode can switch over in less than 10 nsec and this time is more than adequate for the present needs. The minimum amplitude, $\underline{U_o}$, of input pulses, is proportional to the magnitude of the resistance, R. It has just been pointed out that the voltage range of acceptable trigger pulse amplitudes is a fixed value equal to the step generated across one tunnel diode. The resistance, R, should therefore be kept small in order to ease the tolerance required on U_o.

2.3.2.3.2. Equal Peak Currents.

The introduction of a standing current, I_s, was shown not to modify seriously the basic operation of the tunnel diode pair from that of the theoretical case as long as the peak currents were different. On the other hand, when the peaks are identical, such that both tunnel diodes can start switching together, the presence of I_s has a great significance. In effect, one of the diodes can return to the low voltage state only if its capacitor current is reduced to zero when the diode current is still above the intersection of the current level, I_s, with the corresponding negative resistance. The limit has been shifted from the valley point to point B which lies much closer to the peak (see figure 19.).

It will be remembered how the interaction between the diodes was shown to engender the return of one of them to the low voltage state. The reduction of the capacitor current, i_{c2}, to zero was a consequence of a sufficiently large discrepancy betwen the magnitudes of the negative resistances of the diodes which itself was caused by the disparity of their switching speeds. In the present context, it means that the faster diode must approach the valley region before the other one has reached point B. Therefore, the high frequency performance of the two units must differ considerably.

In a chain containing more than two tunnel diodes, the situation becomes even worse. At any moment, the diodes not being switched contribute an additional resistance in series with the external R and if two units trigger at the same time, the drive being no longer of the low impedance type, both diodes reach their high voltage state.

As a result of the above investigations, a list can be made of the requirements to be satisfied by a series of two or more tunnel diodes and by the driving signal in order to achieve reliable sequential triggering of the diodes in the chain.

1. All peak currents are slightly different from one another.
2. The driving signal is generated from a low impedance circuit if possible.
3. The rate of rise of the input signal is limited such that it never exceeds the rate of change of the voltage across a tunnel diode switching in the chain.
4. Finally, the input voltage pulse amplitudes are maintained within the acceptable range.

The practical implications of some of these items will be considered during the following analysis of a chain containing N tunnel diodes.

2.3.3. Switching of a Series of N Tunnel Diodes.

The triggering of the tunnel diodes in a long chain, as shown in figure 7, can be achieved either with a current or a voltage drive. It is now intended to derive simple equations establishing the limits of input pulse amplitudes for which only one tunnel diode will switch at a time.

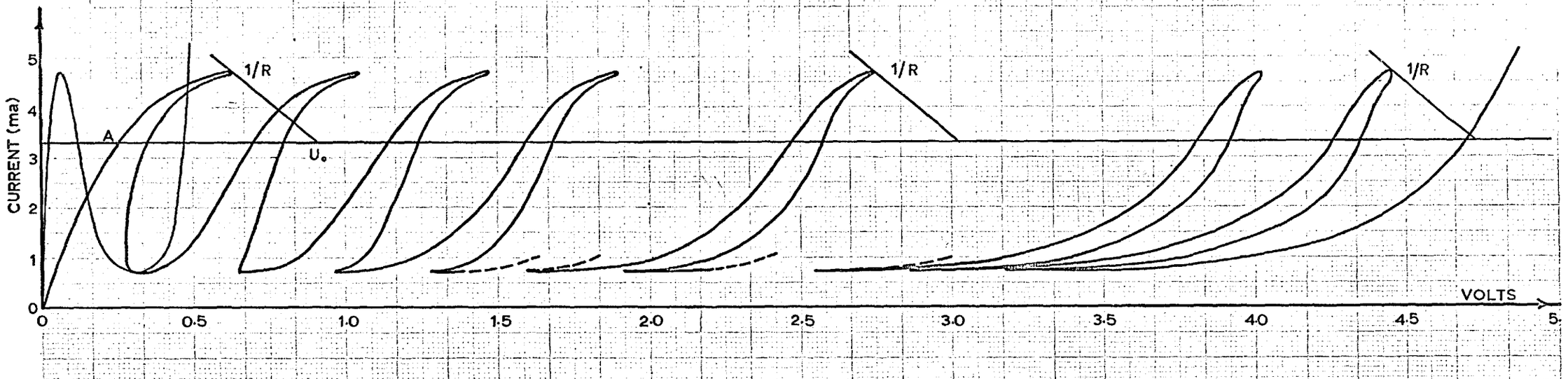
It has been explained in section 2.3.2., how the case of true current drive relied upon the control of a current ramp and necessitated a rather large increment from one peak current to the next. That method was rejected for the present application in favour of a low impedance drive which is simpler to use at high pulse repetition rates and requires fewer components. A solution will therefore be sought only for circuits meeting the conditions listed at the end of section 2.3.2. The description of the switching process needs not be repeated as it is similar to the explanation given for the tunnel diode pair.

2.3.4. Static Characteristic of the Chain.

If it were possible to plot point by point the over-all characteristic of a long chain of tunnel diodes, a curve of the type shown at the top of figure 20 would be obtained. This theoretical representation results from the series combination of ten perfectly identical

THE TUNNEL DIODE CHAIN

STATIC CHARACTERISTIC OF A 10-TUNNEL DIODE CHAIN



LINEAR APPROXIMATION OF THE ABOVE CHARACTERISTIC

Note: The peak point voltages are not defined in the same way.

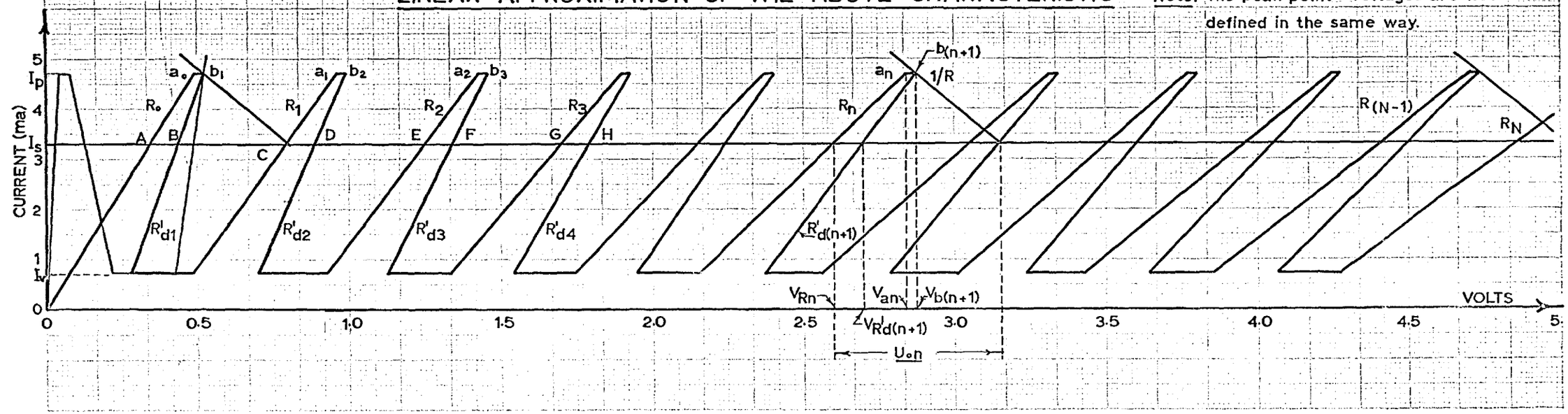


Fig. 20.

tunnel diodes. In order to plot this curve, it was assumed that all the units still in the low voltage state reached their peak points simultaneously but only one of them entered the negative resistance region at a time while all others returned below V_p as the current was decreased again. In practice, instability would occur every time one diode would cross the negative region and part of the static curve could not be displayed during the rapid switching of that unit.

This graph is however of considerable interest as it gives some insight into the actual behaviour of the chain. It can be seen for instance, that in the presence of a standing current, I_s, and for the conditions illustrated by figure 20, it would take more energy from the input pulses to switch the first diode than to drive the last one. This observation is valid only because all diodes were assumed to shift exactly to their peak points before one of them could switch. In fact, the selection of slightly different peak currents to ensure sequential operation keeps all diodes from reaching their peak voltage, V_p, until their turn comes for switching when i_o is increased above their actual I_p. This more realistic situation obviously reduces the voltage drive requirements for the triggering of the first diodes in the chain. The difference between the minimum triggering energies for

the first and the last units is consequently smaller and can even become positive. It was found in practice that the external capacitances put in parallel with the lower part of the chain in order to decrease the effective driving impedance add to the effect just mentioned and the last diodes are slightly more difficult to trigger than the first ones. Under the existing conditions, however, the range of acceptable input pulse amplitudes is not seriously narrowed by this effect.

A linearized version of the chain static characteristic can be obtained if the approximate curve, shown in figure 67 of Appendix A.1, is used instead of the exact one for every diode. The result is given at the bottom part of figure 20 and should be compared to the curve at the top of the same figure. It is seen that the approximate curve does not make the assumption that all V_p's are reached but uses a more realistic approach where one diode gets to 1.25 V_p while all the others still in the low voltage state are standing at 0.75 V_p. A number of equations can be written down directly in order to describe the linear characteristic of figure 20. The dynamic resistances, R_n, to the left of every peak can be expressed by equation (7).

$$R_n = (N - n)R_{d1} + nR_{d2} \quad .. (7)$$

where N = total number of tunnel diodes in the chain.

n = number of tunnel diodes already in their high voltage state. Can take values 0,1,2..N.

R_{d1} = linear approximation of the dynamic resistance of a tunnel diode in the low voltage state (given by equation (A.1)).

R_{d2} = linear approximation of the dynamic resistance of a tunnel diode in the high voltage state (given by equation (A.3)).

R_n = linear approximation of the dynamic resistance to the left of every peak in characteristic of figure 20.

Similarly, equation (8) gives the magnitude of the net dynamic resistance, $R'_{d(n+1)}$, presented by the chain when one diode is in the negative region.

$$R'_{d(n+1)} = -R_d + (N - n - 1)\,R_{d1} + nR_{d2} \quad .. (8)$$

where n = 0,1,2,...(N - 1)

R_d = magnitude of the approximate negative resistance of a tunnel diode.

This last concept of a resistance, $R'_{d(n+1)}$, is only useful in drawing the bottom curve of figure 20. It is

not needed in the following calculations.

The various voltage points terminating the above resistances at the peak current level, I_p, are given by equations (9) and (10).

$$V_{an} = 0.75V_p\,(N - n) + nV_{fp} \qquad \text{for } n = 0,1,2..N \qquad .. (9)$$

$$V_{b(n+1)} = V_{an} + 0.5V_p$$

$$V_{b(n+1)} = V_p\left[0.75(N - n) + 0.5\right] + nV_{fp} \qquad \text{for } n = 0,1,2..(N - 1) \qquad .. (10)$$

where V_{an} = voltages appearing at the top of the resistances, R_n, for $I = I_p$.

or voltages at the left extremity of every horizontal portion of the characteristic when $I = I_p$.

$V_{b(n+1)}$ = voltages appearing at the top of the resistances, $R'_{d(n+1)}$, when $I = I_p$.

The stable voltage points, V_{rn}, defined by the intersection of the characteristic with the standing current, I_s, are given by equation (11) for n = 0,1,2,3...N.

$$V_{rn} = (N - n)R_{d1}\,I_s + \left[V_{fp} - R_{d2}\,(I_p - I_s)\right]n \qquad .. (11)$$

2.3.4.1. Lower Limit of Trigger Pulse Amplitude.

The linear static characteristic of figure 20 can now be used to establish the minimum amplitude, U_o, of the input pulses which will ensure sequential triggering of all tunnel diodes in the chain. It can be seen from figure 20, that the following inequality must be satisfied.

$$U_{on} > V_{b(n+1)} - V_{rn} + R(I_p - I_s) \qquad .. (12)$$

Replacement of $V_{b(n+1)}$ and V_{rn} from equations (10) and (11) respectively in equation (12), leads to the general expression for the minimum trigger voltage amplitude when $n = 0,1,2...(N-1)$.

$$U_{on} > V_p\left[0.75(N-n) + 0.5\right] - (N-n)R_{d1}I_s + (nR_{d2} + R)(I_p - I_s) \qquad .. (13)$$

Therefore, equation (13) represents the lower limit to be exceeded by the amplitude of the trigger pulse, U_o, in order to ensure that one diode will switch for every input pulse. A more pessimistic expression is derived if it is assumed that all units still in the low voltage state, are standing at their peak voltage, V_p, by the time the switching diode is at $1.25V_p$. In this case, the first term of equation (13) must be replaced by $V_p\left[(N-n) + 0.25\right]$, producing equation (14).

$$U_{on} > V_p\left[(N-n) + 0.25\right] - (N-n)R_{d1}I_s + (nR_{d2} + R)(I_p - I_s) \qquad .. (14)$$

It was pointed out earlier that the first expression is closer to reality than this last one when it comes to the calculation of the changes in the minimum amplitude, $\underline{U_o}$, from one end of the chain to the other. From equation (13), it can easily be found that the increment of, $\underline{U_o}$, from one step to the next is given by equation (15).

$$\underline{U_{o(n+1)}} - \underline{U_{on}} = R_{d2}(I_p - I_s) - (0.75V_p - R_{d1}I_s) \quad .. (15)$$

As an example, the following values for a typical 1N2941 may be replaced in equation (15): V_p = 60mv, I_p = 4.7ma, I_s = 3.3ma, R_{d1} = 9.6ohms, R_{d2} = 18.3ohms. The answer is + 12.3mv per step showing that the last diodes in the chain are more difficult to trigger than the first ones.

2.3.4.2. Upper Limit of Trigger Pulse Amplitude.

The upper limit of the trigger pulse amplitude is defined as the maximum voltage, $\overline{U_o}$, which must be fed to the input of the chain before two diodes can switch together.

It should be remembered that under the prevailing conditions, the diodes cannot pass their peaks simultaneously, and that the rate of rise of the input signal is limited such that one diode must complete its switching before the driving current can increase again towards the next peak. It is clear from figure 21, that the upper

LIMITS OF
TRIGGER PULSE AMPLITUDE

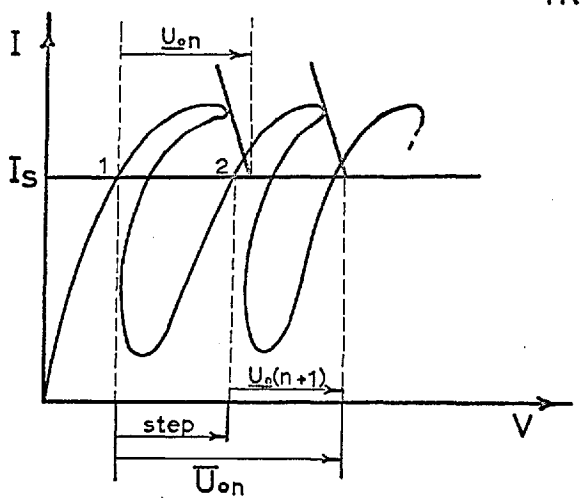


Fig. 21.

N	R (ohms)	Uo (nom.)	Tolerance
2	0	290mv	±75%
10	0	500	±41
10	500	1.2volt	±17
10	1000	1.9	±11
50	0	2.1	±7

TABLE II

limit, $\overline{U_o}$, must be smaller than the magnitude of the step generated by the tunnel diode being switched plus the amplitude of the lower limit valid for the next step. This statement can be written as in equation (16).

$$\overline{U_{on}} < \underline{U_o}(n + 1) + \text{Step} \qquad .. (16)$$

The magnitude of the step can be derived from equation (11), and is given by equation (17).

$$\text{Step} = V_{fp} - R_{d1} \cdot I_s - R_{d2}(I_p - I_s) \qquad .. (17)$$

Two expressions are available to define the lower limit, $\underline{U_o}(n + 1)$. Equation (14) will be used rather than equation (13) because its assumption that all tunnel diodes reach the peak every time one of them switches, leads to more pessimistic results for the range of acceptable input pulse amplitudes. This additional safety in the use of the resulting expressions will allow for the neglected production spread in the tunnel diode characteristics as well as for the influence of any capacitance to ground along the chain. Equation (14) can easily by shown to yield equation (18) for $\underline{U_o}(n + 1)$.

$$\underline{U_o}(n + 1) > \underline{U_{on}} - V_p + R_{d1} \cdot I_s + R_{d2}(I_p - I_s) \qquad ..(18)$$

Replacing the last two equations in equation (16), gives equation (19).

$$\overline{U_{on}} < \underline{U_{on}} + V_{fp} - V_p \qquad .. (19)$$

But U_{on}, in the above expression for the upper limit, must be obtained from equation (14) for n = N - 2. This value of n gives the smallest U_{on} of interest in the present case when two diodes still remain to trigger. The range of input pulse amplitudes is therefore defined by the following equations.

Upper Limit:

$$U_o < 1.25V_p - 2R_{d1} \cdot I_s + \left[R + (N - 2)\, R_{d2}\right](I_p - I_s) + V_{fp} \quad ..(20)$$

Lower Limit:

$$U_o > V_p(N + 0.25) - NR_{d1} \cdot I_s + R(I_p - I_s) \quad ..(21)$$

Equation (21) for the lower limit is simply the equation (14) in which n has been replaced by zero in order to give the maximum possible value of U_{on}.

As long as the amplitude of the driving signal is kept between the limits defined by equations (20) and (21) and provided the other conditions stated earlier are satisfied, one tunnel diode and only one will switch every time a pulse appears at the input of the chain.

If the nominal value of the input pulse is chosen to lie half way between the lower and the upper limits, its magnitude is given by equation (22).

$$U_o(\text{nominal}) = 1/2\left\{V_p(N + 1.5) - (N + 2)\, R_{d1}\cdot I_s + \left[2R + (N - 2)R_{d2}\right](I_p - I_s) + V_{fp}\right\} \quad .. (22)$$

The tolerance expressed in percent of that nominal value is then obtained from equation (23).

$$\text{Tolerance } (\%) = \quad .. (23)$$

$$\frac{\left[V_p(1 - N) + (N - 2)R_{d1}\cdot I_s + (N - 2)R_{d2}(I_p - I_s) + V_{fp}\right] \times 100}{V_p(N + 1.5) - (N + 2)R_{d1}\cdot I_s + \left[2R + (N - 2)R_{d2}\right](I_p - I_s) + V_{fp}}$$

In order to illustrate the usefulness of the above equations, they were used to calculate the nominal values and the tolerances of the input pulse amplitudes necessary to drive chains containing respectively 2, 10 and 50 tunnel diodes for various resistances, R. The results of table II were checked against measurements taken on four chains of ten tunnel diodes each. With a driving resistance of the order of 600 ohms, tolerances ranging from $\pm 15\%$ to $\pm 20\%$ were found acceptable on the input pulse amplitude. The magnitude of the resistance, R, was not well defined because a small capacitance to ground, in parallel with the chain, was introduced to decrease its effective value during the risetime of the input signal.

For very long chains, i.e. last case in table II when N = 50, certain factors like the necessarily larger

difference between the first and the last peak currents, could no longer be neglected. The minimum increment between the peak currents is dictated by their thermal coefficients and by the fastest rate of rise expected from the input signal. Chains of ten diodes were operated in the laboratory with peak currents differing by as little as 15 to 20μA. However, for normal room temperature fluctuations, it would not be advisable to operate with differences considerably less than about 40μA. Even if the peaks were separated by only 30μA, for N = 50, the over-all change in peak currents would be 50 x 30μA = 1.5ma. In the case of the 1N2941, this amounts to more than 30% of the typical I_p. Consequently, the additional restrictions imposed on the tolerance of U_o would soon make it impossible to trigger reliably only one tunnel diode at a time unless true current drive as described earlier were employed.

Nevertheless, it may be concluded that the requirements imposed on a chain of ten tunnel diodes and on its driving voltage pulses in order to ensure reliable sequential switching of all the diodes, can be easily met in practice. The circuit of figure 7. is therefore interesting as far as its dynamic behaviour is concerned. The staircase waveform generated across the chain must now be considered from the point of view of static precision and linearity.

2.3.5. The Staircase Waveform.

When the tunnel diodes in the circuit of figure 7 are being switched in turn, the voltage at the output of the chain after all transients have disappeared, is given by equation (11). This expression of the output waveform is repeated here for convenience together with the related equation (17) describing the steps produced in the output voltage every time one more diode switches to the high voltage state.

$$V_{rn} = (N - n)R_{d1} \cdot I_s + \left[V_{fp} - R_{d2}\,(I_p - I_s)\right] n \quad .. (11)$$

$$V(\text{step}) = V_{fp} - R_{d2}(I_p - I_s) - R_{d1} \cdot Is \quad .. (17)$$

Apart from the current, I_s, all the parameters in these equations belong to the tunnel diode characteristic.

The current source was analysed in Appendix A.5. It is made up of a single transistor biased in the common-base configuration with the aid of a temperature compensating zener diode. The specifications in Appendix A.5. show that the current, I_s, is defined by an effective resistance of 760kΩ. The magnitude of the step generated by a typical 1N2941 tunnel diode (see Appendix A.9), is of the order of 450mv for I_s between 3 to 4ma. In a chain defining ten levels, the output voltage range would be 10 x 450mv = 4.5 volts, producing a decrease of the current,

I_s, equal to 4.5 volts/760kΩ or less than -6μA. The effect on the last step in the chain would be smaller than $\Delta I_s R_{\partial 2}$ or -6μA x 18.3 = -109.8μv, approximately -.002% of full scale. For most applications, such a small error would be negligible. In any case, if the average step in a chain is calculated from values measured while the current source is present, the small reduction in I_s is automatically taken into account.

It can also be seen in the performance data for the current source (Appendix A.5), that I_s is influenced by ambient temperature changes. Its thermal coefficient is equal to +0.3μA/°C and even for a variation of +10°C in room temperature it is only +3μA. A difference as large as 6μA in I_s was shown in the above paragraph to have negligible effect on the precision of the steps.

The parameter, I_s, in equations (11) and (17), can therefore be considered as a constant in the following study of the accuracy of the staircase voltage waveform.

2.3.6. Precision of the Steps in the Chain.

If the staircase waveform is to serve as the reference in a quantizer, it is of prime importance that the steps should be equal to one another within a reasonable accuracy. It is now intended to summarize the results of an investigation on the subject carried out on a sample of

forty 1N2941 tunnel diodes manufactured by General Electric.

At constant temperature and for a fixed value of I_s, equation (17) gives the magnitude of the voltage step contributed by any one tunnel diode in the chain. Unfortunately, owing to production spread, the parameters V_{fp}, I_p, R_{d1} and R_{d2} are different between units of the same type. Measurements were taken on four chains each containing ten unselected tunnel diodes (1N2941). In the first two cases, the steps were respectively within ±4% and ±5% of their averages. The two other chains contained one odd unit each, causing the steps to be accurate only within -4% to +6%. Straightforward replacement of these two diodes improved the precision such that three of the chains had their steps within ±4% of their averages.

It is believed that this sample of 40 units is fairly representative of the production spread to be expected from a large number of 1N2941 and to a certain extent, from other germanium tunnel diodes of similar construction. It should be noted that these diodes were bought from the same manufacturer in two separate orders at a year interval. No difference in their characteristics could be detected during the measurements apart from normal production spread. In so far as these assumptions are valid, it can be said that a precision of ±6% between the

steps can be attained in tunnel diode chains without any selection. Simply by rejection of a few units, this figure can be reduced to ±4%.

In order to improve the accuracy even further the same forty diodes were selected according to their voltage steps to constitute four new chains. The idea was to get maximum accuracy in two of the chains while keeping the others to better than ±5% with the remaining diodes. The motive behind this approach will be clarified later on by the study of the precision requirements for the complete reference unit of the quantizer. Out of the four chains, the following accuracies were measured: one achieved ±1%; two others, ±2% and the remaining one ±5% as its diodes were not selected. These results are most significant considering that there was a restricted number of diodes to select from. It should be remembered that all of these chains can be operated at 10Mc/s p.r.r. and that the diodes were consequently chosen according to their peak currents for reliable triggering. It is believed that with as little as ten extra tunnel diodes, the four chains could have been selected to better than ±1% without any great effort. In any case, selection need not achieve a precision superior to ±2% as trimming can take over in that range of accuracy.

The method of increasing the precision of the steps in a chain by trimming is described in Appendix A.6. It consists of shunting one or more diodes in the chain with individual resistances. As long as a tunnel diode remains in the low voltage state, only a small current is diverted by its shunt. When the diode switches to the high voltage state, the parallel resistance takes a significant portion of the current, I_s, effectively reducing the magnitude of the step generated by this particular diode. It was shown in Appendix A.6 that a step can be reduced easily by more than 2% in this way. The shunting resistance can therefore be adjusted experimentally until the desired precision is obtained. The effect on the other diodes in the chain is obviously nil as far as accuracy is concerned. The order of triggering of the diodes is controlled mainly by the relative magnitudes of the peak currents. If the trimming resistance becomes small enough to divert a current, while the diode is in the low voltage state, equal to or greater than the increment between the peak currents, the order of triggering is affected and two diodes may switch together. In this case, the dynamic properties of the chain may be recovered by the introduction of a small capacitance to ground between the two units switching together. Both capacitive and resistive trimming were used on one of the chains to serve

as an illustration. With only two shunting resistances of 680Ω and 470Ω respectively, the accuracy in the chain was improved from ±2% to ±1%. One trimming capacitor was needed to restore the normal sequential switching. Complete description of the diodes in the four chains finally adopted can be found in Appendix A.7, together with the results of the accurate measurements of their steps.

It can therefore be concluded that an accuracy of better than ±1% between the steps can be obtained by selection of ten tunnel diodes in a chain biased with a constant current source. This figure can certainly be improved by trimming to better than ±0.1%. The temperature would have to be controlled carefully as it would soon impose a limit on the precision of the chain because of its effect on the tunnel diode characteristic.

The sensitivity of the tunnel diode chain to temperature variations will be analysed in chapter 3 in relation with an expression for the net thermal drift in the reference of the quantizer.

The argument thus far has shown that the tunnel diode chain can serve as a high speed accurate staircase waveform generator. Various methods of resetting the chain to zero will now be discussed.

2.4. Methods of Resetting.

The most useful methods of resetting employ a transistor switch to short circuit the constant current source to ground, reducing the current in the chain to a value below the minimum I_v thus returning all the tunnel diodes to the low voltage state.

The resetting transistor may be controlled in a number of ways, three of which will be mentioned:

1. Direct transistor switching (Ref.32, page 48);
2. Level detector with transformer feedback (Ref.35);
3. Intermediate switching.

Direct transistor switching is the simplest method and will be described in detail later in order to investigate the problems related to the resetting of the chain. The second system utilises two transistors interconnected by a transformer feedback loop to generate a reset pulse. The first transistor serves as a level detector and is cut off until a pre-selected number of tunnel diodes have switched to the high voltage state. The last step brings the first transistor into conduction and a coupling transformer feeds a large current pulse into the base of the second transistor which saturates for long enough to reset the chain. This circuit has been described in

the literature[35], and the explanation will not be pursued any further. The third method is an improved version of the first one as it simply introduces a tunnel diode for regeneration between the chain and the transistor. Its performance is at least comparable to that of the second method but it uses only one transistor and no transformer. It will be adopted for the present system for reasons which will become clear later on.

2.4.1. Direct Transistor Switching.

Figure 22 represents a tunnel diode chain connected across the output of a common-emitter transistor. As long as the last tunnel diode, N, remains in the low voltage state ($V_1 < 65$ mv), the transistor is cut off and the operation of the chain is not affected. The presence of a small capacitance, C_b (20 to 47_{pf}), ensures that the diode, N, is the last one to trigger, therefore permitting full use of the chain before the transistor comes into action. This capacitance, C_b, is unnecessary if the diode, N, has the largest peak current in the chain.

2.4.1.1. Resetting Action.

The basic resetting process is very simple. When the last tunnel diode is triggered to the high voltage state, ($V_2 \cong 500$ mv), the current begins to increase

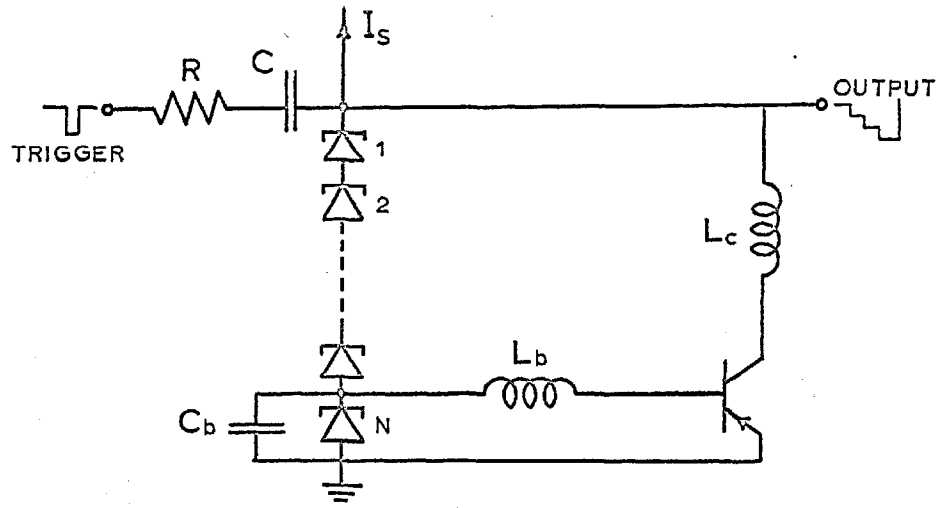

I_S
R
C
OUTPUT
TRIGGER
1
2
L_c
L_b
C_b
N

Fig. 22.

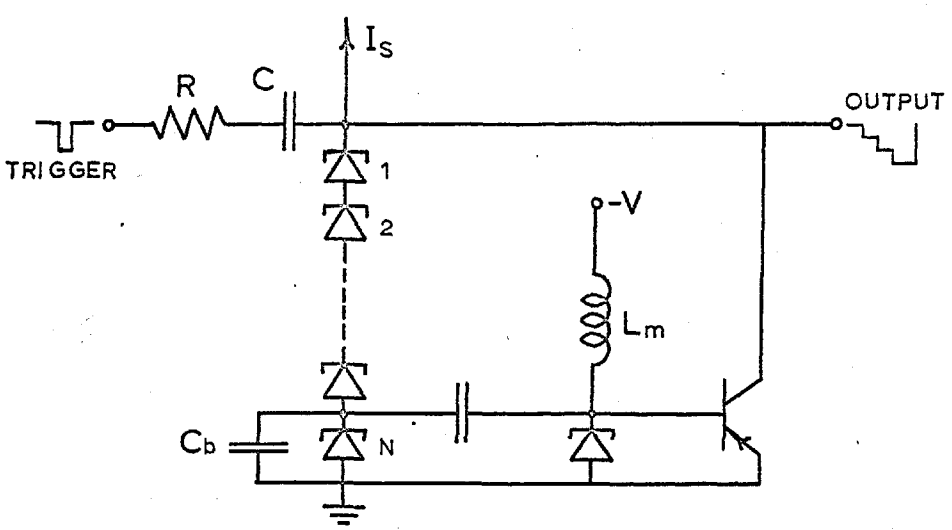

I_S
R
C
OUTPUT
TRIGGER
1
2
-V
L_m
C_b
N

Fig. 23.

in the base inductance, L_b , and the transistor starts diverting the source current, I_s. If the saturation resistance of the transistor is small enough, the current in the chain falls below the minimum I_v and all the diodes resume the low voltage state. At the same time the base current starts to decrease and the transistor cuts off.

Addition of a collector inductance, L_c, is not necessary for the resetting to take place normally provided the saturation resistance of the transistor is low enough. If this is not the case and it is found that one or more diodes do not reset, a small inductance, L_c (4 to 10μh), causes an overshoot when the transistor switches off and permits total resetting to occur.

The base inductance, L_b, on the other hand, cannot be removed. The exact behaviour of the circuit of figure 22, when the base is connected directly to the chain, depends on the $V_{be} - I_b$ characteristic of the transistor as well as on its current gain and its cut-off frequency. Consider for instance the operation of the circuit in the absence of L_b. When the resetting action is initiated by the triggering of the last tunnel diode, the transistor starts diverting part of the current, I_s, from the chain. Consequently, the voltage across the last diode decreases and the base current is immediately reduced. This rapid

feedback prevents the transistor from staying into saturation for long enough and only partial resetting can occur. Furthermore, because of the loading effect of the current, the last tunnel diode is easier to reset than the others and tends to cut off the transistor prematurely. With some transistors, a stable condition can be reached, when L_b is removed, where the last diode stays just above the valley voltage and the source current, I_s, is divided between the transistor and the chain. All of these difficulties disappear when L_b is greater than a certain minimum. It can be said therefore that the inductance, L_b, delays the signal to the base of the transistor such that complete switching can occur. In that sense, the presence of the transformer in the second method described previously served the same purpose. However, that second method is superior to the direct transistor switching scheme because it introduces amplification in the control loop.

2.4.1.2. Disadvantages of the Direct Transistor Switching Technique.

The above considerations reveal some of the disadvantages of the direct transistor switching technique. The exponential rise and fall of the base current in the inductance, L_b, when switching the transistor, unduly

increases the resetting time of the chain. No reverse drive is available to bring the transistor cut of saturation more rapidly. Full advantage cannot be taken of the potential speed of the transistor and of the tunnel diodes used as the minimum L_b sets the limit. The inductance, L_b, must keep the base current large for long enough such that the input of the transistor does not detect the decrease in driving signal until resetting of the chain is completed. The minimum acceptable value of the inductance, L_b, therefore depends on the magnitude of the source current, I_s, the current gain and the cut off frequency of the transistor as well as the exact shape of its input characteristic in the common-emitter configuration, the total capacitance in parallel with the chain and the forward peak voltage, V_{fp}, of the last tunnel diode.

A minimum over-all resetting time of 0.25μsec was achieved with the circuit of figure 22, using an OC171 or an ASZ21 transistor across a chain of ten 1N2941 tunnel diodes passing a current I_s = 4 ma. The base inductance had to be greater than 15 to 20 μh and a small collector inductance was necessary for reliable resetting. A capacitive load of 100pf to ground increased this switching time to about 0.27 μsec.

The maximum speed of operation of the chain being limited to approximately 3.5Mc/s by the presence of L_b, it

was decided to investigate some other method of resetting. Considerable reduction of the resetting time can be achieved if one tunnel diode is inserted in the control loop between the chain and the transistor in order to provide some regeneration of the driving signal. This intermediate switching approach is much superior to the first method just described as will now be seen.

2.4.2. Use of Intermediate Switching.

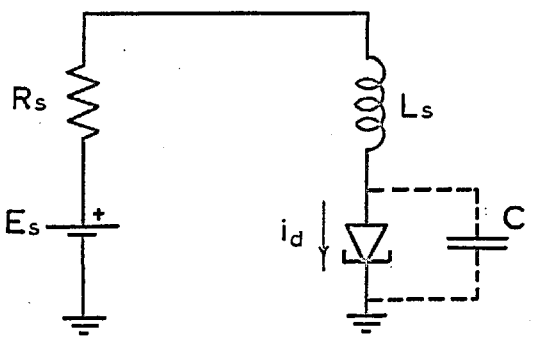
A much faster resetting circuit avoiding the use of a base inductance is illustrated in figure 23. The last diode in the chain triggers a monopulser which in turn switches on the resetting transistor. The transistor stays in saturation for a time controlled by the magnitude of the inductance, L_m. The base current is not supplied by the chain itself as before and the delay introduced by L_b is no longer needed for complete switching to occur. Furthermore, a larger base current is available for faster "switching on" of the transistor. The saturation resistance is therefore reduced, making the collector inductance, L_c, unnecessary. Finally, the transistor is switched off much more rapidly as a reverse base current is applied when the monopulser returns to its initial state. The resetting of the chain is therefore dependent to a large extent on the action of the monopulser and maximum switching speed must be aimed at in the design of this most important unit.

It was pointed out earlier, in section 2.2.2. that the simple tunnel diode circuit of figure 5. could be used as a monopulser. The main reason for referring to the diagram of figure 5. as the "basic circuit", lies in the fact that only one of its various configurations needs to be analysed completely. The results can then be applied with minor changes to a large variety of circuits derived from this basic unit. The astable oscillator is the simplest of all configurations as it does not need any external triggering signal. It will therefore be chosen to derive the general equations which will then be adapted to the design of all the tunnel diode switching circuits to be used in the quantizer.

2.5. The Astable Oscillator.

Figure 24. represents the circuit diagram of a tunnel diode relaxation oscillator and figure 25. is a piecewise-linear approximation of its characteristic.

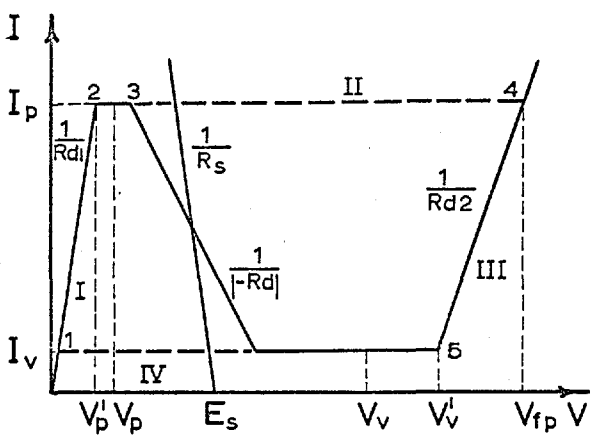
Qualitatively, the operation of the tunnel diode relaxation oscillator is easily explained. When the bias voltage, E_s, is first turned on, the current builds up in the series inductance, L_s. As soon as the peak current, I_p, is attained, the tunnel diode switches to the high voltage state (point V_{fp}). Instability in the negative region is ensured even with $R_s < |-R_d|$, if the dynamic



ASTABLE

OSCILLATOR

Fig. 24.



ELECTRICAL

CHARACTERISTIC

Fig. 25.

load impedance is greater than $|-R_d|$ at the operating point[36]. For very small values of L_s, the oscillation is sinusoidal. If L_s is large enough, however, relaxation oscillation builds up. In this latter case, the tunnel diode reaches the high voltage region rapidly and develops a voltage drop greater than the supply voltage itself. The current starts to decrease gradually through L_s until the valley point where the tunnel diode switches back to the low voltage region. The first cycle is completed and starts repeating itself as the current builds up again in L_s.

In order to avoid the solution of nonlinear differential equations, in the analysis of the relaxation oscillator, the linearized characteristic given in Appendix A.1. will be used for the tunnel diode. Analytical expressions have been derived to fit the characteristic of the tunnel diode[37, 38], but they are themselves approximations. In view of the added complexity, their use would not be justified here. The present analysis aims at the derivations of formulas with an accuracy better than ±10% and the linear approximation is perfectly adequate as will be seen later.

The following analysis relies on the assumption that L_s is made large enough to ensure constant current switching from the low to the high voltage state and vice versa. It is also postulated that L_s controls the changes

in the current and that, in the regions 1 to 2 and 4 to 5 of figure 25, the presence of the parallel capacitance may be neglected e.g. $R_{d2}C_1 \ll L/(R_{d2} + R_s)$. The validity of these simplifications has been verified experimentally, (see Appendix A.3.), by checking the accuracy of the resulting equations for the relaxation oscillator. Bearing in mind these conditions, the characteristic of figure 25. can be reproduced by four linear models, each describing its particular region of the curve. These equivalent circuits are given in figure 26. and are labelled according to figure 25. The analysis of the relaxation oscillator can now be carried out.

Region I: from 1 to 2, figure 25.

In this region, the first circuit of figure 26. is valid and the well known expression for the building up of a forced current in an inductance can be written directly.

$$i = \frac{Es}{R_{t1}} (1 - e^{-t/\tau_1}) \qquad .. (24)$$

where $\tau_1 = L/R_{t1}$

$R_{t1} = R_s + R_{d1}$

Equation (24) can be used to find the time necessary for the current to increase from an initial value I_1 to a final

Linear Equivalent Circuits for Computation of Switching Times of the Tunnel Diode Relaxation Oscillator.

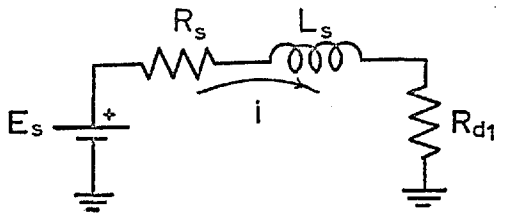
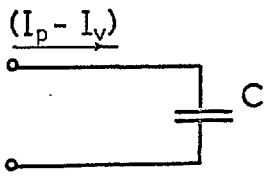
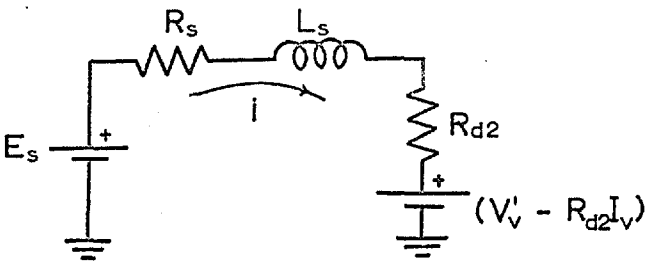
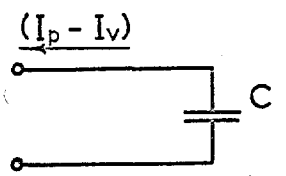
Equivalent Circuits (see fig. 24.)	Region of Validity (see fig. 25.)
	From 1 to 2
	From 2 to 4
	From 4 to 5
	From 5 to 1

Fig. 26.

value I_2.

$$t_{1-2} = \tau_1 \ln \left[\frac{E_s - R_{t1} I_1}{E_s - R_{t1} I_2} \right] \quad .. (25)$$

In the case of the relaxation oscillator, I_2 is equal to the peak current, I_p, of the tunnel diode and, provided L is large enough, I_1 is the valley current, I_v.

Region II: from 2 to 4, figure 25.

The presence of the negative resistance contributes to a very fast switching from the peak point voltage, V_p, to the forward voltage, V_{fp}. The current in the inductance, L_s, does not change appreciably during that time and a current, $I_p - I_d$, is available to charge the capacitance, C. It can be seen from figure 25. that a good approximation would be to assume that the capacitance charges at a constant current $I_p - I_v$. The amount of charge accumulated on C during the switching can be expressed in terms of the charging current or as a function of the voltage variation.

$$Q = (V_{fp} - V_p) . C = (I_p - I_v) . t_{2-4} \quad .. (26)$$

$$t_{2-4} = \left[\frac{V_{fp} - V_p}{I_p - I_v} \right] . C \quad .. (27)$$

It is seen that this time is controlled almost entirely by the characteristics of the tunnel diode used. A typical 1N2941, for instance, would give t_{2-4} = 5.2 nsec with C = 50pf.

Region III: from 4 to 5, figure 25.

As soon as point 4 is reached, the third equivalent circuit of figure 26. becomes operative. The solution for the loop current is the same as for region I except that the net voltage is now the difference between E_s and $(V_v' - I_v R_{d2})$.

$$i = \frac{E_s - (V_v' - I_v R_{d2})}{R_{t2}} \left[1 - e^{-t/\tau_2}\right] \qquad .. (28)$$

where $\tau_2 = L/R_{t2}$

$$R_{t2} = R_s + R_{d2}$$

Equation (28) is transformed to give the time for the current to decrease from point 4 to point 5.

$$t_{4-5} = \tau_2 \ln \left[\frac{E_s - V_v' + I_v R_{d2} - R_{t2} I_4}{E_s - V_v' + I_v R_{d2} - R_{t2} I_5}\right] \qquad .. (29)$$

If I_4 is replaced by I_p and I_5 by I_v, the expression may be simplified.

$$t_{4-5} = \tau_2 \ln \left[\frac{V_{fp} + R_s I_p - E_s}{V_v' + R_s I_v - E_s}\right] \qquad .. (30)$$

Region IV: from 5 to 1, figure 25.

The arguments used for the analysis of the switching process from 2 to 4 (region II) still apply in this last region. It can be seen from figures 25 and 37 that equation (31) is intended to represent the rapid switching to the low voltage state shortly after V_v is passed.

For practical reasons, the neglected transition time from point 5 to V_v is considered as an additional error in t_{4-5}. The times t_{2-4} and t_{5-1} will normally be negligible in the design equations.

$$t_{5-1} = \left[\frac{V_v - V_1}{I_p - I_v}\right] \cdot C \qquad .. (31)$$

Accuracy of Equations (24) to (31).

In order to assess the amount of inaccuracy introduced by the approximations of the above analysis, a relaxation oscillator was designed and measurements were taken for a wide range of supply voltages, E_s. Theoretical results, from equations (25), (27), (29) and (31), were within ± 10% of the measured values as long as E_s was sufficiently greater than V_p but less than about $1/2 \cdot V_v$ (see Appendix A.3.). For larger values of E_s, the linear approximation in the high voltage region (R_{d2} in figure 25), introduced serious errors. In these cases, the time necessary for the current to decrease in the inductance, L_s, from a value corresponding to the voltage V_v', to the valley point current, I_v, is no longer negligible. This time is proportional (as a first estimation) to $L_s \Delta_i/(E_s - V_v)$ and can become very large when E_s approaches V_v. New equations have been derived in Appendix A.2. defining two segments instead of one to describe the tunnel diode characteristic in the high voltage region. With very little added complexity, the results using the new

equations were found to be accurate to better than 5% for values of E_s as high as 97% of V_v.

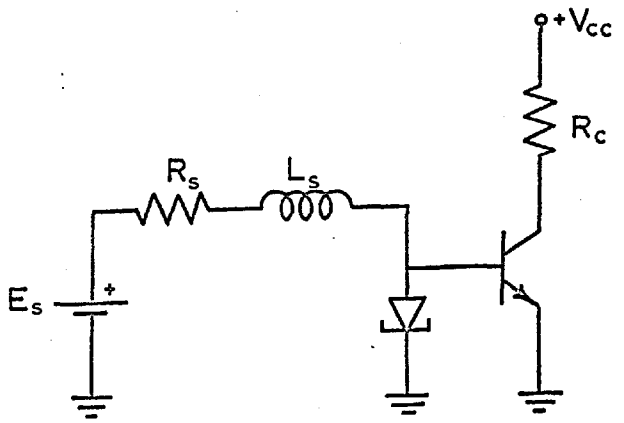
The first analysis, based on the linear model of figure 25, has permitted the derivation of simple equations describing the operation of the tunnel diode relaxation oscillator. Their accuracy, however, was maintained to better than $\pm$ 10%, only for a narrow range of the supply voltage, E_s. The much superior model of Appendix A.2 extends the usefulness of these basic equations to the entire range of possible values of the supply voltage, E_s, and ensures improved accuracy. These results can also be applied directly to the case of resistive loading of the tunnel diode, provided that the load is sufficiently greater than the negative resistance of the device (more than a few hundred ohms for the 1N2941).

2.5.1. Loading of the Tunnel Diode by a Transistor.

In most practical circuits to be discussed here, the tunnel diode is directly coupled to a common-emitter transistor. Fortunately, this case turns out to be much simpler than may be expected at first. It will be shown that equations (27) to (31) need only minor alterations to take into account the influence of the transistor on the operation of the tunnel diode relaxation oscillator.

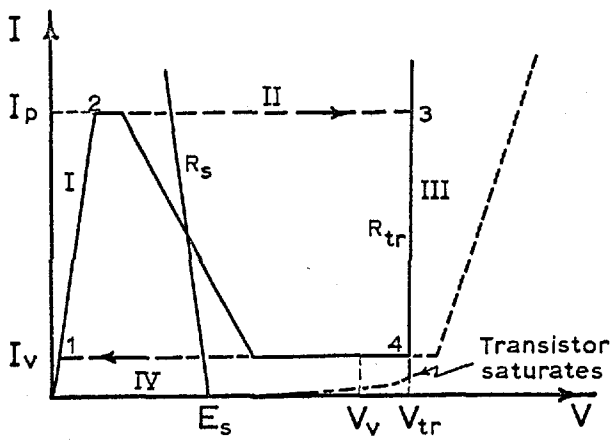
The circuit diagram of a complete relaxation oscillator, including a transistor, is presented in figure 27. The forward voltage, V_{fp}, for a germanium tunnel diode is of the order of 500 mv. On the other hand, the base to emitter voltage for a medium power germanium transistor does not exceed normally 450 mv, even at the maximum rating of the transistor. The collector current must therefore be limited to a safe value by a resistor R_c (figure 27) and the transistor saturates when the tunnel diode switches to the high voltage state. Figure 28. reproduces the V_{BE} vs I_B curve for a typical medium power high speed switching germanium transistor, superimposed on the characteristic of a tunnel diode. A piecewise-linear approximation of the combined characteristic is also illustrated. In that figure, V_{tr} represents the voltage appearing between the base and the emitter when the transistor is in saturation. For the two transistor types used, 2N797 and ASZ21, and for the current range of interest, that voltage lies between 350 mv and 450 mv. For design purpose, V_{tr} may be selected as 400 mv.

Assuming a valley current, I_v = 0.6ma, and a minimum current gain, β = 20, a collector current, I_c = 12ma, would be flowing in the transistor for I_b equal to I_v. If a collector resistance, R_c, limits the current to approximately that level, the transistor enters into saturation



RELAXATION OSCILLATOR

Fig. 27.



ELECTRICAL CHARACTERISTIC

Fig. 28.

for $I_b = I_v$. The input dynamic resistance, R_{tr}, of a saturated transistor in the common-emitter configuration is very low. A simple argument can illustrate this fact.

The dynamic resistance of the forward biased emitter-base diode of a transistor can be evaluated from the well known approximation r_e (ohms) = $26/I_e$(ma)[39,page 17]. The resistance seen at the base of the same transistor is given by $r_b = \Delta V_{be}/\Delta I_b$ or $r_b = (\Delta V_{be}/\Delta I_e)(\beta + 1) = r_e(\beta + 1)$. As long as the transistor operates in the active region, these expressions are valid. When saturation is reached, however, the collector current is maintained almost constant by the resistance, R_c, and any further increase of the emitter current must be diverted to the base, i.e. $\Delta I_b \cong \Delta I_e$. The dynamic resistance at the base, $r_b = \Delta V_{be}/\Delta I_b$, becomes $r_b = \Delta V_{be}/\Delta I_e = r_e$. The resistance, R_{tr}, in figure 28, therefore represents the forward resistance of the emitter-base diode of the transistor and it can be estimated as a function of the base current from the expression given above for r_e. From figure 28, it is seen that the base current immediately after the tunnel diode has switched to the high voltage state, is of the order of $(I_p - I_v)$ or 4.1ma for a typical 1N2941, giving a value of 6.4ohms for R_{tr}.

The resistance, R_{tr}, is therefore very small and will be taken as zero for the present application. This

choice is justified if the following points are remembered. The resistance, R_{tr}, is in series with R_s and in parallel with the tunnel diode. Its exact contribution to the time of transition from 3 to 4 in figure 28. is not critical. On the other hand, the time factor $L_s/(R_s + R_{tr})$ is not constant because R_{tr} gets larger when the base current decreases. The transition from 3 to 4 is nonlinear and most of t_{3-4} occurs in the upper part of the line 3-4 (figure 28.) where I_b is large and R_{tr} is small. This last remark seems to suggest that R_{tr} should be chosen slightly larger in order to take its variation into account. However, in practical circuits, the supply voltage, E_s, is normally of the order of $\frac{1}{2}.V_v$ or larger. It was pointed out earlier, in connection with equation (29), that under these conditions, the method of analysis tended to underrate the transition time in that region of the curve. An improved approximation for the tunnel diode characteristic was even developed in Appendix A.2. to overcome this difficulty. Fortunately, this error can be compensated, when a transistor is loading the diode, simply by choosing R_{tr} smaller in order to increase the time constant $L_s/(R_s + R_{tr})$. It was found in practice that the best correction was obtained by reducing R_{tr} to zero in the equations which will now be derived. The accuracy of these assumptions can be verified from the results tabulated in Appendix A.4.

2.5.2. Computation of the Switching Times.

The equations for the switching times of the tunnel diode relaxation oscillator loaded by a transistor can now be established. Comparison of figure 28. to figure 25. shows that the presence of the transistor can be ignored in the determination of the combined characteristic, until the transistor enters into saturation.

Region I and IV: from 1 to 2 and from V_v to 1, figure 28.

It follows from a comparison of figure 28. with figure 25. that region I (from 1 to 2) and region IV (from V_v to 1), are not affected by the presence of the transistor. Equations (25) and (31) therefore apply respectively to these cases.

Region II: from 2 to 3, figure 28.

Equation (27) can be used as it is, ignoring the presence of the transistor. In fact, the transistor diverts part of the total current $(I_p - I_v)$ during that interval, increasing the charging time of the capacitance, C. Employing V_{fp} instead of V_{tr} in the computation of t_{2-3}, tends to correct for that effect otherwise neglected in the formula. In any case, this risetime accounts for only a small fraction of the total period; the added complexity of a more accurate expression would not be justified.

Region III: from 3 to 4, figure 28.

The derivation of equation (29) is still perfectly valid but the following changes must be made: V'_v is replaced by V_{tr} and R_{d2} by R_{tr} which is equal to zero.

$$t_{3-4} = \tau_2 \ln\left[\frac{E_s - V_{tr} - R_{t2}I_p}{E_s - V_{tr} - R_{t2}I_v}\right] \qquad .. (32)$$

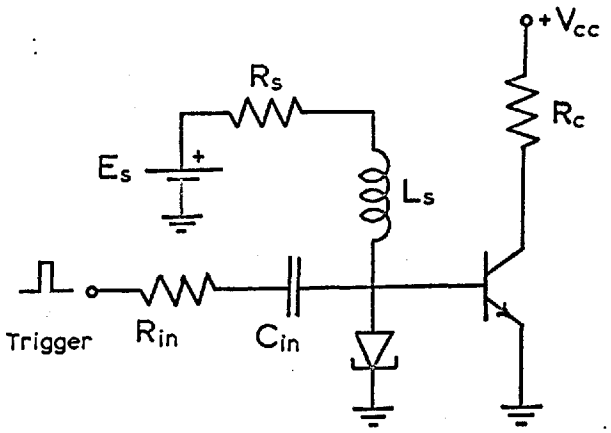
where $\tau_2 = L_s/R_{t2}$

$R_{t2} = R_s$

Appendix A.4. shows that equations (25), (27), (31) and (32), can be used to compute the period of a tunnel diode relaxation oscillator loaded by a common-emitter transistor, to an accuracy better than 5%. This series of equations will be applied later in a discussion of the design of a monopulser, a 10 Mc/s pulse generator and a one-tunnel diode flip flop. They will now be adapted to the case of the tunnel diode monopulser to be used in the building block for the high speed staircase generator.

2.6. The Monopulser.

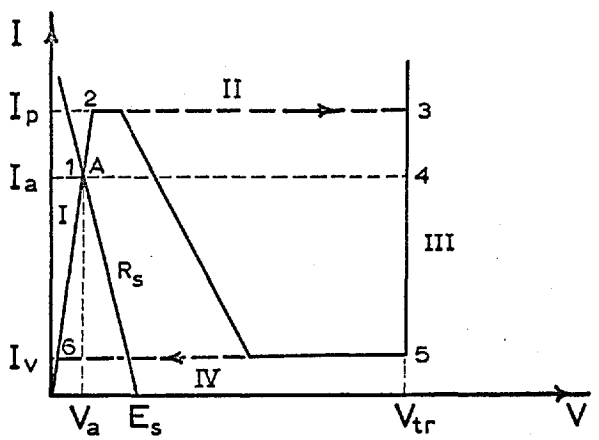
The principle of operation of the tunnel diode monostable trigger circuit (figure 29.) is illustrated by figure 30. The tunnel diode is biased in the low voltage



TUNNEL DIODE

MONOPULSER

Fig. 29.



ELECTRICAL

CHARACTERISTIC

Fig. 30.

region (below V_p) by a small voltage, E_s, in series with a resistance R_s. The voltage drop, V_a, across the tunnel diode is smaller than 60 mv and the transistor is cut off. On the incoming of a positive trigger pulse, the peak point, (V_p, I_p), is reached after a time controlled mainly by the pulse generator. As soon as the peak is passed, the operation of the circuit is similar to that of the relaxation oscillator analysed in sections 2.5 and 2.5.1. Equations (25), (27), (31), and (32) still apply to the description of the switching times but the presence of the trigger pulse during the transition from 2 to 3 (figure 30.) and the introduction of a stable point in region I must be taken into account. In order to find out what changes are necessary in these equations, figure 30. may be used to follow the sequence of events over one complete cycle of the monostable.

A- From 1 to 2, figure 30.

As stated before, this time depends entirely on the risetime of the input pulse when loaded by the tunnel diode. It concerns the design of the pulse generator and does not enter into the analysis of the monopulser.

B- From 2 to 3, figure 30.

Equation (27) still holds for reasons given in section 2.5.2. but I_p must be replaced by ($I_{in} + I_a$), the

new current charging the capacitance, C, being $(I_{in} + I_a - I_v)$, assuming that the input pulse width is greater than t_{2-3}. For the present design purpose, however, $(I_{in} + I_a)$ is normally close enough to I_p for equation (27) to be used directly.

C- From 3 to 4, figure 30.

If the input pulse is still supplying current at the end of time t_{2-3}, the high voltage state is reached at a current level equal to $(I_a + I_{in})$. The current in the base of the transistor decreases by an amount equal to I_{in} when the input signal is removed. As long as the duration of the input signal is sufficiently smaller than the pulse width of the monopulser itself, the timing is not affected as the net shift is zero.

D- From 4 to 5, figure 30.

It follows from "C" above, that the current has to decrease effectively from a value I_a to I_v. If I_p is replaced by I_a, equation (32) still applies.

$$t_{4-5} = \tau_2 \ln \left[\frac{E_s - V_{tr} - R_{t2} I_a}{E_s - V_{tr} - R_{t2} I_v} \right] \qquad .. (33)$$

where all parameters are defined as for equation (32).

E- From 5 to 6, figure 30.

In this case, equation (31) can be used directly as explained in section 2.5.2.

F- From 6 to 1, figure 30.

Because of the presence of the stable point, (I_a, V_a), one more factor must be introduced in equation (25) before it can be used to compute t_{6-1}. If I_2 is merely replaced by I_a, in equation (25), a time equal to infinity would be obtained. This result is not surprising if it is remembered that in equation (24), the final value of the current, $I = E_s/R_{t1}$, will be mathematically attained only after an infinite time. On the other hand, an exponential function is already at 95% of its final value after only three time constants. Defining n as some important fraction of I_a, it is now possible to write equation (27) in a form applicable to the monostable circuit.

$$t_{6-1} = \tau_1 \ln \left[\frac{E_s - R_{t1} I_v}{E_s - R_{t1} n I_a} \right] \qquad .. (34)$$

where $\tau_1 = L_s/R_{t1}$

$R_{t1} = R_s + R_{d1}$

n = important fraction of I_a

For design purpose, n can be estimated from the following inequality (see section 3.5.2.2.):

$$n \geq \frac{I_p\,(max) - I_{in}\,(min)}{I_a} \qquad .. (67)$$

2.6.1. Design Equation for the Tunnel Diode Monopulser.

The duration of one cycle of the monopulser can be expressed as the summation of the times given by equations (27), (31), (33) and (34).

$$T = t_{2-3} + t_{4-5} + t_{5-6} + t_{6-1} \quad \text{(see fig.30)}$$

In this expression, t_{2-3} and t_{5-6} are proportional to the total capacitance, C, in parallel with the tunnel diode, while t_{4-5} and t_{6-1} are proportional to the inductance, L_s.

$$T = L_s(K_1 + K_2) + CK_3$$

$$L_s = \frac{T - CK_3}{K_1 + K_2} \qquad .. (35)$$

where

$$K_1 = \frac{1}{R_{t1}} \ln\left[\frac{E_s - R_{t1}I_v}{E_s - R_{t1}I_a}\right]$$

$$K_2 = \frac{1}{R_{t2}} \ln\left[\frac{E_s - V_{tr} - R_{t2}I_a}{E_s - V_{tr} - R_{t2}I_v}\right]$$

$$K_3 = \frac{V_{fp} + V_v - V_p - V_1}{I_p - I_v}$$

Equation (35) is a useful design expression.

2.6.2. Design Procedure for Monopulser.

Notes: 1. Worst case design procedure has been applied to all circuits in the staircase generator. For simplicity, the following conventions will be used: a line above a symbol indicates a maximum and a line under a symbol indicates a minimum.

2. Data concerning the production spread about typical values for the various parameters of the 1N2941 tunnel diodes are reproduced in Appendix A.9.

1. Choose T, the period of the monopulser, as the minimum spacing between two consecutive input pulses.

2. Estimate the minimum trigger current, $\underline{I_{in}}$, from a knowledge of the driving circuit.

3. Select the operating current, I_a.

$\underline{I_a} > \overline{I_p} - \underline{I_{in}}$ and $\overline{I_a} < \underline{I_p}$

4. Choose the series resistance, $R_s < |-R_d|$.

R_s must not be reduced unnecessarily if the monopulser is to operate with a period $T < 0.1\ \mu$sec, otherwise, L_s would have to be made so small as to become impracticable. The maximum value for R_s is given by the inequality $\overline{R_s} < (V_v - V_a)/(I_a - I_v)$.

5. Compute the magnitude of the supply voltage, E_s.

$$E_s = (R_{d1} + R_s)\, I_a \qquad ..(36)$$

6. From equation (35), determine the maximum inductance, L_s.

7. Design the input coupling network according to the characteristics of the driving circuit. A coupling capacitor approximately equal to three times the parallel capacitance of the tunnel diode is a good compromise. This value is normally small enough to differentiate the input pulse, introducing some isolation between the driving circuit and the monopulser during the operation. On the other hand, it is large enough to pass adequately the leading edge of the trigger pulse. These remarks are perfectly valid at least for the range of frequencies envisaged for the staircase generator (up to 20 Mc/s p.r.r. and for pulse widths down to 50nsec).

2.6.3. Practical Design of a Monopulser.

It was pointed out in section 2.4.2. that a tunnel diode monopulser could be used to control the resetting transistor (figure 23.). The procedure just outlined has been applied to the design of a circuit meeting the various requirements as will now be described.

If the ten-tunnel diode chain is to operate continuously at a maximum speed of 10 Mc/s, resetting will be initiated at 1.0 μ sec intervals (period, T, in equation (35)). The resetting action has to be completed within less than 0.1 μ sec, (pulse width of monopulser is given by equation (33)), such that no pulse is lost at the input even at the maximum pulse repetition rate. The trigger pulse is generated by the last tunnel diode in the chain and, in theory, the driving current may be as high as $(\underline{I_p} - \overline{I_v})$ but it was found in practice that two thirds of that value was a more realistic estimate, especially for L_s smaller than 10 or 15 μ h. Appendix A.9. lists the electrical characteristics of the tunnel diodes used, together with the guaranteed production spreads which will be accepted as the design limits (i.e. maxima and minima for worst case design). The minimum driving current for the monopulser is therefore $\underline{I_{in}} \cong \frac{2}{3}(\underline{I_p} - \overline{I_v})$ or 2 ma. Straightforward application of the remaining steps in the design procedure gives: I_a = 3.7ma ($\underline{I_a}$ = 3.2ma, $\overline{I_a}$ = 4.2ma), R_s = 22 ohms, E_s = 117mv, $\overline{L_s}$ = 10.6μh, C_{in} = 120pf. The resulting circuit is illustrated in figure 31; its performance was found to be in close agreement with the computed values. The rise and fall times of the tunnel diode monopulser, (equations (27) and (31)), were less than 10 nsec and the pulse width was 0.1μsec. At these speeds, the response time of the transistor must be taken into

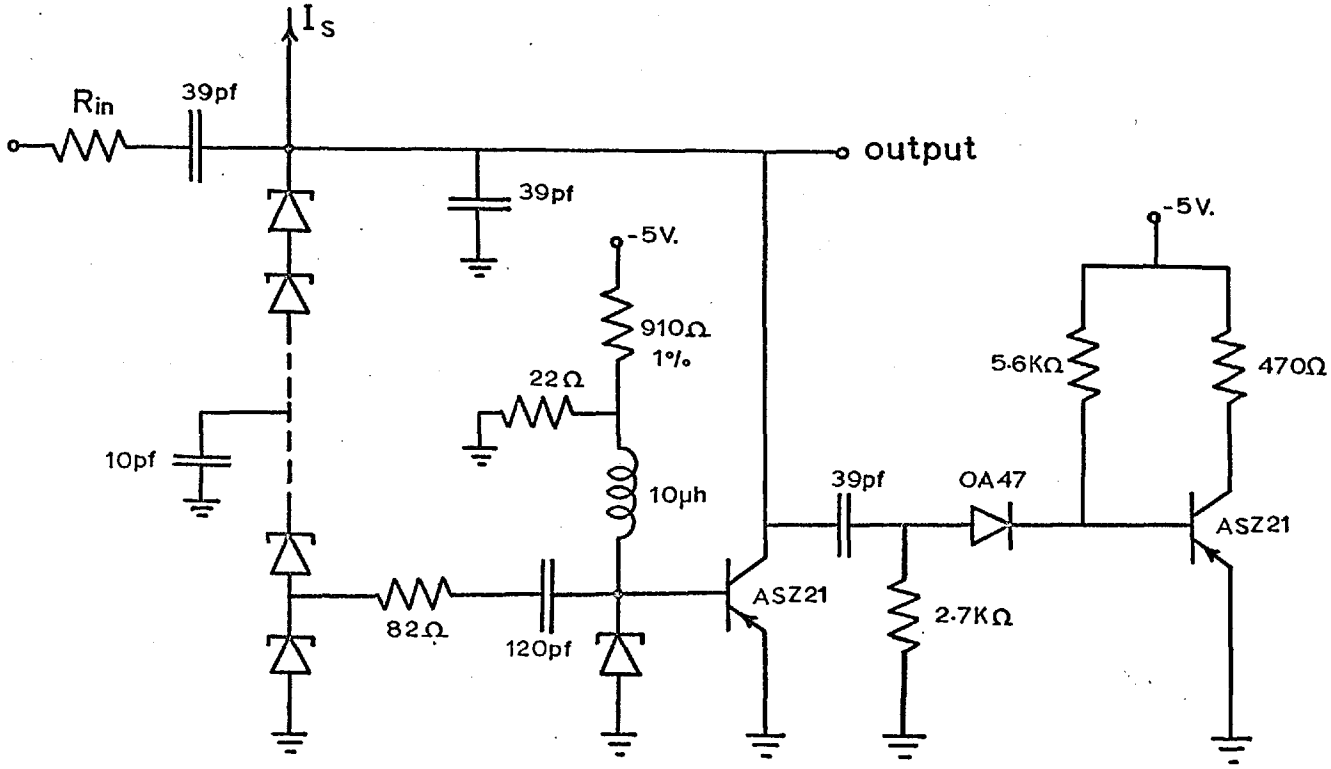

I_S
R_{in}
39pf
output
39pf
-5V.
910Ω
1%
22Ω
10pf
10μh
82Ω
120pf
ASZ21
39pf
OA47
2·7KΩ
-5V.
5·6KΩ
470Ω
ASZ21

Fig. 31.

account. The switching time of the ASZ21 transistor was computed when driven by the monopulser, and the results are given in Appendix A.10. It is seen that the total capacitance across the chain ($C_t \cong 100pf$) can be discharged and the chain reset to zero in less than 60 nsec. The transistor is over-driven in both directions by the tunnel diode and switches on and off in less than 5 and 14 nsec respectively. The total resetting time for the circuit of figure 31. is therefore computed as 0.144μsec as compared to a value of 0.11μsec measured when driven with .1μsec pulses. In order to operate the chain continuously at 10 Mc/s, the inductance, L_s, in the monopulser would have to be reduced below 10μh. The maximum value for the inductance was selected because of the fact that the first chain only is driven at 10 Mc/s when two decades or more are interconnected and ~~and~~ that the drive available from the monopulser starts to decrease when L_s is reduced below 10μh. The input staircase may be easily provided with a faster monopulser if necessary.

The addition of the two capacitances in parallel with the chain (39pf across the output and 10pf from the middle of the chain to ground, in figure 31.), increases slightly the resetting time but improves to a great extent the range of acceptable input pulse amplitudes. These capacitances reduce the possibility of triggering two or

more diodes simultaneously, as was noted in subsection 2.3.4.2., by decreasing the rate of rise of the input pulses fed to the chain. They also serve the purpose of presenting a very low impedance at the switching speed of the tunnel diodes. This situation is highly desirable as it corresponds to the case of very low impedance drive, i.e. R = 0 (see table II in section 2.3.4.). The size of these capacitors is not critical. The final choice is a compromise as the amplitude of the input signal would have to be increased if larger capacitances were used.

One more point must be considered to complete the design of the building block. Every decade must be able to drive a similar unit. Two different approaches suggested themselves. The first one requires the last tunnel diode to trigger one additional monopulser which, in turn, drives the next decade. With this approach, the question arises whether the voltage pulse generated by a tunnel diode would be large enough to trigger the chain. The most stringent condition would be met when only one tunnel diode remained in the low voltage state in which case, the necessary voltage increase across the chain is given by $\left[(\overline{V_p} - R_{d1}\underline{I_a}) + 9R_{d2}(\overline{I_p} - \underline{I_a})\right]$ or 367mv. This result is sufficient to rule out that method on the ground that almost no voltage drop (30mv in the worse case) could be tolerated across an eventual coupling network between the monopulser and the next chain.

The second approach employs one more transistor as illustrated in figure 31. The positive going step generated at the output of the chain during resetting, is differentiated by the coupling capacitance and the resulting pulse is inverted and amplified by the output transistor. The biasing conditions must be such that the transistor is still saturated in the worst case of current gain and resistor values. If the coupling capacitor is large enough, its discharge will be sufficient to cut the transistor off completely, generating a well defined pulse at the output.

2.7. Design of the Output Stage.

The DC biasing conditions must first be established and the minimum drive from the coupling capacitor to cut off the transistor in a given time can be deduced from them.

Worst case design techniques were again used and the tolerances on all resistors and on the supply voltage were taken as ±10%. The output stage, to be useful, should provide say, at least twice as much current as is available from a tunnel diode and a collector current greater than 5ma was aimed at. The upper limit for the collector resistance, R_c, is given by equation (37).

$$\overline{R_c} = \frac{\underline{V_{cc}} - \overline{V_{ce}\,(sat)}}{\underline{I_c}} \qquad .. (37)$$

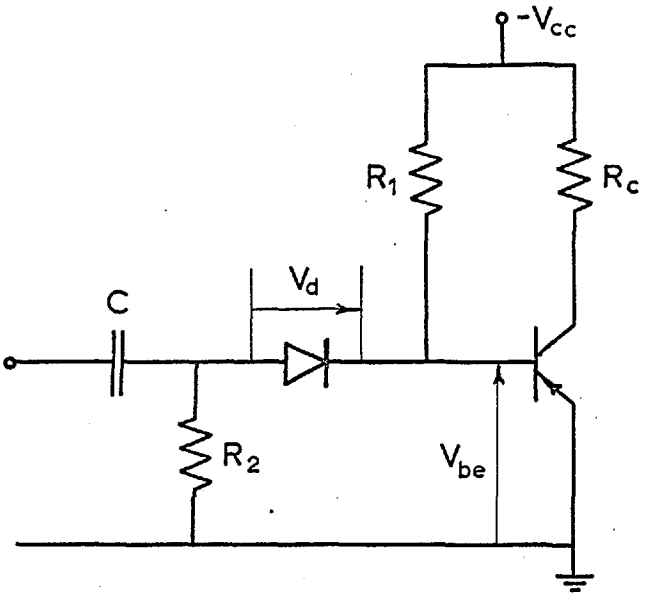
The significance of the symbols may be found in figure 32. A value of $\overline{R_c}$ = 830ohms is obtained for $\overline{V_{ce(sat)}}$ = .35v, and a nominal R_c = 470ohms ±10% is chosen in order to exceed the minimum current requirement by a safe margin. With this new value for R_c, and using worst case design equations, the limits of the collector current can be computed as $\overline{I_c}$ = 12.3ma and $\underline{I_c}$ = 8.03ma.

The minimum base current must be sufficient to keep the transistor into saturation when the maximum collector current is flowing and the current gain is at its minimum.

$$\underline{I_b} = \frac{\overline{I_c}}{\underline{\beta_o}} \qquad .. (38)$$

The minimum current gain $\underline{\beta_o}$ is now taken as 35 directly from the data sheet for the ASZ21 because the design is very conservative and estimating an additional safety factor on $\underline{\beta_o}$ beyond the specified limits would impose unnecessary requirements on other circuit parameters. Equation (38) gives a value $\underline{I_b}$ = 0.35ma.

The presence of R_2 must be taken into account before R_1 can be computed. The diode in series with the base of the transistor is kept conducting slightly by R_1 and R_2 so that the positive going step generated by the resetting process may be fed directly into the base of the



OUTPUT INVERTER

FOR STAIRCASE RESET PULSE

Fig. 32.

output transistor. The diode is needed in order to avoid undesirable loading of the negative input pulses to the chain by the low dynamic impedance of the saturated transistor. The standing current in the diode must therefore be small and a value of I_d = 0.1ma is adequate. The maximum resistance $\overline{R_2}$ is computed from equation (39).

$$\overline{R_2} = \frac{\underline{V_{be}} - \overline{V_d}}{\underline{I_d}} \qquad .. (39)$$

For $\underline{V_{be}}$ = 0.36 volt, $\overline{V_d}$ = 0.25 volt, $\underline{I_d}$ = 0.05ma, the resulting $\overline{R_2}$ is 2.2Kohms. The nominal value is chosen as R_2 = 2.7Kohms but it should be realized that this resistance is not at all critical and that it is desirable to keep it large to improve the efficiency of the coupling network.

Resistance R_1 effectively defines the base current, I_b. The minimum current through that resistance is already known: $\underline{I_{r1}} = \underline{I_b} + \overline{I_d}$ or $\underline{I_{r1}}$ = 0.45 ma. The upper limit for R_1 is then given by equation (40) and is equal to 8.94Kohms.

$$\overline{R_1} = \frac{\underline{V_{cc}} - \overline{V_{be}}}{\underline{I_{r1}}} \qquad .. (40)$$

The nominal value of R_1 can be obtained from a similar expression but the standing base current must be defined.

Taking I_b nominal, twice the minimum value obtained previously, and using $I_{r1} = I_b + I_d = 0.8$ma, a resistance R_1 equal to 5.7Kohms is found. A value of $R_1 = 5.6$Kohms $\pm 10\%$ is selected and the worst case limits for the standing base current can be obtained from equations (41) and (42).

$$\underline{I_b} = \frac{\underline{V_{cc}} - \overline{V_{be}}}{\overline{R_1}} - \frac{\overline{V_{be}} - \underline{V_d}}{\underline{R_2}} \qquad .. (41)$$

$$\overline{I_b} = \frac{\overline{V_{cc}} - \underline{V_{be}}}{\underline{R_1}} - \frac{\underline{V_{be}} - \overline{V_d}}{\overline{R_2}} \qquad .. (42)$$

With the following values: $\overline{V_{be}} = 0.44$ volt, $\underline{V_{be}} = 0.36$ volt, $\overline{V_d} = 0.25$ volt, $\underline{V_d} = 0.13$ volt, and a 10% tolerance on all other terms, the resulting limits are $\overline{I_b} = 0.983$ma and $\underline{I_b} = 0.420$ma which satisfy the requirement of equation (38).

2.7.1. Transient Response of the Output Transistor.

The amount of reverse drive needed to cut off the output transistor depends on the response time to be achieved. It has been said that the output pulse must have a 0.1μ sec width. It is therefore reasonable to expect the transistor to cut off completely in less than 25nsec. In the worst case, the collector current is at its maximum $\overline{I_c} = 12.3$ma, the base current equals $\overline{I_b} = 0.98$ma and a maximum current gain $\beta_o = 50$ is

assumed. If it is supposed that the total "switch off" time of the transistor is made up of a storage time ts = 19nsec and a turn off time tf = 6nsec, equations (A.25) and (A.26) from appendix A.10. may be transformed to find the necessary reverse current drive I_{br}. With the values listed above, the amount of reverse drive obtained from equation (A.25) is $\underline{I_{br}}$ = 1.35ma. In these conditions, the turn off time computed from equation (A.26) is tf = 4.43nsec and the above assumption is valid. The equivalent constant current drive from the capacitor C (figure 32), must therefore be greater than $\underline{I_m} = \underline{I_{br}} + \overline{I_b}$ = 1.35 + 0.98 = 2.33ma. Supposing again that the reverse current drive can be approximated by a triangle (see Appendix A.10), the peak amplitude of that triangle would have to be twice as large as the equivalent $\underline{I_m}$ or 4.7ma. It was found in Appendix A.10 that the current in the collector of the resetting transistor was $\underline{I_c}$ = 30ma. From figure 31, it can be seen that if the coupling capacitor is made equal to 39pf the peak current at the beginning of the discharge would be roughly one third of the total current $\underline{I_c}$ which would be divided between three equal capacitances. In actual fact, the discharge is much more complicated to analyse than may be thought. The presence of a negative pulse at the input of the chain when the resetting is first initiated as well as the impedances in series with the two coupling capacitances,

change the distribution of the discharge currents. Nevertheless, it was found in practice that the above approximation is adequate as the measured values of the peak current in the coupling capacitance was of the order of $I_c/3$ or 10ma. It should be remembered that as soon as the transistor cuts off, its input impedance increases sharply and the discharge current is affected.

2.7.2. Output Pulse Width.

The output pulse width is made up of the "turn off" time at the collector of the output transistor, plus the discharge time of the coupling capacitor and the "turn on" time, tr. The time, tr, may be computed from equation (A.23) of Appendix A.10. and is equal to 23.3nsec under the conditions $\overline{I_c} = -12.3$ma, $\underline{I_{bf}} = -.42$ma and $\beta_o = 50$. Both the leading and the trailing edges of the output pulse present a similar slope. The discharge time of C can be deduced from the risetime at the output of the staircase, computed in Appendix A.10. According to these results, the discharge of C would be completed in less than 60nsec and the output pulse width would be tr + tf + 60nsec or 87.73nsec. The actual measured value was 98 or 100nsec. The explanation for this significant difference can be found from a simple study of the discharge of the coupling capacitor C. As long as the output transistor is in saturation, its dynamic input impedance is low and the

capacitor is discharging rapidly. When the transistor cuts off, its input impedance increases many times and the discharge must be completed through R_1 and R_2 (figure 32.) at low current levels. This effect was neglected for the computation of the risetime at the output of the chain because the remaining charge across C when the transistor cuts off is small enough not to influence significantly the resetting of the chain. At the base of the output transistor, however, the current levels are small and the presence of that residue is not negligible. The net result is a prolongation of the effective I_{br}. No attempt was made to include this effect in the analysis as it is much simpler to readjust slightly the value of C in the circuit if necessary.

The circuit of figure 31. with a chain containing ten tunnel diodes was operated in the laboratory at a continuous pulse repetition rate as high as 10 Mc/s. The pulse generator to be described in Chapter 3, producing pulses of 30nsec duration, was used for that test. The positive equivalent of the building block, is identical to figure 31. except that the current source I_s is reversed, the tunnel diodes are all inverted and the ASZ21 are replaced by 2N797 NPN transistors.

Chapter 2 was orientated completely towards the design of a building block for the high speed stair-

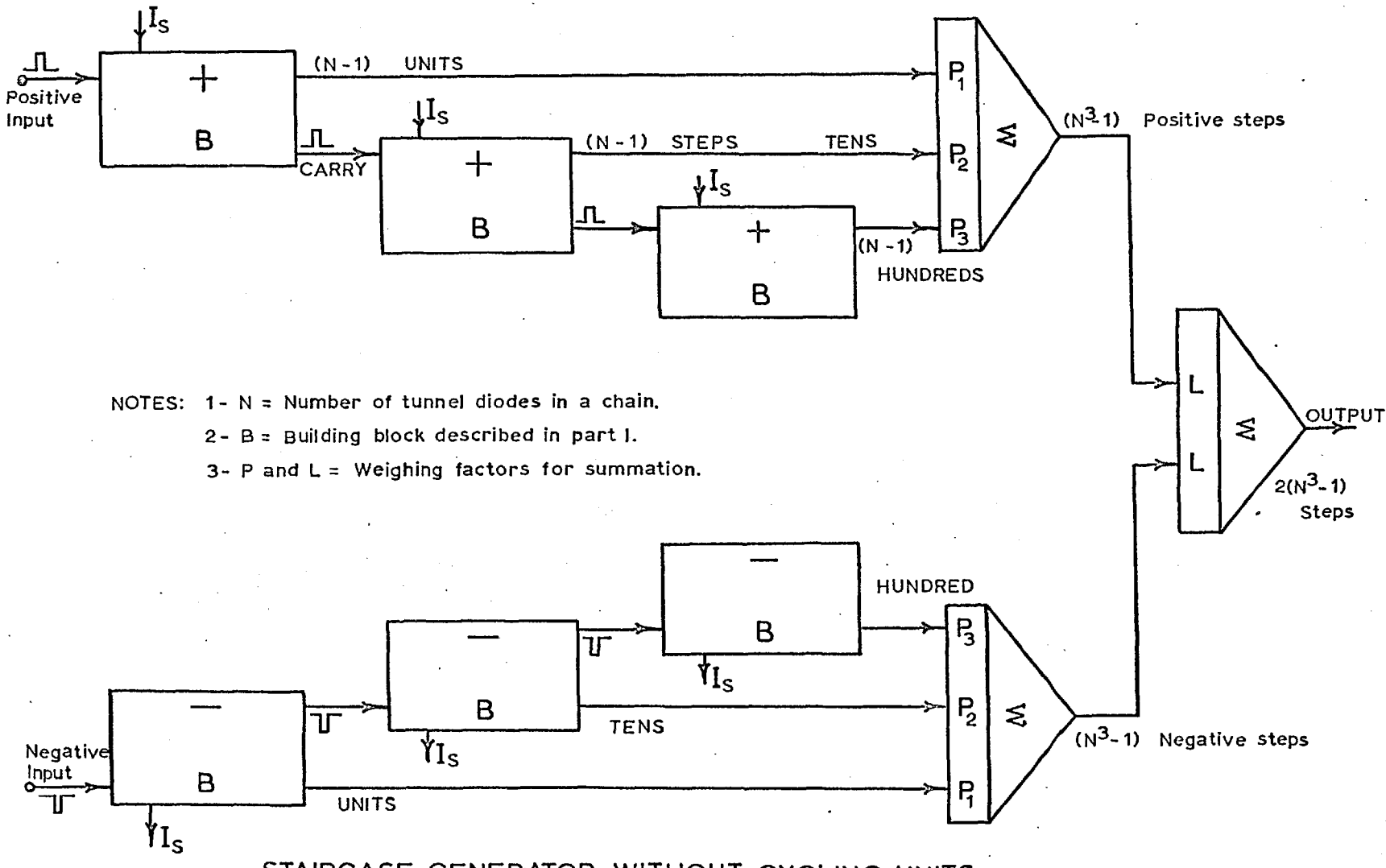
case generator. The tunnel diode was investigated at first as a switching element and a general method of analysis was developed to cover a large variety of circuits some of which will be introduced in subsequent chapters. The resulting equations were used to establish a design procedure for a type of tunnel diode monopulsers. Finally, the performance of the circuit shown in figure 31. was computed and was found adequate for the present needs. The combination of a number of these building blocks to constitute a complete staircase generator will now be considered.

C H A P T E R 3

The Complete Staircase Generator.

3.1. Basic System.

The basic method of assembling a complete staircase generator using the building block described in Chapter 2, is illustrated in figure 33. The operation of the system is self-evident and can be summarized as follows. Consider first the positive half of the generator. Three identical building blocks are connected to an output adder by weighing resistors bearing a decimal relationship. The first block represents the units and receives the positive input pulses fed into the system. The tenth pulse resets the "unit" decade to zero while stepping up the next block representing the tens. Similarly the hundreds are controlled by the resetting pulses from the previous decade. The same process occurs with pulses of the reverse polarity on the negative side of the generator. Summation of the positive and the negative waveforms produces the stepping up and down of the output. (The staircase waveforms produced respectively by two positive chains connected in cascade can be seen in figure 33.a.).



STAIRCASE GENERATOR WITHOUT CYCLING UNITS

Fig. 33.

POSITIVE CHAINS.

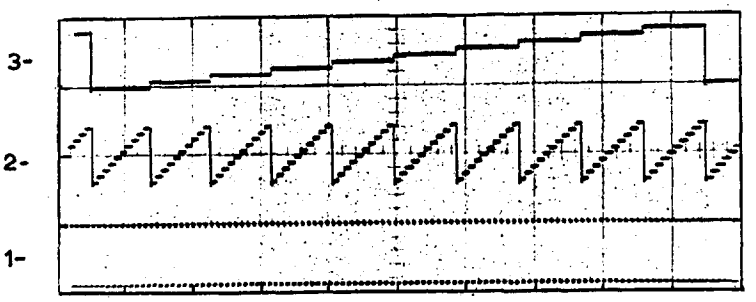


Fig. 33.a.

Traces. 1- Input pulses from a pulse generator driving the first positive chain continuously.

2- Voltage waveform appearing at the output of the first positive chain.

3- Voltage waveform appearing at the output of the second positive chain driven by the resetting action of the first one.

Scales. Horizontal: about 10μsec/cm (uncalibrated)

Vertical : Trace 1 = 2 volts/cm

Traces 2 and 3 = 5 volts/cm

Notes. 1- Input p.r.r. was about 1Mc/s.

2- Input pulse width was increased to about 0.4μsec. to improve display.

3- Unitsused during cycling process were disconnected.

4- Unless otherwise stated, the oscilloscope used for all photographs of traces was a 545A Tektronix with a Type M plug-in unit.

3.2. Precision of the Decades.

One of the requirements for the staircase generator was that it should define a large number of levels. In theory, the number of building blocks driving one another may be unlimited. In practice, however, two factors limit the number of levels: the maximum precision of the steps in any one decade and the thermal drift.

It is obvious from figure 33. that the accuracy required from every decade depends on its relative position in the system. Every tunnel diode chain possesses its own average step which should be used in the computation of the weighing resistors in order to standardize on a given average. The accuracy of the staircase generator is of prime importance as it is intended to serve as the reference unit in the quantizer. Basically, figure 33. yields sufficient information to establish the precision needed in each decade to ensure normal generation of the staircase waveform. The equality of the steps in the first decade presents no difficulties as their deviation from their average may add to almost 100% of a quantization interval without seriously increasing the total error. The steps in the second building block, on the other hand, must not deviate from their average by more than $\pm 10\%$ as every one of them must replace ten of the unit steps

within plus or minus one unity interval. Similarly, the next decade must be accurate to ±1% of the average, (case of 2000 steps), and so on.

In fact, these figures represent absolute limits and neglect such things as thermal drift and over-all deviation. These two items among others contribute to impose more severe limitations on the staircase when used as a reference unit. This problem is treated thoroughly in Part II, in connection with the study of the precision requirements for all units in the quantizer. It cannot be analysed at this stage as the influence of some auxiliary circuits in the staircase generator and the inaccuracy introduced by other units in the quantizer must be taken into account.

However, the thermal drift introduced in the staircase waveform by the tunnel diodes themselves is independent of these factors. An expression for the net thermal coefficient of the staircase generator will now be derived.

3.3. Thermal Drift.

When semiconductor devices are used to define accurately a number of voltage levels, thermal drift is normally a major problem.

Two causes of thermal drift are important in the tunnel diode for the present application. One is due to the variation of V_p and I_p with temperature and will affect the reference when one or more diodes are in the low voltage state. The other is present whenever there are diodes in the high voltage state and is given mainly by the sensitivity of V_{fp} to temperature variations. A general expression for the thermal drift at the output of the tunnel diode staircase generator of figure 33. can be derived. Remembering that a positive chain is always associated with its negative counterpart, the following terms can be defined.

N = number of tunnel diodes in a chain (positive or negative).

n = number of tunnel diodes in the high voltage state for the positive chain.

n' = number of tunnel diodes in the high voltage state for the corresponding negative chain.

$(N - n)$ = number of tunnel diodes in the low voltage state for the positive chain.

D_L = low voltage state thermal coefficient of a tunnel diode, (mv/^oC).

D_H = high voltage state thermal coefficient of a tunnel diode, (mv/^oC).

As explained before, the output of the staircase generator is the summation of the voltages from two identical stair-

cases working in opposition. The net drift is therefore the difference between the drifts introduced on each side. The contribution of one complete decade can be expressed as follows.

Net drift $/\Delta T$ = (Drift in positive staircase)

- (Drift in negative staircase)

$$\text{Net drift } /\Delta T = \left[D_H.n + D_L.(N - n)\right] - \left[D_H.n' + D_L.(N - n')\right] \quad .. (43)$$

Before equation (43) can be simplified, some more thought must be given to the nature of the coefficients D_H and D_L. The thermal sensitivity of the voltage appearing across a tunnel diode biased in the high voltage state from a constant current source, depends mainly on the combined effects of $\Delta V_{fp}/\Delta T$ and $\Delta V_v/\Delta T$. (It was shown in Appendix A.5. that the current source had a negligible temperature coefficient). For germanium tunnel diodes, these two factors are identical (reference 32, page 13). A good approximation of D_H can therefore be obtained by making it equal to $\Delta V_{fp}/\Delta T$ or $-1.0 mv/^oC$ as specified in reference 32. The forward voltage, V_{fp}, of a tunnel diode is influenced by temperature changes to a lesser extent than is the voltage drop across an ordinary germanium diode ($-2.5 mv/^oC$). It can be assumed for the present needs that the temperature coefficient, D_H, is controlled essentially by the material

used and that its variations from one diode to another in the chains are negligible.

The low voltage state temperature coefficient, D_L, depends on the combination of two thermal effects on the tunnel diode characteristic. The first one is due to the temperature coefficient of the peak voltage, $\Delta V_p / \Delta T$, and is specified as $-60 \mu V/^{\circ}C$. This coefficient may be assumed constant for all of the tunnel diodes used. The second part of D_L comes from the temperature sensitivity of the peak current. That temperature coefficient, $\Delta I_p / \Delta T$, depends on the doping level and on the resistivity of the semiconductor[32 (page 12), also 40]. The peak voltage, V_p, exhibits good correlation with the doping level and provides an indication of the temperature characteristic of the peak current. For germanium tunnel diodes manufactured by General Electric, $\Delta I_p / \Delta T$ is positive for V_p greater than approximately 60mv and it becomes negative for V_p smaller than that value. Measurements have shown that the 1N2941 tunnel diodes in hand agreed very well with the above statement.

However, a brief investigation was carried out on a small number of JK10B tunnel diodes made by S.T.C. In all cases, the temperature coefficient, $\Delta I_p / \Delta T$, was positive even for diodes with a peak voltage as low as 48mv. The magnitude of $\Delta I_p / \Delta T$ increased as expected

for larger values of V_p. It is possible that the actual levels of impurity concentrations in the materials used to make the junctions may be responsible for these differences. No special attempt was made to clarify that point as 1N2941 diodes were used throughout. A study in that direction would have been completely outside the scope of this project. The thermal drift in the staircase generator was therefore analysed considering only those units obeying the rule stated above for G.E. tunnel diodes but the results are equally valid for the S.T.C. components.

As long as V_p lies in the vicinity of 60mv, which is the typical value for the diodes used, $\Delta I_p/\Delta T$ is close to zero at room temperature and its contribution to D_L may be ignored. Even when V_p goes to some extremes like 45 or 80mv, $\Delta I_p/I_p . \Delta T$ is only of the order of $\pm 0.15\%/^oC$[32] (page 13). This effect constitutes the second part of D_L and it can be deduced from the following equations.

$$\text{Low voltage state:} \quad V_1 = \frac{0.75 V_p . I_s}{I_p} \qquad .. (44)$$

Suppose V_{11} and V_{12} represent the voltage, V_1, at temperatures T_1 and T_2, respectively; I_{p1} and I_{p2} being the peak currents at these temperatures.

$$I_{p2} = I_{p1} + \frac{\Delta I_p}{\Delta T} \cdot \Delta T \qquad .. (45)$$

$$V_{12} - V_{11} = \Delta V_1 = \frac{0.75 V_p \cdot I_s}{I_{p1}} \left[\frac{I_{p1} - I_{p2}}{I_{p2}} \right] \qquad .. (46)$$

Replacing equations (44) and (45) into equation (46), and defining the normalized temperature coefficient of the peak current, $M = \Delta I_p / I_p \cdot \Delta T$, the final expression for $\Delta V_1 / \Delta T$ may be obtained.

$$\frac{\Delta V_1}{\Delta T} = \left[\frac{-M}{1 + M \cdot \Delta T} \right] V_{11} \cong (-M) V_{11} \qquad .. (47)$$

The total temperature coefficient for the low voltage state of the tunnel diode can be found from $D_L = -60\ \mu V/^{\circ}C + (-M)V_1$. The maximum value of D_1 is therefore $\overline{D_L} = -60\ \mu V/^{\circ}C - \overline{V_1} \times 0.0015$.
But $\overline{V_1} = \overline{I_s} \times 0.75 \overline{V_p} / \underline{I_p}$ gives $\overline{V_1} = 40mv$ yielding $\overline{D_L} = -120 \mu\ V/^{\circ}C$. The actual magnitude of D_L will always be smaller than this maximum because $(-M)V_1$ will never be as high as $-60\ \mu V/^{\circ}C$ and may even become positive. Furthermore, only a fraction of $\Delta V_p / \Delta T$ influences V_1 to an extent depending on the magnitude of the standing current, I_s, through the chain.

The temperature coefficients D_H and D_L can therefore be assumed constant and equation (43) reduces to equation (48).

$$\text{Net drift } /\Delta T = (D_H - D_L).(n - n') \qquad .. (48)$$

Equation (48) represents the drift introduced by the combination of one positive and one negative chain employing the same type of tunnel diodes. However, more than one unit can be used and the output from various units are respectively attenuated or amplified, before the final summation is performed, by factors P_1, P_2 and P_3 numbered according to the increasing order of magnitude of the blocks. An expression for the total drift of the reference voltage can be deduced by repeating equation (48) as in equation (49).

$$\text{Total drift} = (D_H - D_L)\left[P_1(n_1 - n_1')\,\Delta T_1 + P_2(n_2 - n_2')\,\Delta T_2 + P_3(n_3 - n_3')\,\Delta T_3 + \ldots\right] \qquad .. (49)$$

The subscripts 1, 2, 3... refer to the first, second and third building block respectively. The scale factors are not independent of one another. If the base of the numerical system used is denoted by the letter B, the factors P_1, P_2 and P_3 can be replaced respectively by B^m, B^{m+1} and B^{m+2} where m is a positive or a negative integer depending on the number of units cascaded and on the necessity for amplification or attenuation.
Equation (49) becomes:

Total drift =

$$(D_H - D_L)\left[B^m(n_1 - n_1') \Delta T_1 + B^{m+1}(n_2 - n_2') \Delta T_2 + B^{m+2}(n_3 - n_3') \Delta T_3 + ..\right] \quad .. (50)$$

Equation (50) also leads directly to an expression for the output voltage of the staircase generator. In fact, $D_H . \Delta T$ and $D_L . \Delta T$ can be thought of as voltages representing the two possible states of the tunnel diodes. If the low and the high voltage states are called V_1 and V_2 respectively, it is sufficient to replace $(D_H - D_L)$ by $(V_2 - V_1)$ and to remove ΔT inside the bracket in equation (50) to obtain the output voltage.

Output voltage =

$$(V_2 - V_1)\left[B^m(n_1 - n_1') + B^{m+1}(n_2 - n_2') + B^{m+2}(n_3 - n_3') + ..\right] \quad .. (51)$$

Comparison of this last expression with equation (50) shows that the thermal drift in the staircase is a constant percentage of the magnitude of the output voltage if the chains are submitted to the same temperature variations. This observation is translated into mathematical form in equation (52).

$$\text{Relative drift} = \frac{(D_H - D_L) \Delta T}{(V_2 - V_1)} \quad .. (52)$$

The average step $(V_2 - V_1)$ is typically 450mv and it has been seen that $D_H = -1mv/^oC$. The maximum drift occurs when D_L is reduced to zero by a $\Delta I_p/\Delta T.I_p$ negative and equal to $-0.15\%/^oC$. In that case, equation (52) gives a relative thermal drift equal to -0.22% of the amplitude of the reference signal per degree Centigrade. This result is certainly interesting as it shows that the magnitude of the thermal drift decreases when the output voltage is close to zero. This compensation effect is limited by the "mismatch" of the temperature coefficients in opposite chains and by possible temperature differences between the chains. The thermal drift at the output of the staircase generator could also be reduced considerably by adequate temperature control of the tunnel diodes.

The temperature coefficients of the four chains described in Appendix A.7. were measured and the results are tabulated in Appendix A.8. An experimental value of $-0.23\%/^oC$ was obtained for the relative thermal drift of the reference unit. Remembering that the compensation was assumed to be 100% efficient for the derivation of equation (52), the experimental results demonstrate the usefulness of that expression. For very small output voltages, the mismatch between the thermal coefficients of opposite chains contribute to increase slightly the net relative drift. A complete analysis of the results can

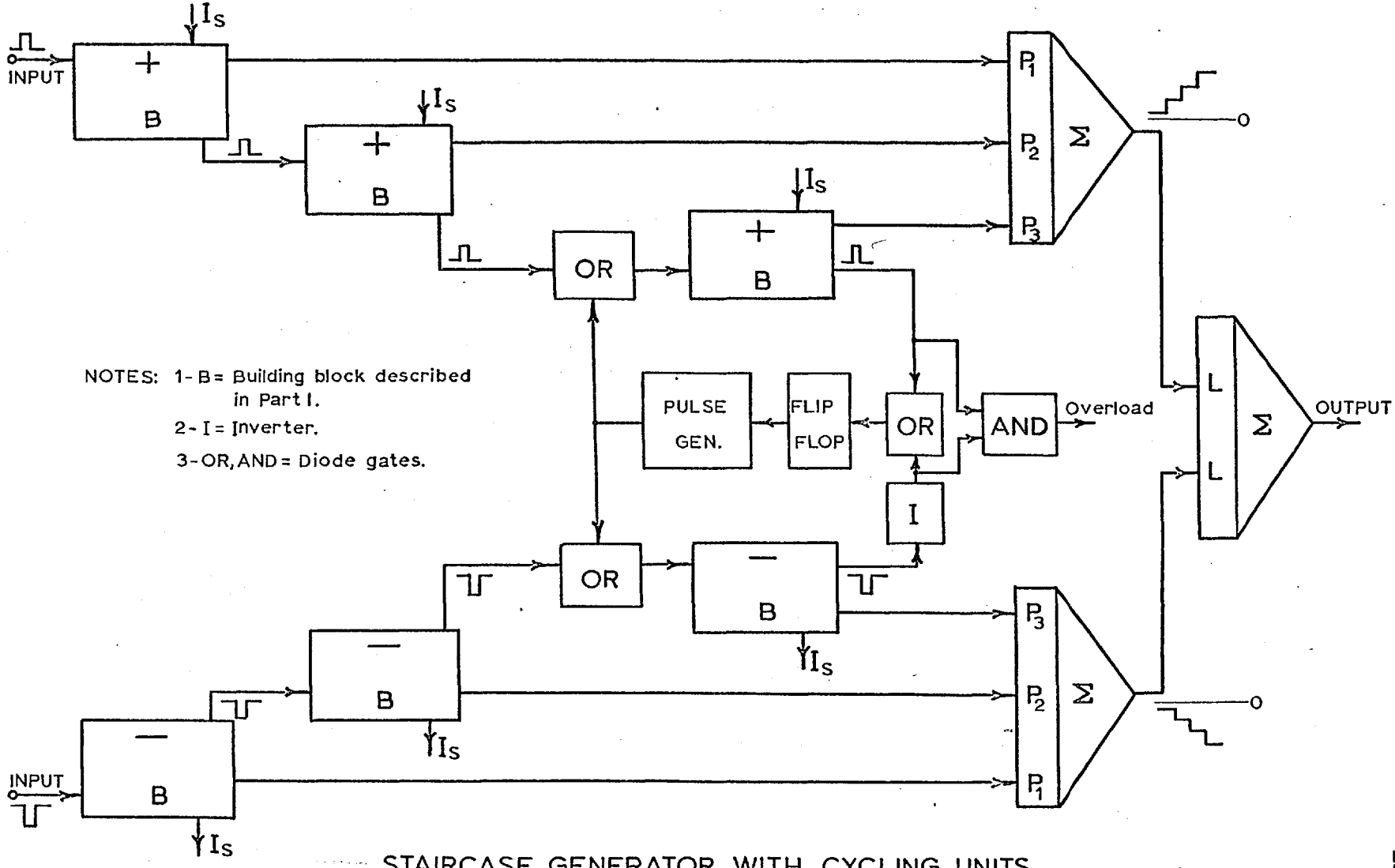
be found in Appendix A.8.

Up to this point, the tunnel diode staircase generator was shown to offer the accuracy and the high speed of operation required by the stepping reference of the quantizer. One more problem remains to be solved: the control of the step generating units to permit uninterrupted operation.

3.4. High Speed Cycling Process.

The operation of the staircase generator was described in section 3.1. Under normal conditions, the number of tunnel diodes in the high voltage state increases gradually in the chains of either polarities as pulses arrive at the input. A point is reached, however, where one side overloads and resets completely to zero. At that moment, a large discontinuity would appear at the output unless some action were taken. This undesirable effect can be avoided if the overloading initiates a "cycling" process where the contents of the two sides are subtracted from one another.

The proposed method of cycling permits uninterrupted operation at the input and leaves unchanged the maximum pulse repetition rate of the staircase. Figure 34. represents the complete staircase generator



STAIRCASE GENERATOR WITH CYCLING UNITS

Fig. 34.

together with the control units. The subtraction is carried out only between the blocks representing the most significant figure. The operation is performed as follows. The overloading side resets to zero and triggers a high speed pulse generator which starts stepping up both sides of the highest order unit at the same time. The pulse generator is then stopped by the first overload pulse coming from either side. If both chains were initially at zero, the positive and the negative blocks overload together, indicating that the full scale output has been attained. Part of the dynamic range can be lost in that fashion as the contents of the lower units are not taken into account but it will be seen that the advantages of the technique overshadow this minor drawback. If, on the other hand, the second side was not at the zero level, this block overloads first and resets to zero, stopping the cycling process. The number of pulses received by the first block is then equal to the difference between the maximum content of a chain (10 in the present case) and the number of diodes in the high voltage state in the second chain when cycling was initiated.

If, for example, three decades are being used, an overload of the positive side would indicate a positive level equivalent to +1000 steps. If the negative staircase reads -955, for instance, the desired output would be

+1000 -955 = +45 steps. After cycling, by the method described above, the chains would reset respectively to +100 and -55 producing an output equal to +45.

3.4.1. Influence of the Cycling Process on the Speed of Operation.

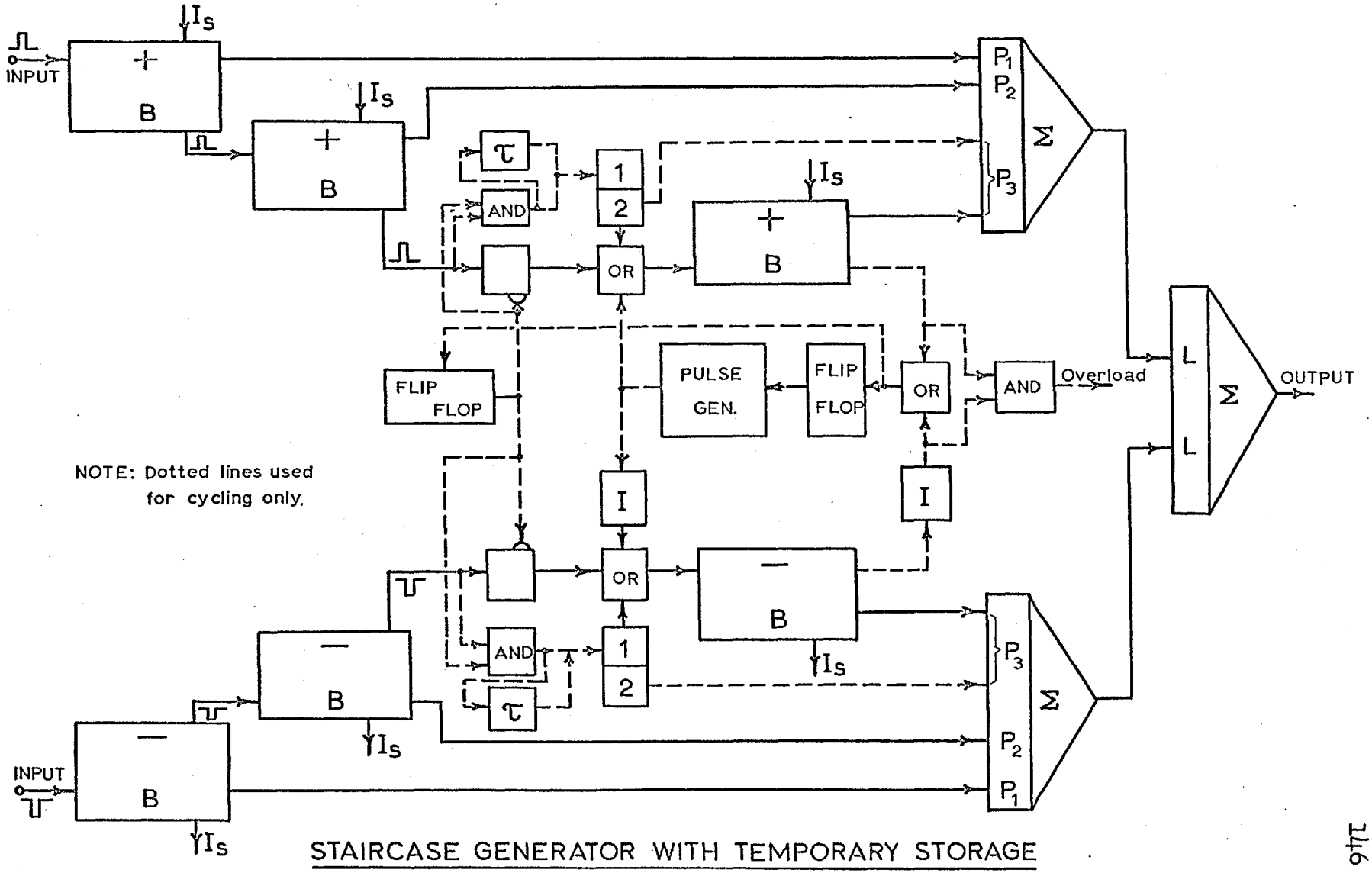
In order to take full advantage of the proposed cycling technique, a temporary storage must be incorporated within the system.

It was pointed out, during the qualitative description of the cycling process, that the pulse generator may be required to feed a maximum of ten pulses into the last decades for the case of a complete overload. During that time, no carry pulse may be accepted from the lower units. This is to say that unless something is done about it, the minimum spacing between two consecutive input pulses of opposite polarities, must be at least equal to ten times the period of the pulse generator used for cycling. If the cycling is done at the maximum pulse repetition rate acceptable by the building blocks, the speed at the input is still limited to one tenth of its possible maximum. It is important to note, however, that the minimum spacing between input pulses of the same polarity is not affected by that restriction. For some applications, this may be most significant. For the case of the proposed quantizer, for instance, it means that the maximum slope, ($\Delta V/\Delta T$),

acceptable at the input is computed assuming operation of the staircase at its maximum pulse repetition rate. On the other hand, the transition from a positive rate of rise ($\Delta V/\Delta t$) at the input of the quantizer to a negative one and vice versa, must be sufficiently gradual so that the minimum spacing between the last positive pulse and the first negative one meets the above requirement. The implications of this last statement will be clarified in a further study of the quantizer.

3.4.2. Temporary Storage.

The restriction is not inherent to the system itself and it may be removed if an auxiliary loop is included, as in figure 35, to store any carry pulse coming from the lower units during the cycling of the last blocks. When the cycling process is initiated, a flip flop inhibits the normal inputs to the last blocks and opens a gate to the temporary storage unit. This latter unit is identical to the standard building block of Chapter 2, except that it contains only two tunnel diodes in the chain. If a carry pulse arrives at the gate during the cycling, it is fed simultaneously to a time delay circuit and to the unit just described switching on the first tunnel diode. The delay may be produced by a simple tunnel diode circuit containing two monopulsers. The carry pulse resets the temporary storage unit after



STAIRCASE GENERATOR WITH TEMPORARY STORAGE

Fig. 35.

a time controlled by the delay circuit (longer than ten periods of the pulse generator). The resetting of the two-tunnel diode chain finally transfers the carry to the corresponding decade after the cycling is completed.

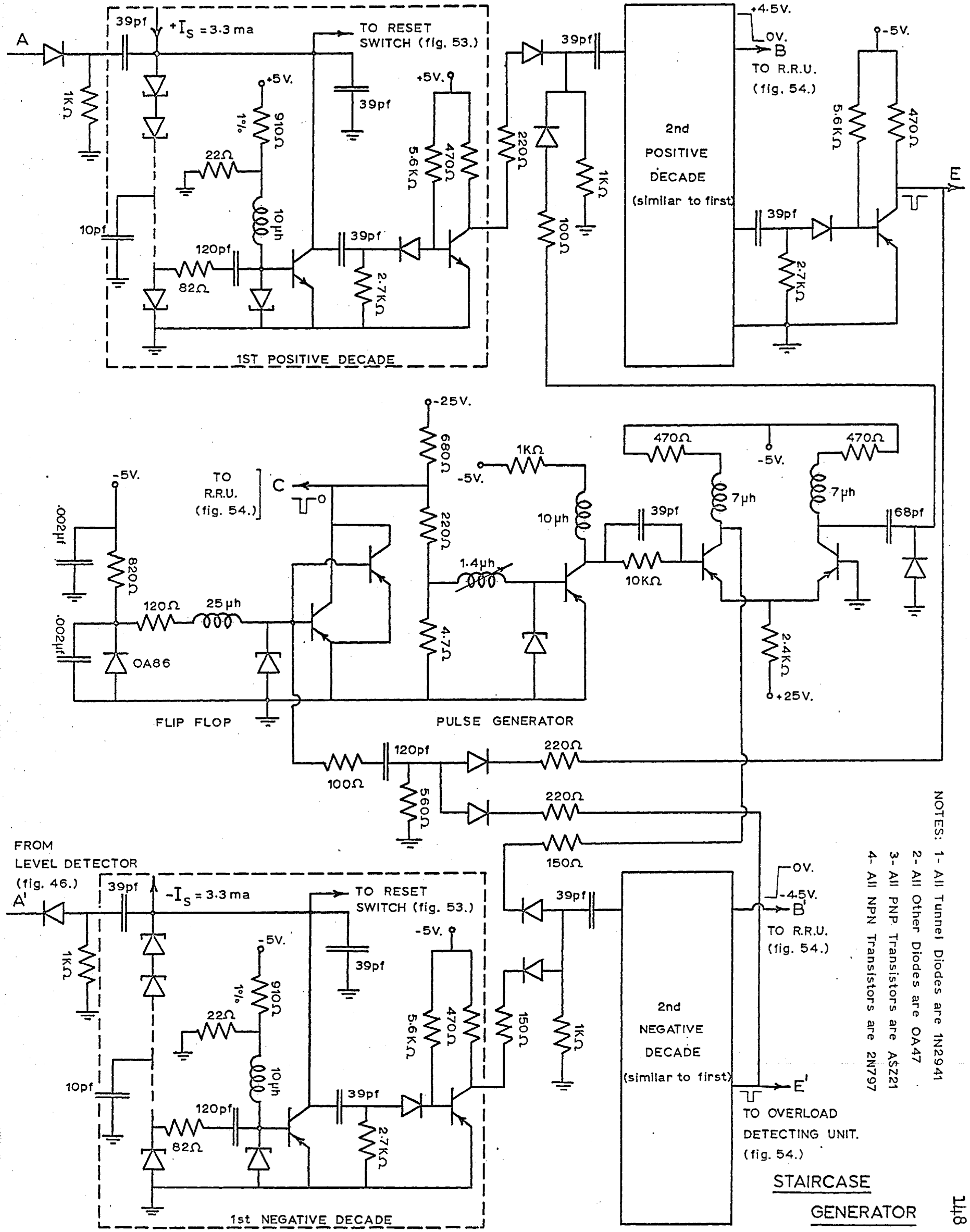
A simplified version of the staircase generator employing only two decades, i.e. ± 100 steps, has been built and tested in the laboratory. The "cycling" pulse generator operates at 10 Mc/s and no temporary storage facilities are provided in the prototype. The maximum pulse repetition rate on any one side is consequently limited to just under 10 Mc/s and the minimum spacing between pulses of opposite polarities must be greater than 1 μsec. The design of the control circuits achieving this performance will be outlined briefly.

3.5. Design of Control Circuits.

All of the following circuits are illustrated in figure 36.

3.5.1. Pulse Generator.

The complete analysis of the tunnel diode relaxation oscillator was carried out in section 2.5. Equation (35), derived in section 2.6.1., for the design of the tunnel diode monopulser still applies but the constants K_1 and K_2 must be altered according to the



NOTES: 1- All Tunnel Diodes are 1N2941
2- All Other Diodes are OA47
3- All PNP Transistors are AS221
4- All NPN Transistors are 2N797

Fig. 36.

different conditions. For convenience, equation (35) is reproduced below together with the new expressions for K_1 and K_2.

$$L_s = \frac{T - CK_3}{K_1 + K_2} \qquad .. (35)$$

where $$K_1 = \frac{1}{R_{t1}} \ln \left[\frac{E_s - R_{t1} I_v}{E_s - R_{t1} I_p} \right]$$

$$K_2 = \frac{1}{R_{t2}} \ln \left[\frac{E_s - V_{tr} - R_{t2} I_p}{E_s - V_{tr} - R_{t2} I_v} \right]$$

$$K_3 = \frac{V_{fp} + V_v - V_p - V_1}{I_p - I_v}$$

For the description of the various terms, see section 2.6. The series resistance, R_s = 4.7ohms, was chosen much smaller than the negative resistance of the tunnel diode in order to improve the d.c. stability. The pulse repetition rate of the tunnel diode relaxation oscillator depends to a certain extent on the operating point and the larger R_s, the more sensitive the circuit is to changes in E_s and to temperature variations. A source voltage, E_s = 150mv, is chosen such that the tunnel diode is biased approximately in the region of maximum negative resistance. For a 0.1 μsec period and with all other terms as defined in Chapter 2, the inductance L_s is computed from

equation (35) as 1.4 μh. Adjustment of the pulse repetition rate is made with the aid of a movable slug in the inductance.

As for the monopulser, the tunnel diode relaxation oscillator was connected to the input of a common-emitter transistor. Computation of the transient response of this booster stage is similar to that of the resetting transistor given in Appendix A.10., and will not be reproduced here. Only one point will be mentioned. The pulse width from the 10Mc/s oscillator, if computed from equations(27), (30) and (31), is found to be less than 35nsec (see Figures 37 and 38). The tunnel diode itself stays in the high voltage state for only 20nsec. It is therefore necessary to reconsider the choice of the equivalent forward base current applied to the transistor. The pulse width being almost three times narrower than for the case of the monopulser, I_{bf} = 2ma/3 or 0.7ma was selected for the computations.

The 10Mc/s pulse generator must drive simultaneously a positive and a negative chain. A long tailed pair amplifier was designed for that purpose. Peaking inductances and d.c. coupling were used for the booster stage and the amplifier in order to obtain pulses of equal amplitudes as soon as the 10Mc/s pulse generator was

SWITCHING TRANSIENTS FOR A TUNNEL DIODE

RELAXATION OSCILLATOR

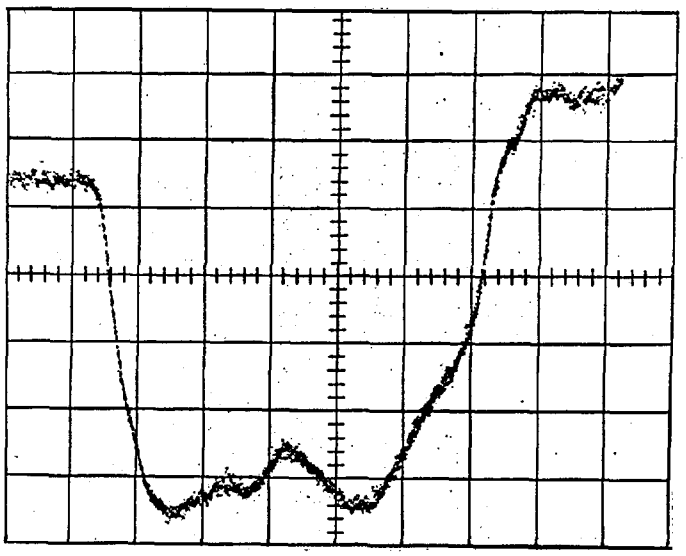


Fig. 37.

Trace. Voltage waveform appearing across the tunnel diode in the 10Mc/s relaxation oscillator for one pulse duration.

Scales. Horizontal: 5 nsec/cm

Vertical : about 80mv/cm (uncalibrated)

Notes. 1- The transistor normally loading the tunnel diode was removed.

2- Sampling Oscilloscope - Tektronix Type 564.
Plug-in units - Sampling Sweep Type 3T77
and Sampling Dual-Trace Type 3S76.

3- See also figure 38.

PULSES ACROSS THE TUNNEL DIODE IN THE 10Mc/s RELAXATION OSCILLATOR

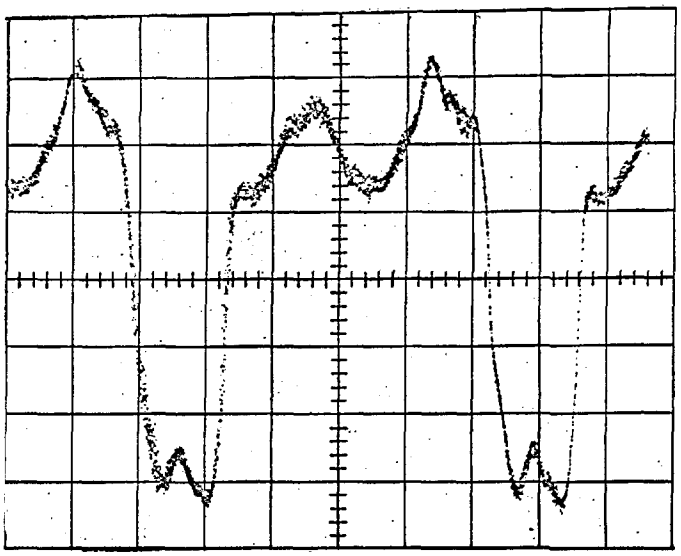


Fig. 38.

Trace. Voltage waveform appearing across the tunnel diode in the 10Mc/s relaxation oscillator for the duration of two pulses.

Scales. Horizontal: 20nsec/cm

Vertical : about 80mv/cm (uncalibrated)

Notes. 1- Same conditions as for figure 37.

2- Sampling Oscilloscope - see Note 2 in figure 37.

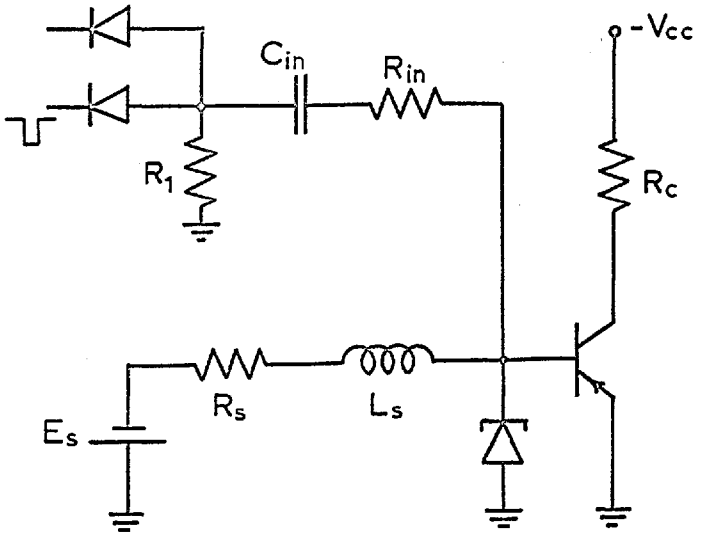
switched on. One of the transistors is normally cut off while the other is ~~kept into~~ held in saturation by the current defined in the emitter resistor. The positive pulses from the booster stage switch the current between the two transistors, generating pulses of opposite polarities at the collectors. The actual design of the amplifier is a straightforward application of well known circuit techniques and presents no special interest. The voltage pulses appearing at the output of the amplifier, when driven from the 10Mc/s pulse generator via the booster stage, were displayed on a sampling oscilloscope. The amplifier was driving the chain normally and risetimes of less than 30nsec were measured at the collectors.

3.5.2. <u>One Tunnel Diode Flip Flop</u>.

The 10 Mc/s pulse generator must be switched on and off within less than 0.1 μsec whenever the cycling process requires only one pulse. For a two-decade staircase, the pulse generator may be expected to operate again within 0.9 μsec after the "switch off" action was initiated. This time is increased to 9 μsec for a three-decade staircase generator. The bistable circuit controlling the pulse generator must therefore be ready to switch off less than 0.1 μsec after being switched on and its recovery time must then be less than 0.9 μsec. A one-tunnel diode flip flop, operating on the same

principle as the monopulser of section 2.6., has been designed to meet these requirements.

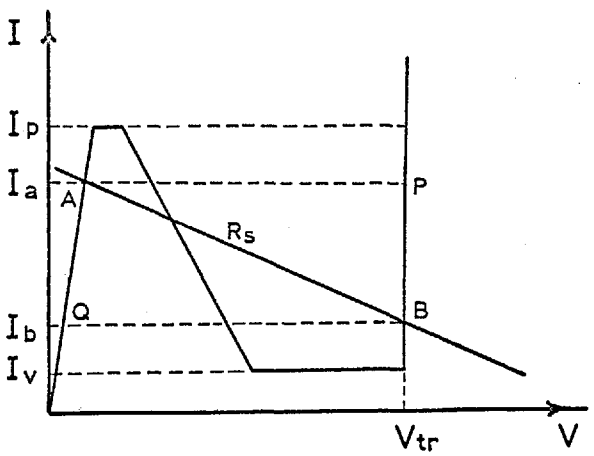
The operation of the one-tunnel diode flip flop of Figure 39. is very similar to that of the monopulser and can be explained from the characteristic of Figure 40. The tunnel diode is biased such that the source resistance intersects its characteristic at two stable points A and B. Initially, the tunnel diode is at point B. When the first negative pulse is applied to the input gate, the coupling capacitor C_{in} charges up rapidly, increasing temporarily the base current of the transistor. No effect is detected at the output as the transistor is already in saturation. For the remaining of the input pulse, C_{in} has already charged up and a negative voltage is maintained across the resistance R_1 (Figure 39.), by the conduction through the input diode. At the end of the input signal, the diode in the OR gate cuts off and C_{in} must discharge through R_1 and R_{in}, lowering the current in the tunnel diode below the valley point. The switching from point B to point A proceeds exactly as explained for the monopulser and the transistor cuts off rapidly. The delay introduced by the input pulse width before the flip flop switches on, is useful in the present application as it gives some time to the chain to reset completely before the 10 Mc/s pulse generator



TUNNEL DIODE

FLIP FLOP

Fig. 39.



ELECTRICAL

CHARACTERISTIC

Fig. 40.

starts to operate. As soon as another pulse of the same polarity arrives at the input gate, the charging up of the capacitor C_{in} by the leading edge of the pulse, increases the current in the tunnel diode and switches it to the high voltage state. The input pulse must be narrow compared to the time taken by the current to decrease from point P to point B (Figure 40.), otherwise, the discharge of C_{in} would switch the flip flop back to point A. It will be seen later on that R_1 can be adjusted such that the peak of the discharge current through C_{in} is smaller than the charging current, thus permitting the use of a larger input pulse duration and easing the design requirements.

3.5.2.1. Analysis of the One-Tunnel Diode Flip Flop.

The analysis carried out in section 2.6. for the monopulser applies almost exactly to the one-tunnel diode flip flop. The presence of a stable point in the high voltage region is taken into account in the same manner as was done for point A in equations (33) and (34). The resulting equations will now be listed.

1. Switching from point B to point A: (use figure 40.)

From V_v to point Q: equation (31) applies.
From point Q to point A: equation (34) can be used if I_v is replaced by I_b, where I_b is equal to the current at point B.

2. Switching from point A to point B:

From V_p to point P: equation (27) still holds.
See related remark in section 2.5.2.
From point P to point B:

$$t_{P-B} = \tau_2 \ln \left[\frac{I_a - I_b}{m.I_b}\right] \qquad .. (53)$$

where $\tau_2 = L_s/R_{t2}$

$R_{t2} = R_s + R_{d2}$ $(R_{d2} \cong 0)$

m = fraction of I_b representing the difference from I_b of the current in the inductance L_s at time t_{P-B}.

The choice of m will be determined by some design parameters to be considered later on.

3.5.2.2. Design of the One-Tunnel Diode Flip Flop.

The design procedure outlined in section 2.6.2., for the moncpulser must be altered slightly before it can be applied to the one-tunnel diode flip flop. The establishment of the design limits for the trigger current must be done carefully if a worst case technique is to be used. The following equations will serve to set these limits and to decide the choice of the operating points A and B.

Definitions: (use Figure 40).

I_a = current at point A

I_b = current at point B

$I_{in\ a}$ = input trigger current produced by the leading edge of the input pulse during the charging up of C_{in}. (Figure 40).

$I_{in\ b}$ = input trigger current produced at the trailing edge of the input pulse by the discharge of C_{in}.

Limits of I_a:

$$\underline{I_a} = \overline{I_p} - \underline{I_{in\ a}} \qquad .. (54)$$

$$\overline{I_a} = \underline{I_p} \qquad .. (55)$$

Limits of I_b:

$$\underline{I_b} = \overline{I_v} \qquad .. (56)$$

$$\overline{I_b} = \underline{I_{in\ b}} + \underline{I_v} \qquad .. (57)$$

Limits of $I_{in\ a}$:

$$\underline{I_{in\ a}} = \overline{I_p} - \underline{I_a} \qquad .. (54)$$

$$\overline{I_{in\ a}} = \text{depends on } \overline{I_{in\ b}}$$

Limits of $I_{in\ b}$:

$$\underline{I_{in\ b}} = \overline{I_b} - \underline{I_v} \qquad .. (57)$$

$$\overline{I_{in\ b}} = \underline{I_a} - \overline{I_v} \qquad .. (58)$$

By definition:

$$I_{in\ b} = k_2 I_{in\ a} \qquad .. (59)$$

There are six independent equations and eight unknowns. Some other circuit considerations must be used to derive two

more equations. A very useful expression may be obtained if the constant k_2 from equation (59) is expressed as a function of "$I_{in\ a}$" only. It is done by replacing $\underline{I_a}$ from equation (54) in equation (58) and using the result in equation (59).

$$\overline{k_2} = \frac{\overline{I_p} - \overline{I_v} - \underline{I_{in\ a}}}{\overline{I_{in\ a}}} \qquad .. (60)$$

A lower limit for k_2 can also be found by noting from equations(56) and (57) that $\underline{I_{in\ b}}$ cannot be chosen arbitrarily small as at the limit:

$$\overline{I_b} = \underline{I_b} = \overline{I_v} \quad \text{when} \quad \underline{I_{in\ b}} = \overline{I_v} - \underline{I_v} \qquad .. (61)$$

For similar reasons, the absolute lower limit for "$I_{in\ a}$" can be expressed as in equation (62) which is deduced from equations (54) and (55).

$$\underline{I_{in\ a}} = \overline{I_p} - \underline{I_p} \qquad .. (62)$$

Combining equations (61) and (62) with equation (59) gives the expression for the lower limit of k_2.

$$\underline{k_2} = \frac{\overline{I_v} - \underline{I_v}}{\overline{I_p} - \underline{I_p}} \qquad .. (63)$$

Equations (54) to (63) are sufficient to establish from known data the design limits regarding the choice of the

operating points and the range of input pulse amplitudes for the one-tunnel diode flip flop.

One more equation must be derived before the design procedure can be outlined. From equations (31) and (34) or from equations (27) and (53), the maximum value of inductance, L_s, can be expressed as in equation (64).

$$\overline{L_s} = \frac{T - CK_2}{K_1} \qquad .. (64)$$

If T, in equation (64), is defined as the minimum time interval between switch on (from B to A) and switch off (from A to B) pulses, the other terms are given by equations (65) and (66).

T = maximum permissible switching time from point B to point A.

$$K_2 = \frac{V_v - R_{d1} I_b}{\overline{I_p} + I_{inb} - I_b} \qquad .. (65)$$

$$K_1 = \frac{1}{R_{t1}} \ln \left[\frac{E_s - R_{t1} I_b}{E_s - R_{t1} n . I_a} \right] \qquad .. (66)$$

$$\underline{n} = \frac{\overline{I_p} - \underline{I_{in\ a}}}{I_a} \qquad .. (67)$$

Note: $\underline{n}$ is computed from the maximum distance that the current in the inductance may be from point A when the next input pulse arrives.

If, on the contrary, T is defined as the minimum time interval between switch off (from A to B) and switch on (from B to A) pulses, K_2 and K_1 are given by equations (68) and (69).

T = maximum permissible switching time from point A to point B.

$$K_2 = \frac{V_{fp} - V_p}{I_{ina} + I_a - I_v} \qquad .. (68)$$

$$K_1 = \frac{1}{R_{t2}} \ln \left[\frac{I_a - I_b}{m . I_b} \right] \qquad .. (69)$$

$$\bar{m} = \frac{\underline{I_{in\ b}} + \underline{I_v} - \overline{I_b}}{I_b} \qquad .. (70)$$

Note: m represents the relative difference of the current in the inductance from point B on arrival of the input pulse.

It is important to remember that the values of $\underline{I_{in\ a}}$ and $\underline{I_{in\ b}}$ in equations (67) and (70) must be the values calculated from the actual circuit tolerances and not the absolute limits set by equations (61) and (62). If the circuit tolerances are controlled carefully, say to ± 5% for instance, advantages may be taken of the factors n and m in equations (66) and (69) and larger values of the inductance, L_s, can be chosen for the same speed of operation of the flip flop, permitting the use of greater input pulse widths.

The most favorable conditions for the operation of the one-tunnel diode flip flop will be met when the input pulse width is much shorter than the time constant introduced by the presence of L_s. In any case, it will be seen that the tolerances required for a worst case design can be satisfied easily.

3.5.2.3. Summary of Design Procedure.

1. Choose k_2 slightly greater than the value given by equation (63).

2. Select $I_{in\ a}$ about twice the absolute minimum given by equation (62).

3. From equations (54) to (59), establish the design limits for I_a, I_b, $I_{in\ a}$ and $I_{in\ b}$.

4. From the results of step 3, chose I_a and I_b half way between the design limits and compute their tolerances from these same limits.

5. Compute R_s joining point A to point B and determine the corresponding E_s.

6. From a knowledge of the minimum spacing between two input pulses, and using equation (64), find the maximum L_s.

7. The input coupling capacitance, C_{in}, is not critical and is chosen approximately equal to three times the capacitance of the tunnel diode.

8. Adjust R_{in} and R_1 to obtain "$I_{in\ a}$" and k_2 as chosen in step 1 and 2, taking into account the magnitude of the input pulse and the output impedance of the generator.

3.5.2.4. Practical Design and Performance.

An example of a one-tunnel diode flip flop is illustrated in Figure 36. The actual worst case design of the circuit required an input pulse width of less than 25nsec with a value of $L_s \leq 10\mu h$ if the flip flop is to switch on and off reliably within 0.1μsec. The output pulses from the inverters of the last decades have been designed to have a 0.1μsec width and a flip flop using $L_s = 10\mu h$ would always be reset to point A by the trailing edge of these large pulses. It was pointed out before that as long as the tolerance on the input signal was kept within certain limits, a larger value of L_s could be used, permitting an increase in the maximum input pulse width. This approach was used in the circuit of Figure 36., and L_s was increased to 25μh. The cycling can be carried out at 10 Mc/s and, in the worst case, only one pulse is let through before the flip flop switches the pulse generator

off again. It should be remembered that the restriction on the pulse width is not imposed directly by the minimum time interval between the switching on and the switching off because the flip flop is triggered "on" by the trailing edge of the first pulse. The consequently smaller value of L_s when this time is decreased, however, necessitates closer tolerances on the input pulse amplitude if the pulse width is not reduced, because of the greater tendency for the circuit to trigger back to point A at the end of the "switch off" pulse. This is due to the fact that the decay of the current from point P to point B (Figure 40), is proportional to L_s.

In the present case, the 1% resistors in series with the diodes in the OR gate driving the flip flop, were adjusted experimentally to obtain the same drive from both sides. If the input pulse width were reduced to 25nsec, the tolerances on I_a, I_b and "$I_{in\ a}$" would be eased considerably and are listed below.

$$I_a = 3.7\text{ma} \pm 10\%$$

$$I_b = 1.4\text{ma} \pm 20\%$$

$$I_{in\ a} = 2.5\text{ma} \pm 20\%$$

It can be seen that the one-tunnel diode flip flop presents numerous points of interest some of which are the great

simplicity, the potentially high pulse repetition rate and the normal response of the circuit to pulses of either polarities.

The transient response of the output transistor of the flip flop is similar to that of the resetting transistor. Two transistors had to be used in parallel because the collector standing current when the flip flop is off, is about 30ma which is the absolute maximum for the ASZ21. The current available from the tunnel diode is perfectly adequate to drive the two transistors in or out of saturation in less than 30nsec. The risetime at the collectors is approximately 20nsec (see Figure 41).

In order to illustrate the action of the flip flop during the cycling process, a series of photographs of oscilloscope displays were taken (Figures 42, 43, and 44). The conditions prevailing for each of these photographs are described in the figures themselves. Both sides of the staircase generator arrangement shown in Figure 34, were driven by continuous trains of pulses of corresponding polarities. A time delay of half a period was introduced between the two trains of pulses such that both sides could not overload simultaneously. In this way, the full range of possible cycling conditions can be illustrated depending on the initial states of the chains which can be altered easily. Figure 42 shows, as an example, the negative side

RISETIME AT THE COLLECTOR OF THE ONE-TUNNEL DIODE FLIP FLOP

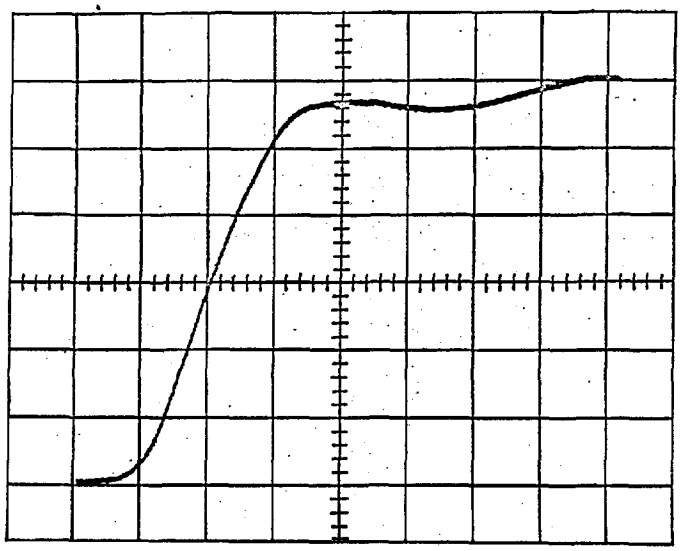


Fig. 41.

Trace. Risetime of the voltage waveform seen at the collector of the one-tunnel diode flip flop (see fig. 36.) at the end of the cycling operation.

Scales. Horizontal: 10 nsec/cm

Vertical : about 0.8 volt/cm (uncalibrated)

Notes. 1- Complete waveform appearing at the same point can be seen in figure 44.

2- Sampling Oscilloscope - see Note 2 in figure 37.

THE CYCLING OPERATION IN THE STAIRCASE GENERATOR

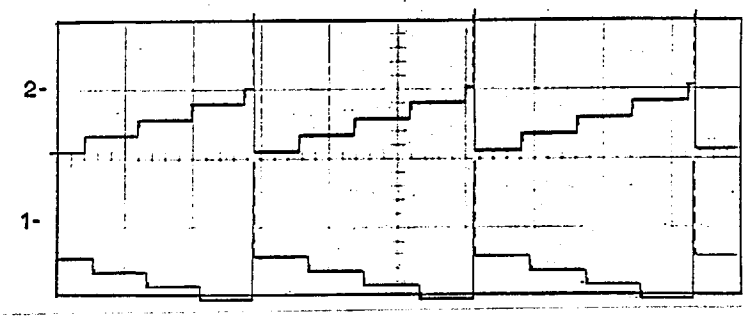


Fig. 42.

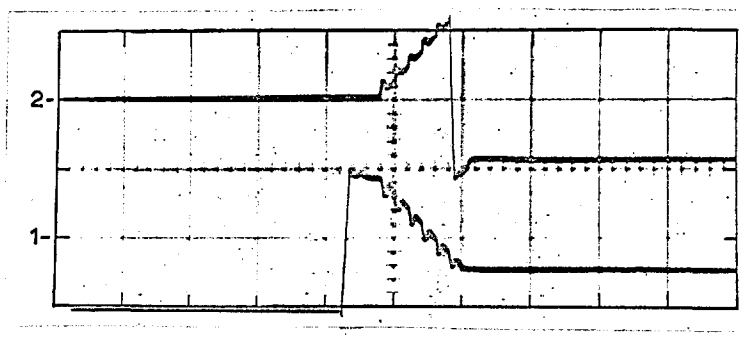


Fig. 43.

Traces. 1- Voltage waveform appearing across the second negative decade. (Rapid transients had to be drawn in ink to improve reproduction)

2- Same as trace 1 but for the positive second decade.

Scales. Horizontal: 50μsec/cm (fig. 42.)

0.5μsec/cm (fig. 43.)

Vertical : 2 volts/cm (both traces on both figures

Notes. 1- See end of section 3.5.2.4. for description of prevailing conditions.

2- Compare to figure 44.

3- Negative side overloading first.

DETAILS OF CYCLING OPERATION

IN STAIRCASE GENERATOR

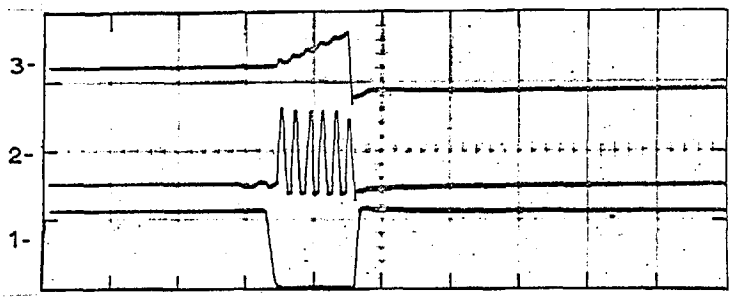


Fig. 44.

Traces. 1- Voltage waveform at the collector of the one-tunnel diode flip flop during the cycling process.

2- Positive pulses, (driving the positive decade), seen at one collector of the 10Mc/s pulse amplifier during the cycling process.

3- Voltage waveform across the second positive decade during the cycling operation.

Scales. Horizontal: 0.5μsec/cm

Vertical : Traces 1 and 3 = 5 volts/cm

Trace 2 = 2 volts/cm

Notes. 1- Same conditions as in figures 42. and 43.

2- Details of trace 1 given in figure 41.

overloading after the corresponding positive chain has reached the fourth level. The cycling process resets the positive decade to zero and returns the negative one to the sixth level. Details of this cycling operation are given in Figures 43 and 44 for clarity.

The staircase generator described thus far (Chapters 2 and 3), was shown to offer many advantageous features including high speed of operation and circuit simplicity. As a pulse counter or a scaler, for instance, it could be of considerable value in a number of applications. However, it was designed to serve as the main reference level generator in a quantizer (Chapter 1). The next part of the thesis will be concerned with the problems related to the ulilization of this stepping reference generator in a complete A-D converter of the type proposed in Chapter 1.

P A R T II

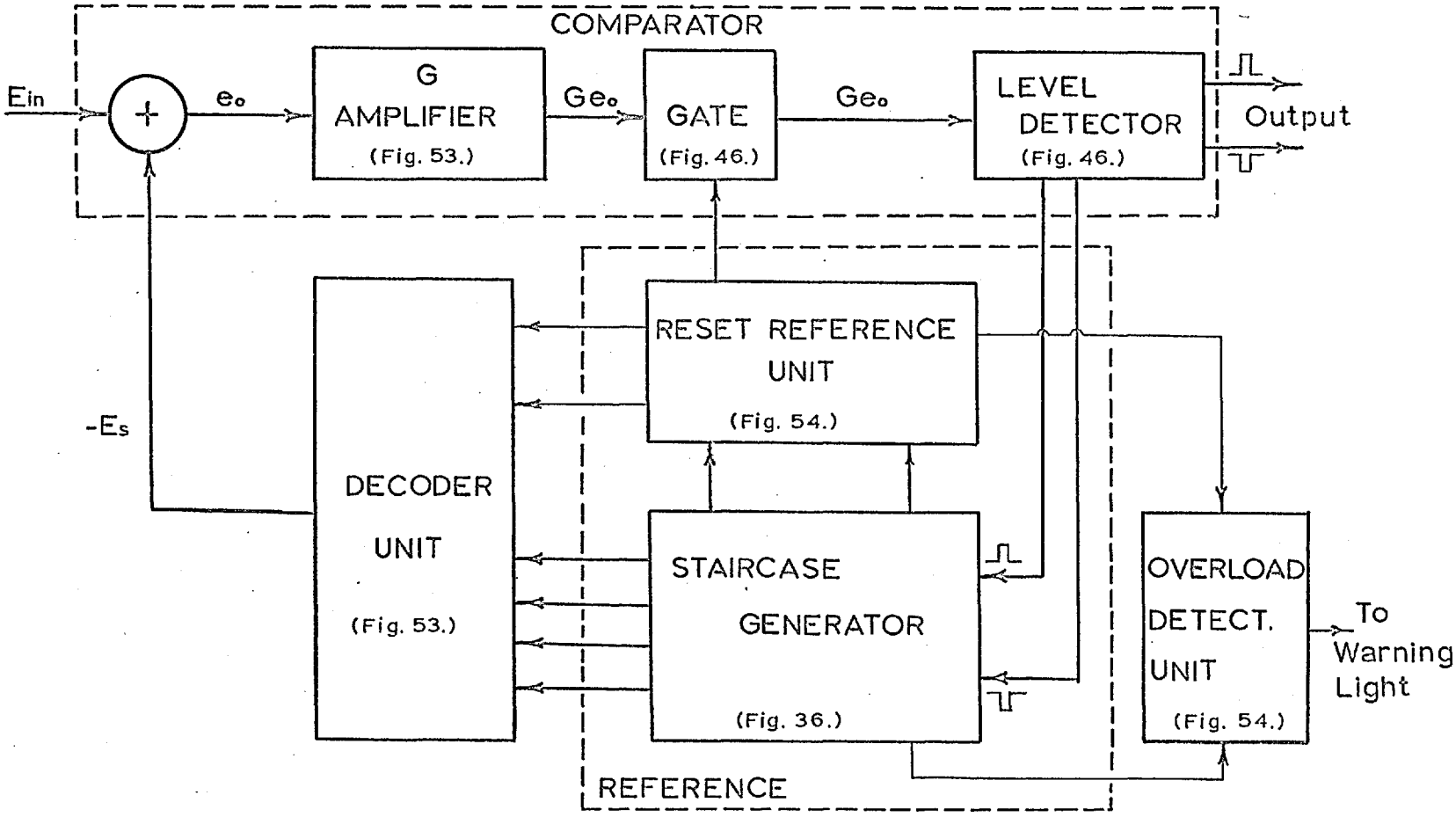
The Quantizer.

C H A P T E R 4

Design of Auxiliary Circuits.

Before the staircase generator of Part I could be used in a quantizer, the design of a number of auxiliary circuits was required. An A-D converter of the type described in Chapter 1 (Figure 2) was built as illustrated by the block diagram of Figure 45. The function of every unit can be deduced from the explanation given in Chapter 1 for the basic system.

The summation of the input variable, E_{in}, with the reference voltage, E_s, from the decoder, produces an error signal, e_o, which, after amplification, is fed via a gate to a level detector. This latter unit generates an output pulse of the same polarity as e_o every time its input becomes greater than a predetermined voltage level on either side of zero. Simultaneously, the level detector also feeds a pulse to the staircase generator, adjusting $-E_s$ by one quantization interval such that e_o is returned to zero. Under normal conditions, the



COMPLETE BLOCK DIAGRAM OF QUANTIZER

Fig. 45.

reference, $-E_s$, tracks the input variable in that way to less than plus or minus one quantization interval. An output pulse is therefore generated every time E_{in} has changed by one quantization interval, q, and the feedback action keeps the amplitude of the error signal, e_o, between fixed limits. The pulse repetition rate appearing at the output is proportional to the slope, $\Delta E_{in}/\Delta t$, of the input variable, and the polarity of these pulses is similar to that of the slope.

On the other hand, if the rate of change, $\Delta E_{in}/\Delta t$, at the input exceeds the maximum speed of the feedback action, the error signal does not return below the cross over point when one pulse is fed to the staircase generator. In this case, the level detector generates a continuous train of pulses at the maximum repetition rate accepted by the staircase generator until the error signal has fallen below the critical level. The quantizer can therefore recover rapidly after a variation of the input signal exceeding its speed limit. This useful property becomes indispensable if the converter is time shared, for instance, between a number of independent variables.

In the course of these operations, the cycling process described in Chapter 3 (section 3.4), may be initiated in the stepping reference unit. As soon as one

side of the staircase generator resets to zero, a voltage step equivalent to one hundred quantization intervals would appear at the input of the summing amplifier. This large discontinuity in E_s would be maintained until the end of the cycling process when the opposite side would reset to zero. It was shown in Chapter 3 that this action was controlled by a 10Mc/s pulse generator and can last for up to 1μsec in the worst case (subtraction of nine levels). If nothing were done about it, the amplifier would overload severely and a number of unwanted output pulses would be generated by the level detector. The Reset Reference Unit included in Figure 45 was introduced to cope with this situation. It consists of two accurately defined voltage references of opposite polarities equivalent to one hundred quantization intervals each. One or the other of these references is removed at the beginning of the cycling process by the operation of a corresponding flip flop circuit in order to compensate for the discontinuity in E_s; the flip flop is switched back at the end of the cycling and the Reset Reference Unit regains its original state. It will be seen later that it is advisable to inhibit the input to the level detector during the cycling process in order to avoid the generation of spurious output pulses caused by voltage spikes of a few nanoseconds duration appearing in E_s when the Reset Reference Unit is switched on or off. The gate shown in Figure 45 was introduced

for that purpose. This precaution also eased the precision requirements for the Reset Reference Unit.

It can therefore be said at this stage that the quantizer just described operates on the principle outlined in Chapter 1 and that it contains necessary refinements imposed by practical circuit considerations. The timing sequence in the different loops presented no special difficulties as the system is asynchronous, i.e. the ending of a particular event automatically starts the following one. The speed requirement was that no auxiliary unit should limit, if possible, the maximum pulse repetition rate of the staircase generator. The design specifications for the summing amplifier, the level detector and the Reset Reference Unit were also dictated to a large extent by the influence of these parts on the over-all accuracy of the converter. A detailed analysis of the quantizer in terms of precision requirements and tolerances has been summarized in Appendix A.11. Sufficient insight into the problem was gained from these derivations to complete the design of the quantizer. It is now intended to outline briefly the design procedures for these various circuits in so far as they differ from normal practice. Some of their most striking features will also be mentioned.

4.1. Level Detector.

A circuit diagram of the level detector is shown in Figure 46. The function of this unit in the quantizer was explained at the beginning of the present chapter with reference to Figure 45. Considerable simplification of the design resulted from the use of a single tunnel diode circuit to operate both as a voltage level detector and as a pulse generator.

4.1.1. Basic Circuit of Level Detector.

In order to illustrate more clearly the principle of operation of the level detector circuit, part of Figure 46 has been reproduced in Figure 47. This circuit uses the tunnel diode peak current value to define a detected level of input signal; a single pulse is required to mark the instant of detection. In the present scheme, an increase of applied signal level, V_{in}, from zero, causes a corresponding increase of the diode current (all input current being taken by the diode) until the peak current level is reached. The diode switches to the high voltage state and the resulting voltage change initiates the diversion of the input current from the diode causing it to return to the low voltage state. The system can be well described, in terms previously employed, by the characteristic of Figure 48, (compare to Figure 28.).

LEVEL DETECTOR UNIT

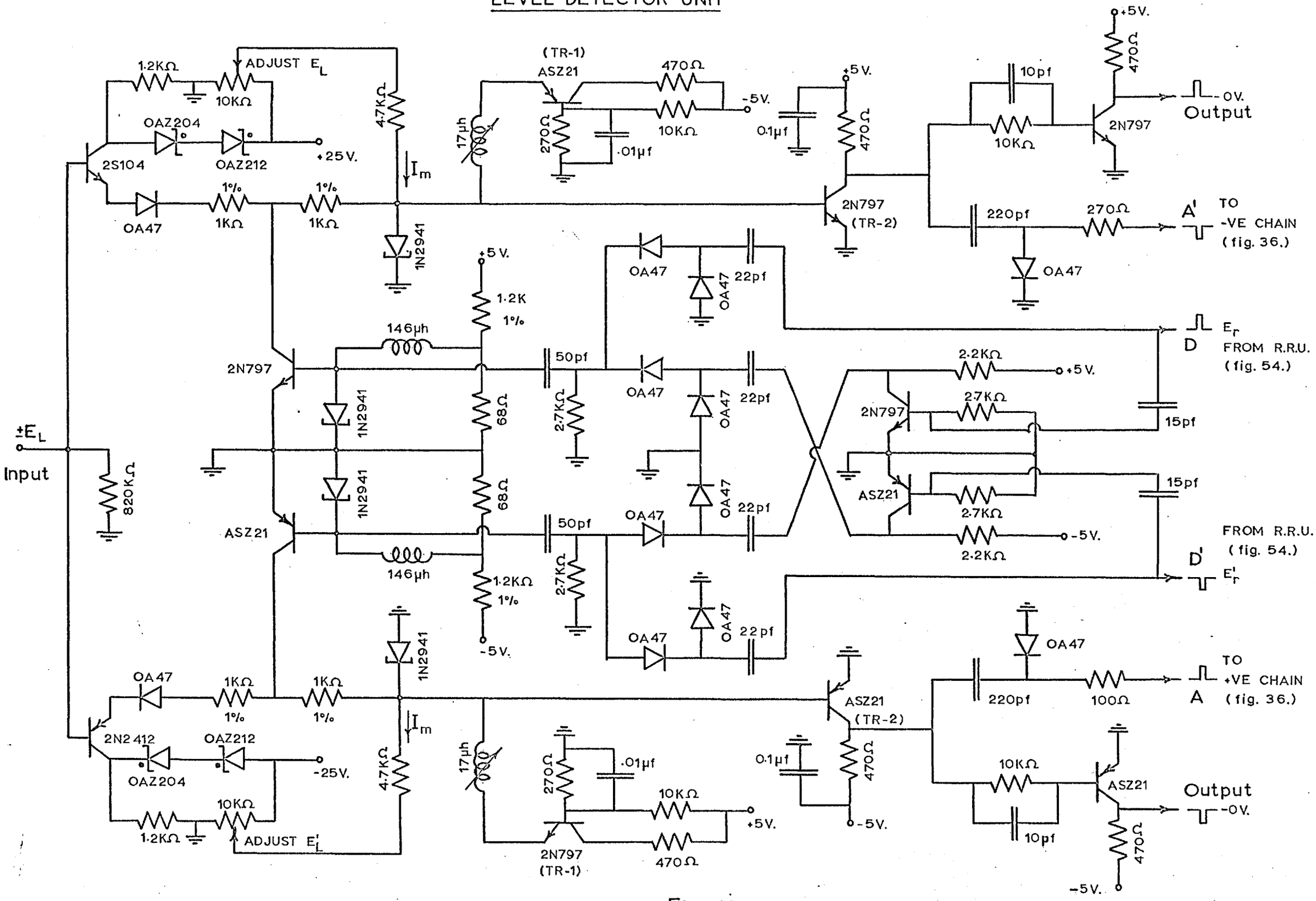
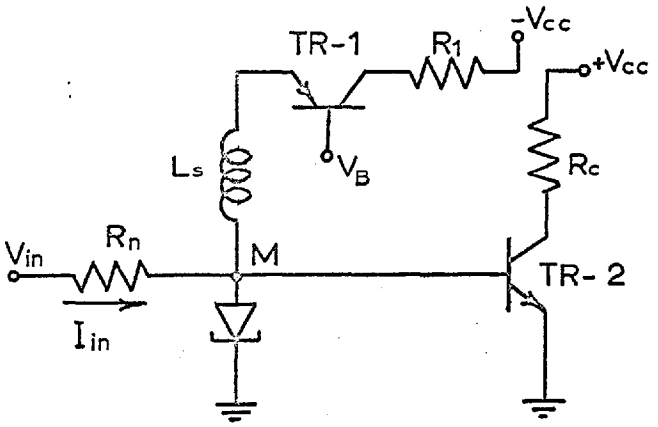


Fig. 46.

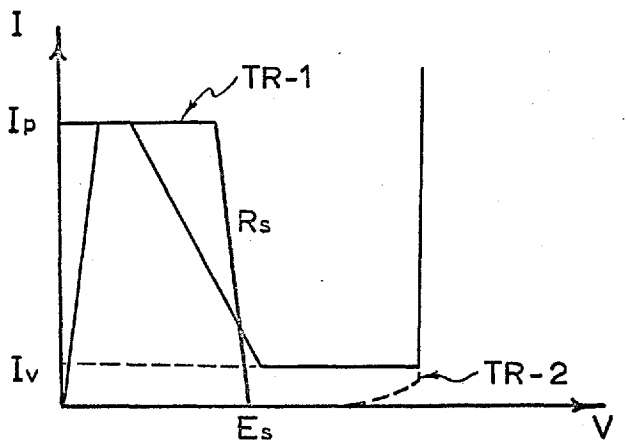


LEVEL DETECTOR

BASIC CIRCUIT.

(COMPARE TO Fig. 27.)

Fig. 47.



ELECTRICAL

CHARACTERISTIC

(COMPARE TO Fig. 28.)

Fig. 48.

This figure shows a linear approximation of the electrical static characteristic corresponding to the circuit of Figure 47; the transistor, TR1, (detecting the change to the high voltage state) is considered as a load on the tunnel diode and the presence of TR2 is taken into account as was done previously in Chapter 2. The base of TR1 is biased with a small negative voltage, V_B, such that the input characteristic of this transistor in a common base configuration, drawn as a load line (see Figure 48), does not intersect the tunnel diode curve above the valley voltage, V_v.

Suppose that the input voltage, V_{in}, is initially at zero and that both TR1 and TR2 are cut off. If V_{in} is then increased sufficiently to raise the input current (defined by V_{in} across a relatively large resistance, R_n) above I_p, the tunnel diode switches rapidly to the high voltage state and TR2 is turned on as explained in Chapter 2 (section 2.5.1.). At the same time, the current starts building up in the inductance, L_s, gradually turning on the transistor TR1. As soon as the current in the tunnel diode has fallen below the valley current, I_v, the diode switches back to the low voltage state. The cycle is then completed as the transistors cut off. This relaxation oscillation is sustained as long as the input current, due to V_{in}, is greater or equal to I_p. On the

other hand, if V_{in} is decreased such that the input current is smaller than I_p, the circuit becomes stable at a point below the peak of the tunnel diode.

It follows from the above description that the method of analysis developed in Chapter 2 for the tunnel diode relaxation oscillator (section 2.5.) can be applied to the present circuit without any modification. The nonlinearity introduced in R_s by the transistor TR1, has negligible effects on the accuracy of Equation (35) (see section 3.5.1.) in the calculation of the magnitude of L_s as a function of the period of oscillation. A series of tests carried out in the laboratory have shown that Equation (35) can predict the period of oscillation of the circuit under study with an accuracy better than 5% for $I_{in} = I_p$, E_s = 200 to 300mv and for pulse repetition rates up to 10Mc/s. The voltage, E_s, is measured at point M (Figure 47), when the tunnel diode and the transistor, TR2, are removed and $I_{in} = I_p$. This voltage, E_s, must be adjusted between 200 and 300mv such that no stable point is present when $I_{in} = I_p$. For a typical 1N2941 tunnel diode (Appendix A.9.), and for R_s = 26ohms, E_s = 250mv and for a period of oscillation T = 0.8μsec, a value of L_s equal to 17μh can be found from Equation (35). The choice of the pulse repetition rate of the level detector resulted from a compromise between the maximum speed of

the staircase generator and the overload recovery time of the summing amplifier after a fast input voltage step.

4.1.2. Related Problems.

The basic circuit just described was shown to possess the fundamental properties required for the level detector unit. In view of its functions in the quantizer, a few refinements were introduced as illustrated in Figure 46.

The pulse inverter and the differentiating network connected to the transistor, TR2, supply respectively the output pulses and an adequate drive for the staircase generator. The design and performance of such circuits have been discussed thoroughly in Chapter 2 and will not be repeated here.

The complete level detector unit is perfectly symmetrical. It employs two complementary versions of the basic circuit defining a negative as well as a positive voltage level. Provision is made for a single input with a voltage range extending to ± 9 volts. The emitter-base diodes of the silicon transistors used as input emitter followers, have a specified maximum reverse voltage of approximately 5 volts. These transistors can enter into the breakdown region without undergoing any noticeable damage provided that the power dissipated in the junction

is kept below a safe value[45]. An OA47 germanium switching diode was put in series with the emitter of each of these transistors to limit the reverse current to a few micro-amperes whenever the breakdown region is reached.

4.1.3. Temperature Coefficient.

A simple expression for the temperature coefficient of the level detector can be derived as follows. The magnitude of the input voltage necessary to trigger the tunnel diode can be written as in Equation (71).

$$E_L = V_{BE} + V_1 + R_n(I_p - I_m) + V_p \quad .. (71)$$

where E_L = input voltage necessary to bring the operation of the tunnel diode to its peak point.

V_{BE} = voltage appearing between the base and emitter of the input transistor when the emitter current is equal to $(I_p - I_m)$.

V_1 = voltage appearing across the OA47 diode when $I = I_p - I_m$.

I_m = current supplied to the tunnel diode by the level adjustment network (Figure 46).

The differentiation of Equation (71) with respect to temperature yields Equation (72) for the temperature

coefficient of the level detector. It is assumed that the current, I_m, and the resistor, R_n, have a negligible temperature sensitivity.

$$\frac{dE_L}{dT} = \frac{dV_{BE}}{dT} + \frac{dV_1}{dT} + \frac{R_n dI_p}{dT} + \frac{dV_p}{dT} \qquad .. (72)$$

The first two terms of Equation (72) represent the temperature coefficient of the voltage drop across semiconductor diodes and are approximately equal to $-2.5mv/^oC$ for both germanium and silicon[44,page 130]. The last term of Equation (72) is of the order of $-60\mu V/^oC$ (see section 3.3.). If $R_n.dI_p/dT$ is adjusted to a value of about $+5mv/^oC$, a very small temperature coefficient is obtained for the level detector. With R_n equal to 2Kohms, a temperature coefficient $dI_p/dT = (+5mv/^oC)/(2000ohms) = +2.5\mu A/^oC$ is needed. It was shown in section 3.3. that a 1N2941 tunnel diode manufactured by General Electric, with a selected peak voltage of the order of 60mv would approach this requirement. A net temperature coefficient of less than $1mv/^oC$ was measured for the level detector using that technique, for a total variation of twenty degrees Centigrade about room temperature.

It may be noted, in passing, that this circuit combines many interesting features which well illustrate the advantages of hybrid tunnel diode-transistor circuits.

In view of the complexity of the operation achieved by the level detector, the number of components is unusually small. The temperature coefficient, described by Equation (72), can be easily controlled to become positive, negative or zero, by adjusting the resistor, R_n, or by selecting a tunnel diode with a different peak voltage. A simple means of adjusting accurately the threshold over a large voltage range is provided. The amount of backlash between switch on and off can be reduced or increased with the base voltage, V_B. If V_B is made sufficiently small, the circuit no longer generates pulses when the threshold is exceeded and becomes a direct-coupled bistable with a change-over time of a few nanoseconds. Finally, it is worth noting that the frequency response is adequate for many applications as the level detector was operated in the laboratory, without any special care, at a pulse repetition rate as high as 10Mc/s.

The performance of the unit shown in Figure 46 will now be outlined.

4.1.4. Performance.

A photograph of an oscilloscope display is shown in Figure 49, illustrating the response of the level detector to a voltage pulse fed from the summing amplifier. Details concerning that photograph are included in

PULSE RESPONSE OF LEVEL DETECTOR

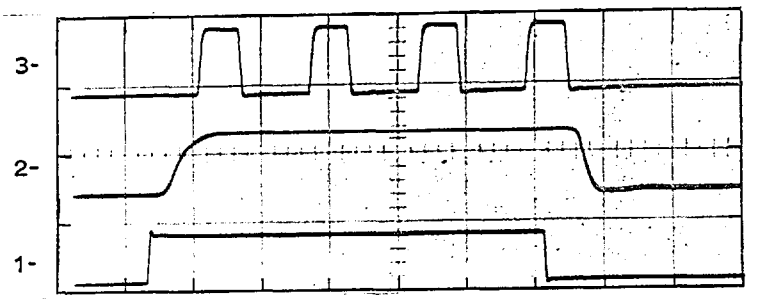


Fig. 49.

Traces. 1- Input pulse to the summing amplifier. Amplitude slightly greater than one quantization interval.

2- Output voltage pulse from summing amplifier unit.

3- Output pulses from the level detector unit. (Corresponding to output of quantizer)

Scales. Horizontal: 0.5 μsec/cm

Vertical : Trace 1 = about 6mv/cm (uncalibrated)

Trace 2 = 10 volts/cm

Trace 3 = 5 volts/cm

Notes. 1- Trace 1 was read on a 2 volts/cm scale but the effective input was reduced to about 4.5mv by a resistance divider.

2- Similar results can be obtained with a negative input signal giving negative output pulses.

Figure 49. The performance of the complete level detector circuit is summarized below.

Input Impedance: greater than 100Kohms in parallel with 10pf when mounted on a Vero board.

Adjustment of voltage threshold: continuous from 0.4 to 9.5 volts.

Polarities: positive and negative.

Backlash as referred to input: 30mv.

Temperature coefficient as referred to input: less than -1mv/°C.

Sensitivity to supply fluctuations: smaller than -0.2volt/volt for all supplies.

Output: 5 volt pulses of both polarities with a 470 ohms output impedance.

Pulse Repetition Rate in Astable Condition: adjusted to 1.25Mc/s.

4.1.5. The Level Detector Gate.

The gate shown in Figure 46, is used to short circuit to ground both sides of the level detector input every time the cycling operation is being performed in the staircase generator. In this way, any undesirable

voltage transient appearing at the output of the summing amplifier while that process is going on, is prevented from interfering with the normal operation of the quantizer. The function of the level detector is not otherwise affected.

The gating circuit, like most of the units in the quantizer, is perfectly symmetrical. Its main element is a tunnel diode monopulser of the type described in section 2.6. As soon as the positive or the negative half of the Reset Reference Unit is switched on, at the beginning of the cycling process, both sides of the level detector gate are triggered via corresponding diode OR gates. The operating times on both sides of the gate are controlled by adjusting the inductances in the two monopulsers and are made slightly longer than the maximum duration of the cycling process. The design procedures for all of these circuits have been well established in Chapter 2.

In order to illustrate the operation of the gate in the quantizer, a constant negative voltage greater than the critical level was applied to the detector, transforming it into a pulse generator. Figure 50 shows a photograph of the resulting waveform generated at the output of the second positive decade of the staircase generator together with the gating pulse produced during the cycling process as the input signal is being short circuited to ground.

OPERATION OF LEVEL DETECTOR GATE

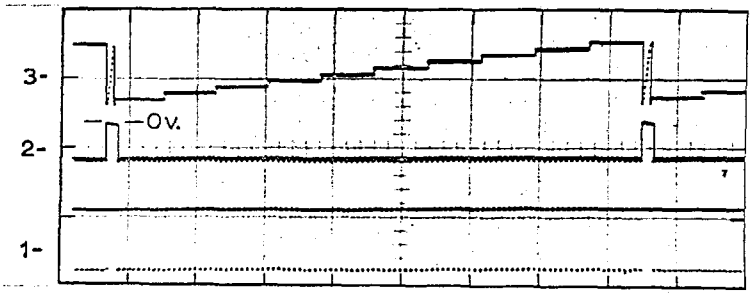


Fig. 50.

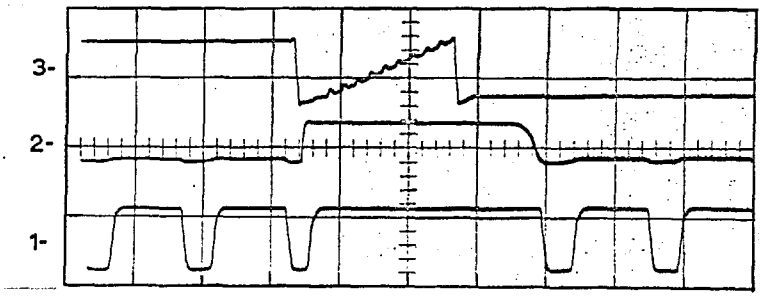


Fig. 51.

Traces. 1- Output pulses from the level detector when a fixed negative voltage, exceeding the detected level, is applied to its input.

2- Driving voltage as seen at the collector of the transistor in the level detector gate (see fig. 46.)

3- Voltage across second positive chain driven from the level detector (including cycling operation).

Scales. Horizontal: 10 μsec/cm (fig. 50.)

0.5 μsec/cm (fig. 51.)

Vertical : 5 volts/cm (all traces in both figures)

Note. 1- Figure 51. shows details of level detector gate operation during cycling process included in figure 50. (See description in section 4.1.5.)

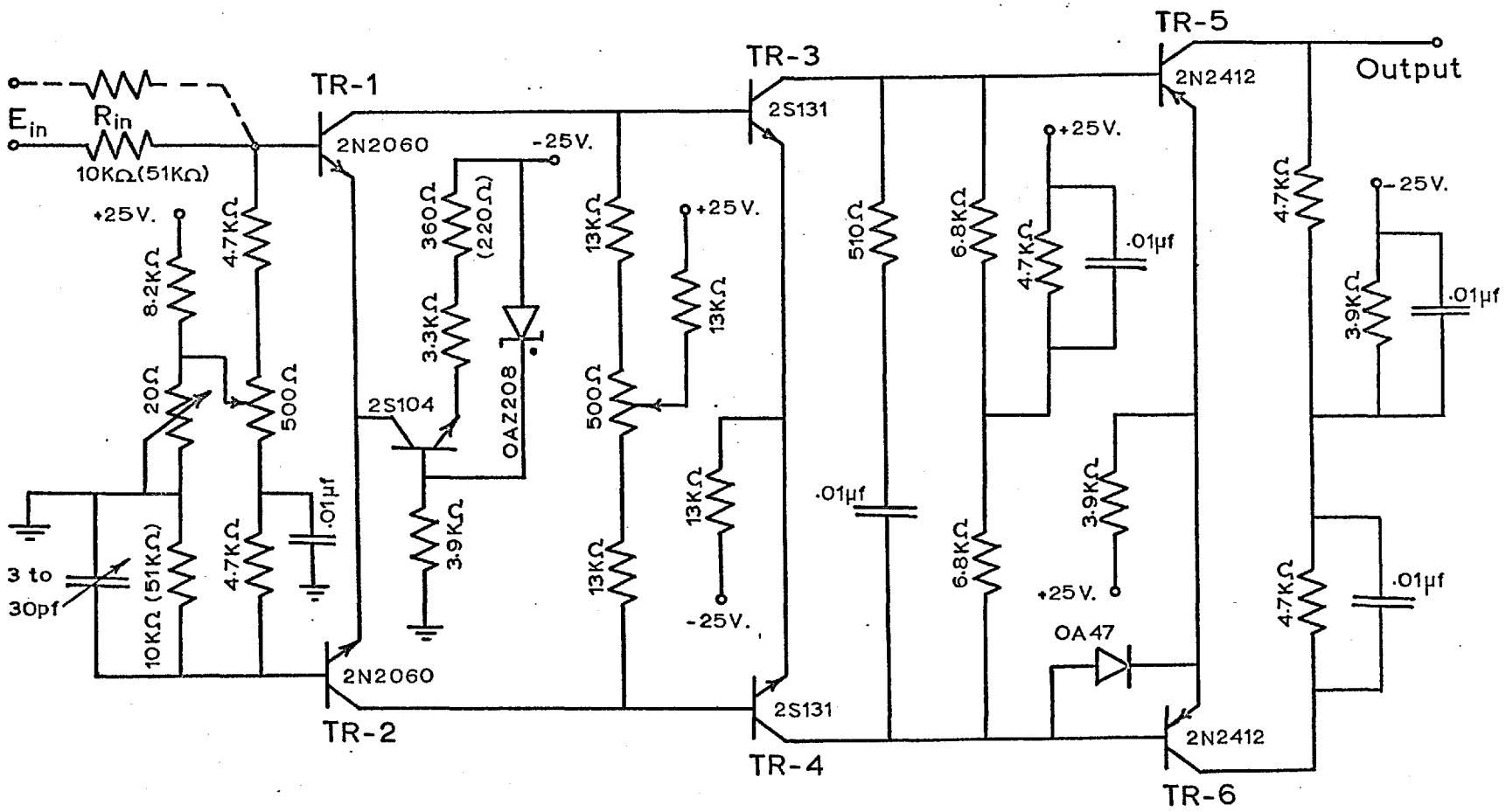
Details of that operation can be seen in Figure 51 on an expanded time scale.

The level detector unit was shown thus far to satisfy all of the conditions for its application in the quantizer. The design of a summing amplifier to supply an adequate driving voltage will now be outlined briefly.

4.2. Summing Amplifier.

The operational amplifier shown in Figure 52 was designed to perform the summation of e_{in} with the various reference signals and to provide for a large voltage gain.

To minimize the influence of the drift of the level detector on the accuracy of the quantizer, it was decided to fix the cross-over points above plus and minus eight volts respectively. Consequently, a rather large amplification of the error signal was needed in order to preserve the sensitivity of the converter. A minimum quantization interval of 5mv was estimated as satisfactory and a voltage gain of approximately two thousand times was therefore aimed at. A direct-coupled amplifier was required with a low input impedance, negligible zero drift and a highly stable gain in the regions corresponding to outputs of plus and minus eight volts. The use of cascaded virtual earth feedback amplifiers suggested



NOTES: 1- Values in brackets are for the second amplifier (see fig. 53.).

2-Feedback resistor not shown.

3- All fixed resistors are metal oxide (1% Tol.).

HIGH GAIN WIDE BAND D.C. AMPLIFIER

Fig. 52.

itself as a possible solution.

In principle, the circuit illustrated in Figure 52 is a straightforward application of well established design techniques. The use of balanced transistor pairs in low drift direct-coupled operational amplifiers has been analysed thoroughly in the literature[46,47,48]. A useful survey of the problems related to the design of such amplifiers has also been published recently[49]. A few comments will therefore be sufficient to clarify certain points in the present design.

A special biasing arrangement was utilized for the base of the transistors in the input stage in order to operate the long tailed pair with equal base-to-emitter voltages. A potentiometer was also included for the adjustment of the base voltage to zero. Considerable reduction of the thermal drift can be achieved using that technique, as compared to the results possible with more conventional methods, and temperature coefficients as low as 0.05μV/°C have been reported[50]. An additional resistance equal to R_{in} was connected between the unused base of the first stage and ground to restore the circuit balance thus avoiding deterioration of the common mode rejection ratio.

The design of the temperature compensated constant current source biasing the emitters of the input

pair is a repetition of the example already given in Appendix A.5. Emitter currents of 500μA were selected for the first stage as a compromise between noise and bandwidth considerations.

The matched pair (2N2060) employed in the first stage has a much lower cut off frequency than the other transistors in the amplifier. A larger bandwidth could certainly be achieved if an amplifier were designed with the faster matched pairs now available from Fairchild Semiconductor. In order to preserve as much as possible of the frequency response, the amplifier has been stabilized only for large values of the feedback resistance; it would break into oscillation if much smaller values were introduced. The feedback resistance was made rather large in view of the high voltage gain required and of its relation to the magnitude of the input resistance ($G = R_F/R_{in}$) of the quantizer. A capacitance-resistance network connected across the output of the second stage reduces the loop gain at high frequencies before the 2N2060 has started to cause a significant phase shift. The open-loop current gain at low frequency is approximately two hundred thousand times.

The diode shown across the base and emitter of the transistor TR6, protects TR6 and TR4 from entering into breakdown if TR5 is pushed into saturation, removing

momentarily the feedback action.

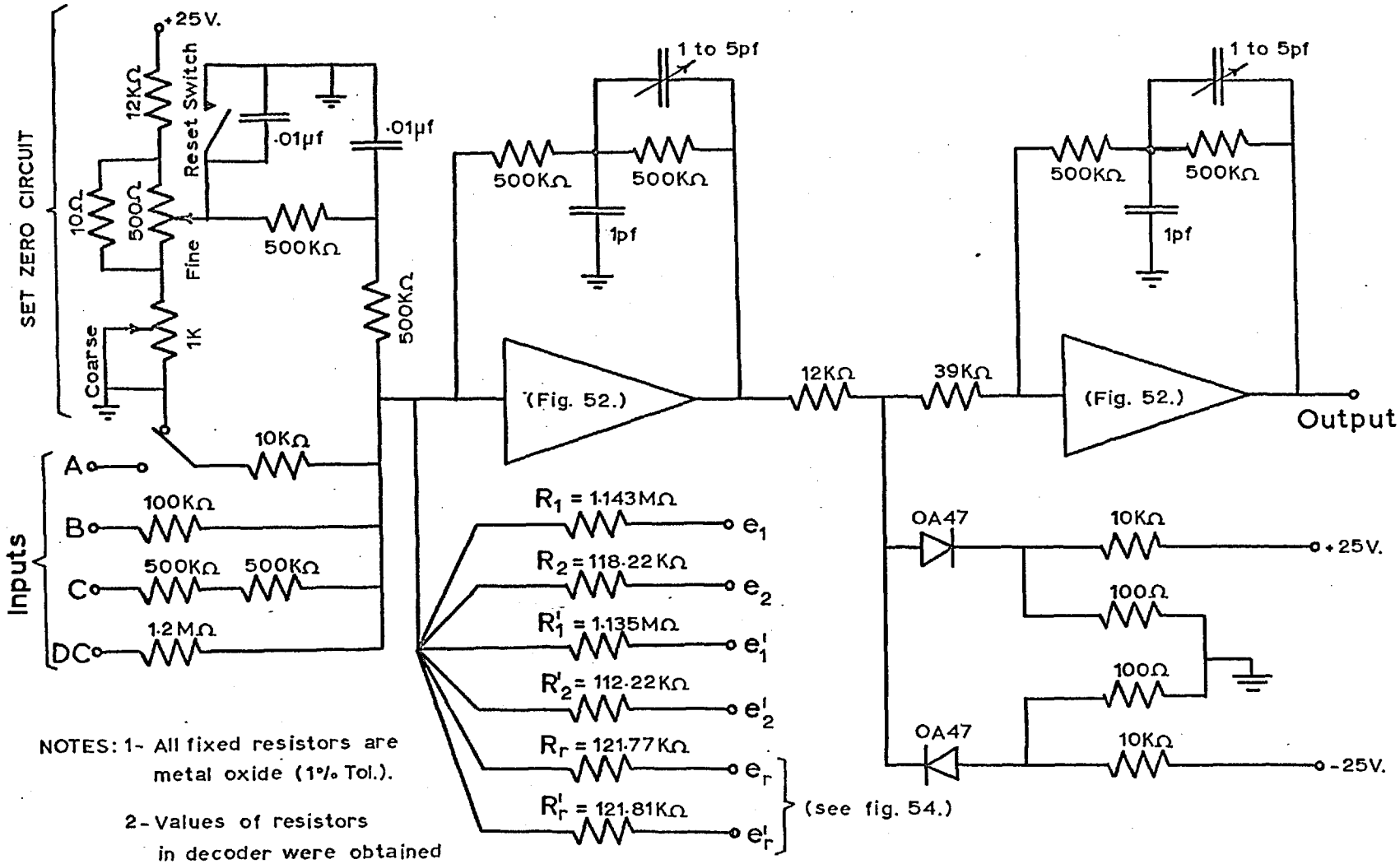
Two operational amplifiers of the type just described were cascaded, as illustrated in Figure 53, to obtain the desirable voltage gain. The limiter circuit shown in the coupling network between the two amplifiers helps reducing the overload recovery time of the system.

4.2.1. Performance.

The characteristics for the summing amplifier unit have been summarized below.

D.C. Voltage gain = 1600.
Input impedance = 10Kohms.
Output impedance = 4.7Kohms (approx.).
Output voltage range = ±9 volts.
Risetime, t_r = 0.28μsec (see Figure 49).
Bandwidth = 1.25Mc/s (computed from t_r).
Time delay = 0.15μsec.
Output noise = 0.44 volt peak-to-peak.
Output thermal coefficient = -13mv/°C
Output sensitivity to supplies fluctuations
= -0.3 volt/volt.

The performance of the amplifier unit will be illustrated in a more realistic fashion (Chapter 5) in a later study of the quantizer.



NOTES: 1- All fixed resistors are metal oxide (1% Tol.).

2- Values of resistors in decoder were obtained from resistance networks.

SUMMING AMPLIFIER UNIT

Fig. 53.

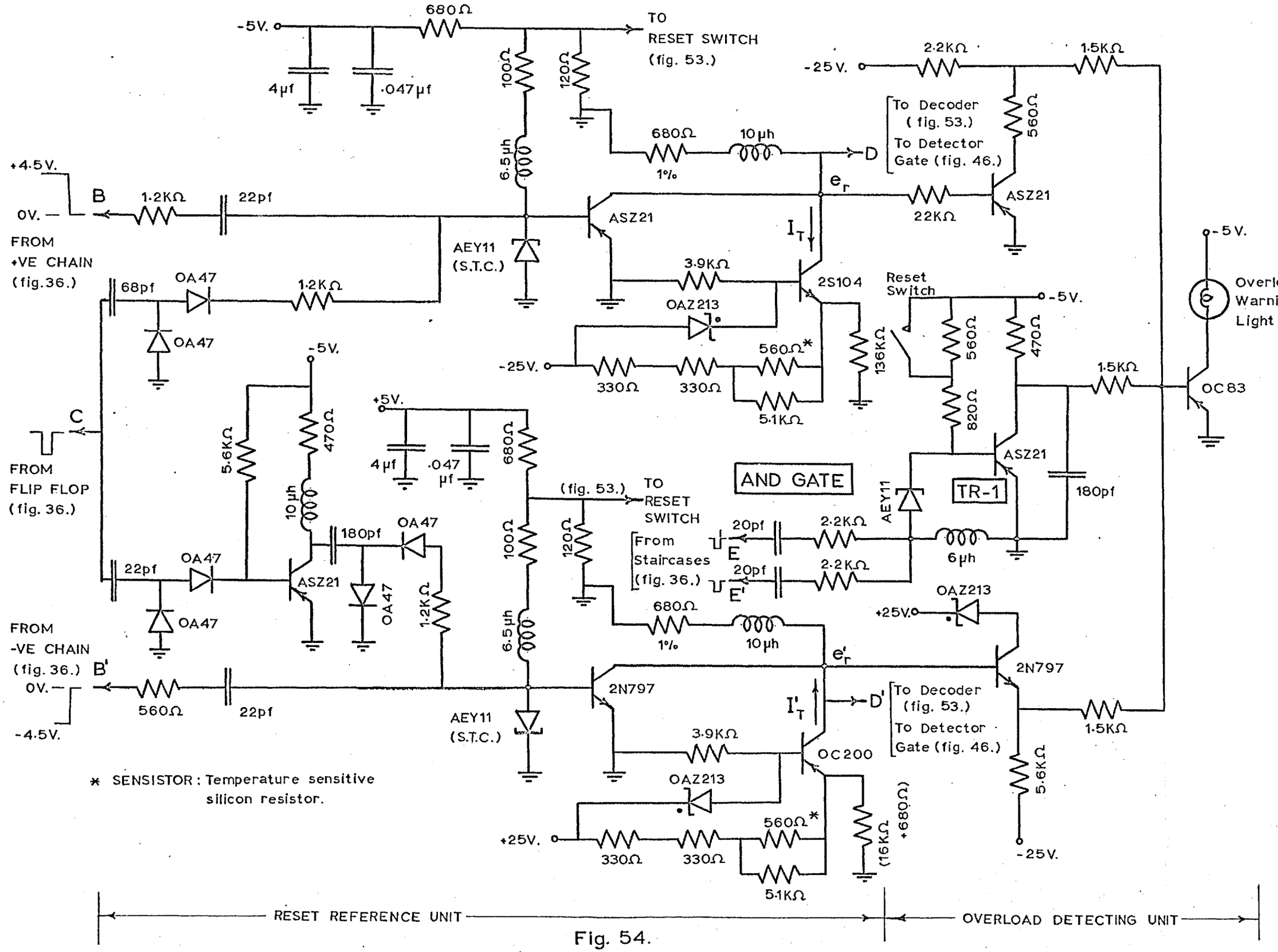
4.3. Reset Reference Unit.

The reset reference unit serves the purpose of keeping the signal from the decoder constant during the cycling of the staircase generator. A circuit diagram for that unit is shown in Figure 54. Owing to its perfect symmetry, only one side will be considered in the following discussion. The function of the unit in the quantizer was explained at the beginning of the present chapter and only a few remarks on the circuits will be added here.

A stand-by voltage, e_r, (see Appendix A.11) is defined across a 680ohms metal oxide resistor connected to the output of a constant current source. A common-emitter transistor, controlled by a one-tunnel diode flip flop, is used to short circuit that current to ground during the cycling process. The resulting voltage step, E_r, is equal to the saturation voltage, V_{ce} (sat), of the transistor minus e_r. It can be seen from Figure 54, that the flip flop is switched on as soon as the corresponding decade starts resetting in the staircase generator. It is triggered back to its original state at the end of the cycling process by the trailing edge of a negative pulse produced in the other bistable (see Figure 36), which controls the 10Mc/s pulse generator.

The design procedure, developed in Chapter 3 for the one-tunnel diode flip flop, was followed to

RESET REFERENCE UNIT AND OVERLOAD DETECTING UNIT



* SENSISTOR : Temperature sensitive silicon resistor.

Fig. 54.

calculate the component values indicated in Figure 54. The magnitude of the inductance, L = 6.5μh, was computed from Equation (64) together with Equations (68), (69) and (70), for T = 0.1μsec. The tunnel diode rests normally in the low voltage state and the worst situation arises when a single pulse is generated in the cycling process. In this case, the tunnel diode is triggered back approximately 0.13μsec after it has been switched on.

The pulse inverter driving one of the flip flops was designed earlier in section 2.7. Peaking inductances were inserted at the collector and in series with the resistors defining e_r in order to speed up the response of the Reset Reference Unit. Any significant delay in the switching times of this unit may cause serious overshoots at the output of the summing amplifier.

The constant current sources are similar to the circuit described in Appendix A.5. A temperature sensitive silicon resistor (sensistor) was included in the emitter resistance, R_e, in order to raise the temperature coefficient of the Reset Reference Unit to a value approximately equal to that of the corresponding chain in the staircase generator. It was shown in Appendix A.11 (section A.11.7.1.), that this technique is useful in reducing the precision required from the Reset Reference

Unit for a given temperature range. Problems related to the computation of this temperature coefficient are discussed in Appendix A.12, where it is shown that a figure of -11mv/°C is acceptable for both e_r and e'_r. The temperature coefficient of R_e, necessary to achieve this performance, was extracted from Equation (A.14) in Appendix A.5. It was obtained in the circuit from a series combination of a 560ohms sensistor (+0.7% temperature coefficient) with a metal oxide resistor of about 660ohms. Both I_T and I'_T and their temperature coefficients were finally adjusted in place with parallel resistors as indicated in Figure 54.

These comments on the design of the Reset Reference Unit completed the description of all circuits in the major feedback loop of the quantizer. However, an overload detection unit (shown in Figure 45), was also included in the converter and its design will now be discussed briefly.

4.4. Overload Detection Unit.

The overload detection unit does not take part in the normal operation of the quantizer. Its circuit diagram was drawn in Figure 54, together with the Reset Reference Unit.

The OC83 transistor, (Figure 54), is used to drive a warning light and it can be turned on by any one

of the three transistors connected to its base or by any number of them operating simultaneously. The transistor, TR1, is normally kept into saturation by the tunnel diode which is biased in the high voltage state. The tunnel diode itself operates as an AND gate and it can be switched to the low voltage state only when two simultaneous pulses are fed to its inputs. The design of such a gate is readily deduced from the procedure outlined in Chapter 2 for the monopulser. If an input signal, e_{in}, greater than one hundred quantization intervals, is applied to the converter, the full capacity of the staircase generator is exceeded and the system overloads. One event peculiar to this situation can be detected at the end of the cycling process when both sides reset simultaneously after the subtraction has been performed between an empty chain and a full one. Resulting coincident pulses are used to trigger the AND gate described above, ultimately switching on the warning light. After the overload is removed, the AND gate must be reset manually to its original state in order to turn off the light in the overload indicator.

The other two transistors connected respectively to each side of the Reset Reference Unit (Figure 54), would turn on the warning light if any of the flip flopsfailed to operate at the end of the cycling process. This arrangement was utilized at an early stage in the design to

indicate possible faults in the Reset Reference Unit or in the staircase generator during the cycling operation. This part of the circuit has not been removed as it can still prove useful when testing the various units separately.

4.5. Linearity of Staircase Generator.

To conclude this chapter, reference will be made to the results of Appendix A.12. in which the linearity requirements for the chains in the staircase generator have been derived. The various factors comprised in Equation (A.51) of Appendix A.11, were computed in Appendix A.12. from a knowledge of the circuits described in the present chapter.

Table IX, (Appendix A.12), illustrates the inter-dependence between the minimum precision requirements for the steps in the chains and the maximum deviation of the staircase waveforms for a given temperature range. It can be seen that for a precision of 1% on the steps in any decade, a deviation three times larger than this can be tolerated for a temperature range of $\pm 5^{o}C$. The data contained in Appendix A.7, show that the tunnel diode chains used for the second decades meet these requirements by a safe margin. It is interesting to note, from Table IX, that the influence of increasing the operating

temperature range on the minimum precision requirements for the steps is almost negligible as compared to the drastic effect of a change in the maximum deviation. Both the positive and the negative staircase waveforms containing one hundred steps each are illustrated in Figure 55. These photographs of oscilloscope displays show the voltage waveforms appearing at the summing junction when the amplifier has been removed and when the stepping reference is being driven continuously. The large impedance seen at that point under such circumstances is responsible for the long resetting time.

Thus far, solutions have been found to the problems concerning the design of all units shown in Figure 45. The performance of the quantizer which was built with these various parts will be outlined in the next chapter. A general discussion of the results will finally assess the merits of the technique illustrated by the prototype, in view of the aims defined in the introduction and in Chapter 1.

COMPLETE REFERENCE STAIRCASE WAVEFORMS

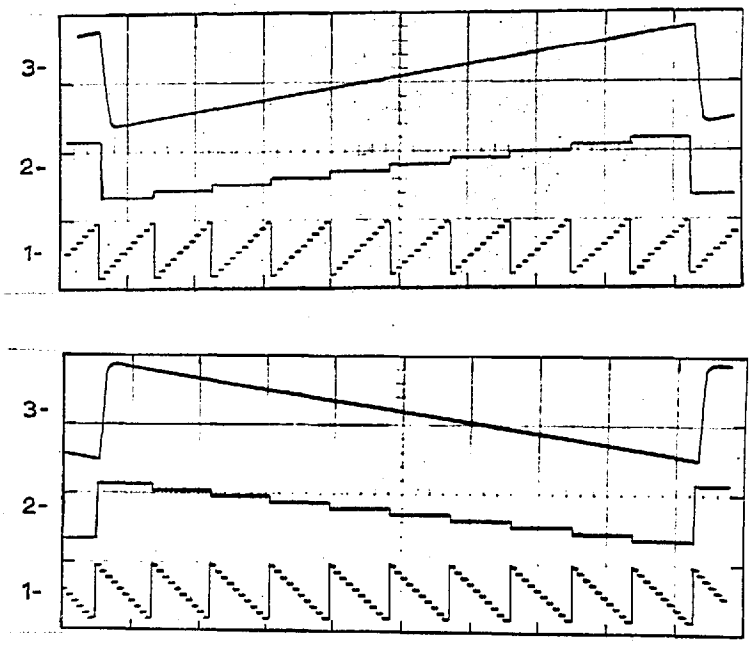


Fig. 55.

Traces. 1- Voltage waveforms (positive and negative) appearing across the first decades driven from continuous pulse trains.

2- Similar to trace 1 but for the second decades driven from the first ones.

3- Voltage waveform seen at the opened summing junction point from the decoder unit when one side of the stepping reference is operated at a time. (See section 4.5.)

Scales. Horizontal: 20μsec/cm

Vertical : Traces 1 and 2 = 5 volts/cm

Trace 3 = 0.5 volt/cm

Note. Both photographs were taken under similar conditions. (The combined waveform is made up of 99 steps in each case).

C H A P T E R 5

Performance of the Prototype and Discussion of the Results.

The equipment built in the laboratory to illustrate the principle of operation of the quantizer described in the thesis, is shown in Figures 56 and 57.

To provide maximum flexibility, the circuits were mounted on plug-in type Vero boards, as can be seen in Figures 58 and 59; sockets were used for transistors and tunnel diodes. The power supplies were carefully decoupled, (filters in Figure 57), and electric shields were introduced in critical positions, (see Figure 57 and 2nd decades circuit board), in order to avoid undesirable interaction between various circuits and between components on the same board. As a further precaution, all connections between boards were made with shielded cables. Whenever possible, the positioning of the boards and the lay-out of each circuit was arranged to necessitate connecting cables of short lengths only, so as to minimize capacitive loading on the circuits. These measures were taken in view of the high frequency response of most circuits in the quantizer and of the low voltage levels at which tunnel diodes operate.

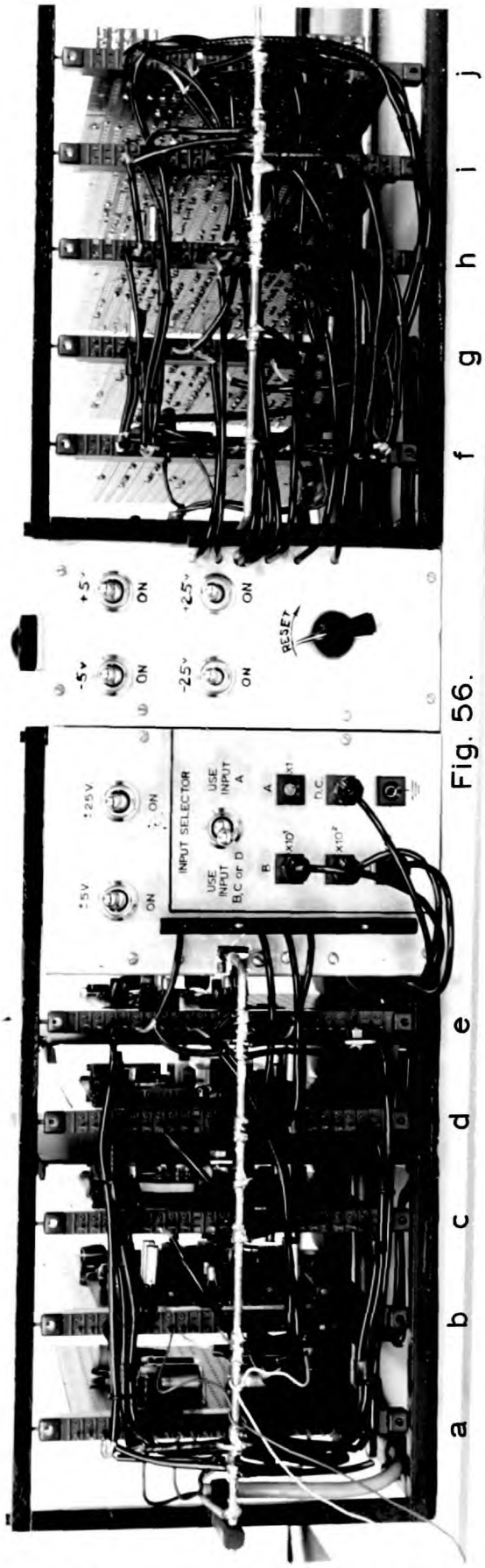


Fig. 56.

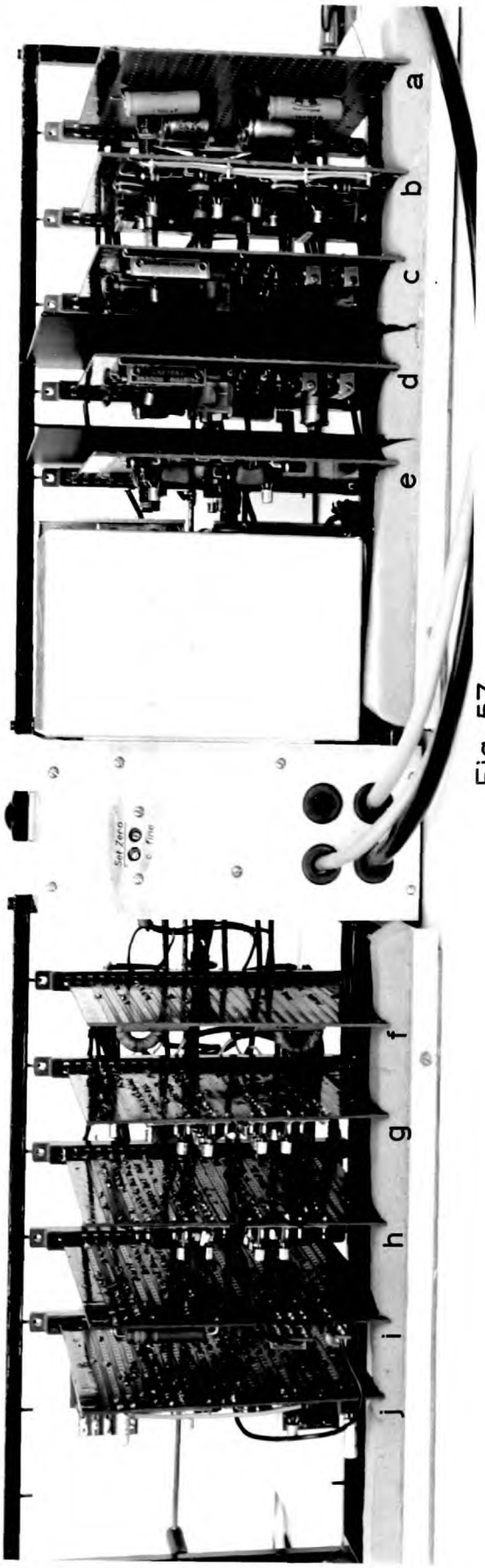


Fig. 57.

Figure 56. FRONT VIEW OF QUANTIZER.

Figure 57. REAR VIEW OF QUANTIZER.

Position of Boards.

a- Filters; b- Level Detector; c- 1st Amplifier; d- 2nd Amplifier; e- Level Detector Gate; f- Filters; g- 1st Decades; h- 2nd Decades; i- 10Mc/s Cycling Unit, Flip Flop, Overload Indicator; j- Reset Reference Unit, Overload Detector.

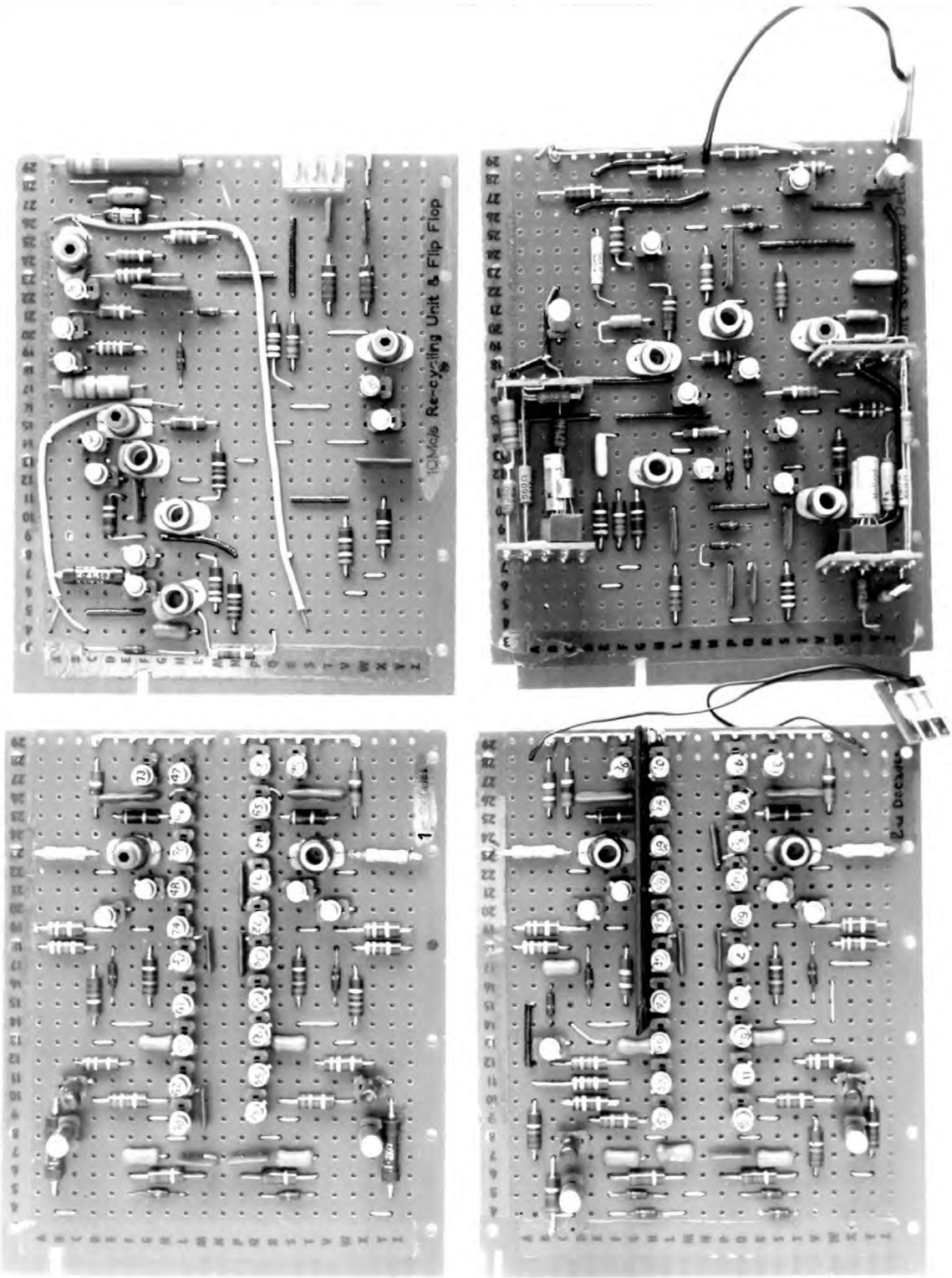


Fig. 58.

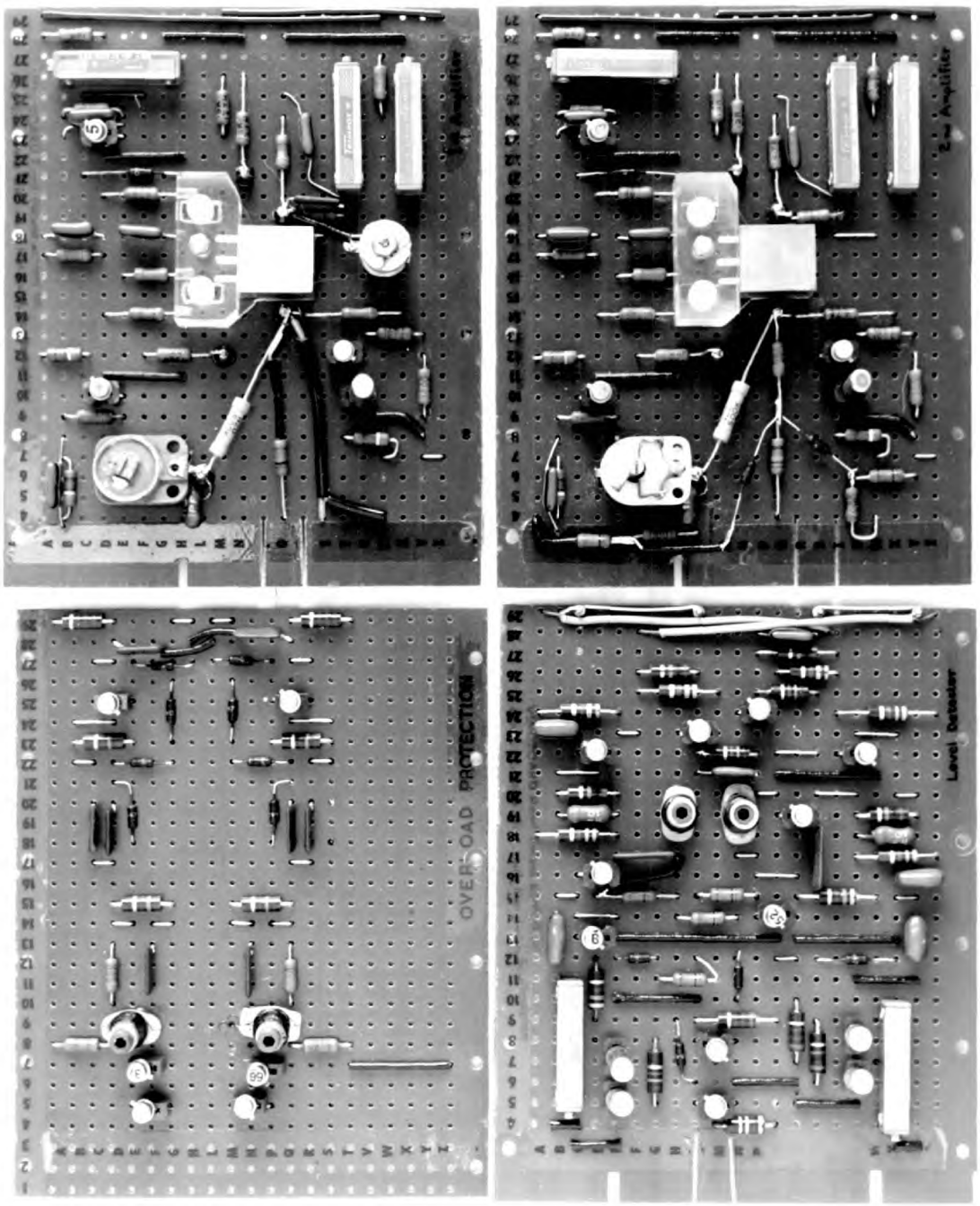

2-W Amplifier
2-W Amplifier
OVERLOAD PROTECTION
Level Detector
1 inch

Fig. 59.

Experience has shown that the system was not affected by electric or magnetic pick-up under normal conditions prevailing in the laboratory. However, it would be advisable to shield the summing amplifiers if relays or switches were operated closer than a few feet from the quantizer. The sensitivity of the tunnel diode circuits to electro-magnetic pick-up was reduced (as a consequence of the worst-case design approach) to a level acceptable for the present application. A more oomplete investigation of this matter would be required before an adequate enclosure could be designed for the apparatus.

Some of the characteristic features of the quantizer will now be illustrated by the results of certain tests performed in the laboratory.

5.1. Very Low Frequency Test.

The following scheme was used to measure the over-all performance of the quantizer at very low frequencies.

A positive voltage ramp increasing from zero at a rate of less than 10mv/sec. was generated by integration and applied to the 10x input of the converter such that a quantization level was passed every 4 seconds or so. Every pulse generated at the output of the quantizer caused

a Solartron 1010 digital voltmeter to sample the input signal at that instant. The coded result was automatically punched on a paper tape, to be finally printed out. The same process was repeated with a negative voltage ramp. In this way, two hundred readings were recorded, corresponding to the voltage levels defined by the quantizer on both sides of zero. The accuracy of the measurements was limited to about ± 5% of one quantization interval by the presence of a small 50c.p.s. component superimposed on the voltage ramp used as the input signal. Nevertheless, useful information about the characteristics of the converter was deduced from these results. The various definitions which will now be used to describe the performance of the converter, follow the general recommendation published three years ago in the AIEE Transactions[51].

(a) Total Count.

The full scale reading of the converter is divided into 200 intervals by the staircase generator. This number of divisions could be extended to 2000 if one more chain were added to each side of the stepping reference unit. In such a case, however, trimming of the tunnel diodes in these chains and adequate temperature control would be required. The decoder resistances would also have to be adjusted more accurately.

(b) Resolution.

The resolution is a measure of the smallest change in the input signal which can be detected by the converter; it is very nearly equal to one quantization interval. The quantization intervals were obtained from the above test by the subtraction of successive readings and their computed averages for the positive and the negative sides were 40.69mv and 40.68mv respectively. Adjustment of the average quantization interval can be made at the level detector, E_L and E_L', or by changing the input resistance, R_{in}. For the test described above, the second input resistance, R_{in} = 100Kohms, was used instead of the ten times more sensitive input in order to reduce the relative importance of the hum present in the ramp signal. On the most sensitive range, the input resistance of the converter is 10Kohms and the quantization interval is equal to 4mv. The maximum resolution in a system of this type would be limited ultimately by the noise in the summing amplifier.

(c) Zero Offset.

The zero offset is defined as the magnitude of the output reading provided by the system, as referred to the input, for zero input signal. In the present case, no pulse appears at the output of the quantizer for zero input and the zero offset is nil.

(d) Deviation.

The deviation is the amount, relative to the correct magnitude of the signal at the point of measurement, by which the measured value varies from the true value after correction of the zero drift. From the results mentioned earlier, the maximum deviation was computed for each polarity and was -0.43% for a positive input and +0.43% for a negative input. As expected, the deviations were directly related to those measured in the tunnel diode chains (Appendix A.7) and therefore reached a maximum at mid-scale. This situation could be improved if desired by choosing values of E_2 and E'_2 (see Appendix A.11) slightly different from the measured averages for the corresponding chains. In this case, the resulting deviations at full scale would have to be taken into account during the adjustment of the reset reference steps, E_r and E'_r.

(e) Linearity.

The linearity is a measure of the constancy of the ratio between the output and the input values. Using the average quantization interval given above, it was found that the linearity of the results was +0.3% of one half full scale for the positive side and +0.2% for the negative side.

(f) Repeatability.

The reproducibility of several independent quantizations of a fixed input signal can be estimated from the maximum total deviation which results from any combination of levels between the positive and the negative staircases. The worst condition is met when the chains are at -46 and +36 levels respectively where the resulting deviation is equal to -3.5% of the input signal or -0.18% of full scale.

(g) Repeatability of the Zero.

The error as referred to the input, when the quantizer is returned to zero in the course of operation, reaches a maximum of -27% of one quantization interval when both staircases are at the 46th level. This result is obtained under condition that the thermal drift for zero input was initially balanced out with the "set zero" circuit, after resetting all chains manually.

(h) Quantization Uncertainty.

The only significant source of uncertainty in the definition of the two hundred voltage thresholds is the noise appearing at the output of the summing amplifier. From the data given in Chapter 4, it can be seen that this uncertainty amounts to less than ± 3% of one quantization interval.

The quantization error in the system is basically equal to ± 1 part in 200 or ± 0.5%. The absolute accuracy of the prototype, taking into account the sources of error already listed, is therefore reduced by the chains nonlinearities to ± 0.8% of full scale.

A few more tests will now be described to illustrate the dynamic response of the quantizer.

5.2. Dynamic Tests.

The internal operation of the main feedback loop in the quantizer is illustrated in Figure 60. To take the photograph shown in this figure, a sinewave of sufficiently high frequency was applied to the input of the converter with a small enough amplitude to cover only a few quantization intervals. The input sinewave is represented, superimposed on the voltage waveform appearing at the output of the summing amplifier. Quick feedback action from the stepping reference is indicated by a large discontinuity of the amplifier output every time the level detector is triggered.

A clear demonstration of the analogue-to-digital conversion performed by the system can be seen in Figure 61. This photograph shows part of an input sinewave together with the corresponding pulse train representation; it illustrates well the dependence of the output pulse

OPERATION OF THE MAIN FEEDBACK LOOP IN THE QUANTIZER

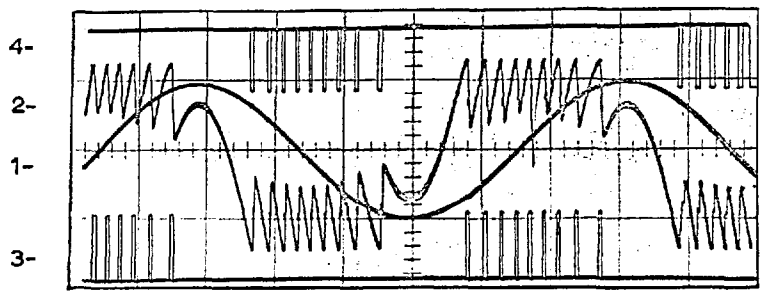


Fig. 60.

Traces. 1- Sinusoidal input to the quantizer. Frequency was about 16Kc/sec.

2- Voltage waveform appearing at the output of the summing amplifier (input of level detector) showing feedback action from stepping reference.

3- Positive output pulses from quantizer produced by positive slopes of the input signal.

4- Negative equivalent of trace 3 for negative input slopes.

Scales. Horizontal: 10 μsec/cm

Vertical : Trace 1 = 0.2 volt/cm

Traces 2,3,4 = 5 volts/cm

Notes. 1- Quantization interval = about 40mv as referred to input of quantizer.

2- See section 5.2. for description.

ANALOGUE-TO-DIGITAL CONVERSION OF

PART OF A SINE WAVE

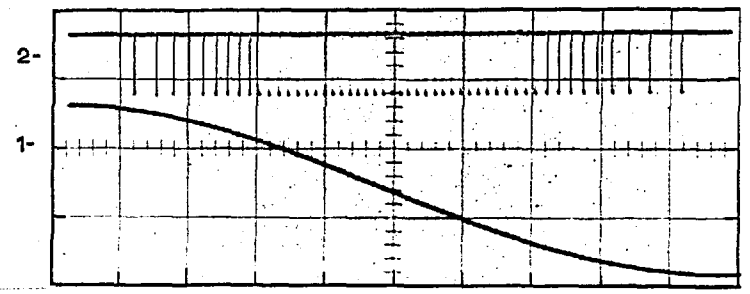


Fig. 61.

Traces. 1- Part of an input sine wave.

2- Output pulses from quantizer corresponding to trace 1.

Scales. Horizontal: about 8μsec/cm (uncalibrated)

Vertical : Trace 1 = uncalibrated

Trace 2 = 5 volts/cm

Notes. 1- Input frequency was between 6 to 7Kc/s.

2- Input quantization interval = about 40mv.

3- Note dependence of output p.r.r. on input signal rate of change.

4- See section 5.2. for description.

repetition rate on the slope of the input signal.

5.2.1. Step Response.

In order to investigate the dynamic response of the converter, a continuous train of relatively long pulses was fed to the system and the output pulses generated by the converter were integrated to reconstitute the original input signal. Figure 62 shows a photograph of two oscilloscope traces corresponding respectively to the input signal and the reconstructed waveform.

The overshoot in the step response of the converter is due to the overload recovery time of the summing amplifier unit. Control of that overshoot is possible by adjusting the pulse repetition rate in the level detector when the summing amplifier overloads. Ideally, the amplifier unit should recover from a nearly full scale overload as soon as the action of the level detector has raised the stepping reference to the required level. Complete recovery should be achieved before an extra pulse is generated by the level detector. To do so, some means of protecting the amplifiers from excessive overload would have to be provided. A limiter circuit, introduced between the two amplifiers (Figure 53), improved the situation only partially. Considerable difficulty arises because of the very low current levels which must not be

STEP RESPONSE OF CONVERTER

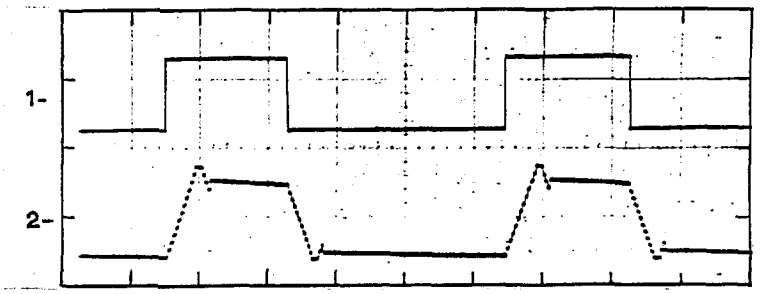


Fig. 62.

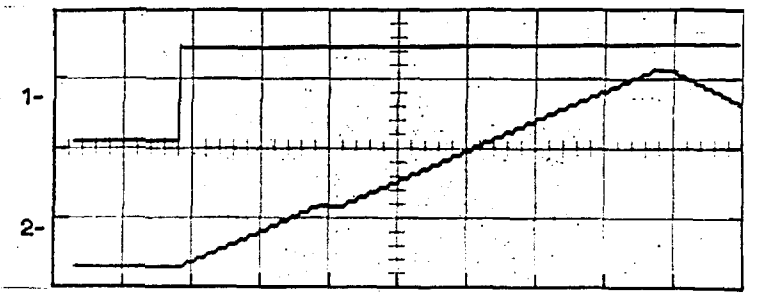


Fig. 63.

Traces. 1- Pulses fed to the input of the converter.

2- Waveform resulting from integration of the output pulses generated by the converter when operated by the input signal shown in trace 1.

Scales. Horizontal: 20μsec/cm (fig. 62.)

5μsec/cm (fig. 63.)

Vertical : Uncalibrated.

Notes. 1- Quantization interval = about 4mv.

2- Note pause in figure 63. due to level detector gate operation during cycling process.

3- See section 5.2.1. for description.

exceeded at the summing junction (i.e. 0.4 μA for a full scale reading of the amplifier unit). It may be advisable to design a new amplifier unit if it is hoped to take full advantage of the high frequency response of all other parts of the quantizer. Very large open loop gain and utilization of over-all feedback in the present amplifiers make it difficult to exert any control on the overload recovery time of the unit. A brief investigation carried out in the laboratory has shown that a circuit using a temperature compensated common-base input stage followed by adequate amplification could replace the two feedback amplifiers employed in the present system. With this new approach to the design, a few stages would be sufficient to produce directly the amount of gain required; problems of overload protection would be simplified and improved frequency response of the amplifier unit could also be expected.

In the prototype, however, the pulse repetition rate of the level detector was simply decreased to 1.25Mc/s (see Figure 49), to allow for a certain overload of the summing amplifier while still preserving a reasonable speed. This adjustment does not permit the use of large input steps which would produce an off-scale overshoot in the converter. It is interesting to note, however, that such a system continues tracking the input signal after a

temporary overload of the amplifier unit; only a transient output error is produced in such cases.

Maximum allowable rate of change of the input signal, to avoid overloading the summing amplifier, can be computed from the level detector pulse repetition rate multiplied by the magnitude of a quantization interval; this maximum input slope can be expressed as $\Delta E_{in}/\Delta t = 1.25 \times 10^6(q)$ volts/sec. On the most sensitive range, for instance, q = 4mv and $\Delta E_{in}/\Delta t$ must be smaller than 5.0×10^3 volts/sec.

Another useful specification for a quantizer is the maximum conversion time. In the present system, it is equal to the time required to sweep the staircase generator over its full range at the maximum pulse repetition rate of the level detector. With a 0.8 μsec period (Figure 49), it takes 160 μsec to generate the full 200 steps. If another 2 μsec is added to allow for the pause created by gating action during the cycling process, a maximum conversion time of 162 μsec is found under most adverse conditions. This result means that over 6000 conversions per second could be effected by the present system, assuming that the sampling time of any input gate could be neglected. For an input signal covering only part of the full scale amplitude, the maximum number of

conversions per second, as computed above, would be increased proportionally. The operation of the level detector gate is illustrated in Figure 63, which represents an expanded view of the step response given in Figure 62. It should be noted that the maximum conversion time could be reduced by a factor of almost ten if a faster amplifier were available, such that the staircase generator could be driven at 10Mc/s by the level detector (with a 1 μsec stop for cycling). It is to be noted however, that such a sampling system is by no means an optimum way of utilizing a quantizer of this type even though its performance in such service is highly satisfactory.

5.2.2. Frequency Response.

As explained in the example of Chapter 1 (section 1.4.4.), a relationship exists between the maximum frequency, f, of a sinusoidal input signal acceptable to the converter and its peak-to-peak amplitude, A; this dependence is given by $f = 1.25 \times 10^6 (q)/\pi A$. From this formula, it can be seen that the maximum frequency of an input sinewave utilizing the full range of the converter (i.e. 200 quantization intervals) must not exceed 2Kc/s. This result is slightly optimistic as it neglects a short time taken by the cycling process twice per cycle. The possibility of trading precision for speed in such a

FREQUENCY RESPONSE OF CONVERTER

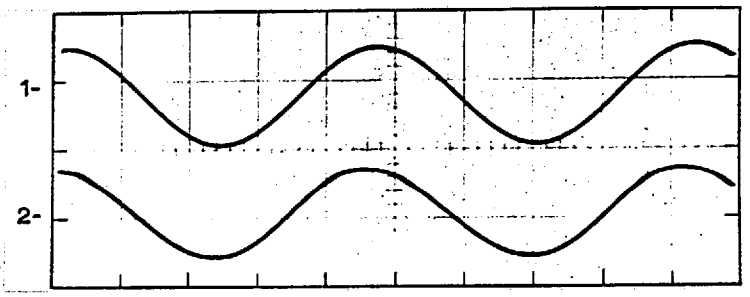


Fig. 64.

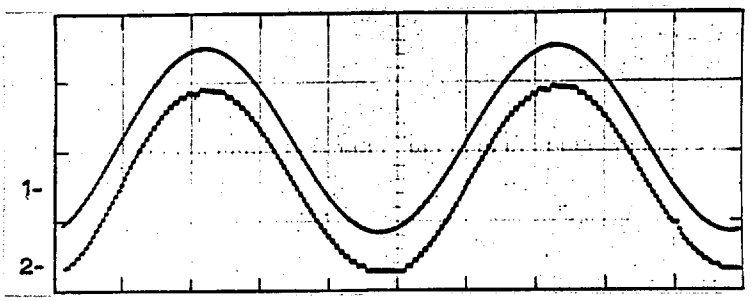


Fig. 65.

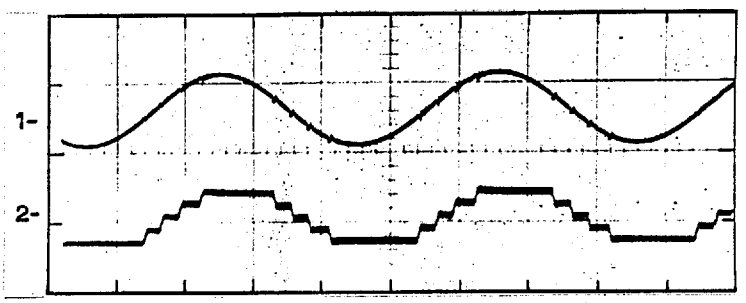


Fig. 66.

Note. See next page for description.

FREQUENCY RESPONSE OF CONVERTER

(See Figures 64, 65 and 66.)

Traces. 1 - Input sinusoidal waveform to the quantizer.

2 - Waveform resulting from integration of the output pulses generated by the converter when operated by the input signal shown in the corresponding trace 1.

Scales. Horizontal: Uncalibrated (Figure 64, 1Kc/s)

20 μ sec/cm (Figure 65, 10Kc/s)

5 μ sec/cm (Figure 66, 50Kc/s)

Vertical: Uncalibrated (all traces and all figures)

Notes concerning Figures 64, 65 and 66.

1. In Figure 64, approximately 100 quantization intervals were used by the input signal.
2. A Tektronix Type O plug-in Unit was used as the integrator. The noticeable slopes on the flat portions of the reconstituted waveforms are due to leakage in the integrator itself.
3. Quantization interval = about 40mv.
4. In Figure 65, the maximum number of quantization intervals in which the converter can divide a 10Kc/s sinusoidal input signal were used. The effect of the cycling operation can be seen to the right of this figure on the reconstituted waveform.
5. In Figure 66, the 50 c.p.s. hum present in the integrator is noticeable on trace 2 because of the higher sensitivity of the vertical scale.
6. See section 5.2.2.

converter is illustrated by Figures 64, 65, and 66, which show the quantizer response to a sinewave of 1Kc/s, 10Kc/s and 50Kc/s respectively. Integration of output pulses was used as a means of comparing the reconstituted waveform to the input signal.

Thus far, the ability of the converter to perform high speed accurate quantizations of voltage signals was illustrated by the performance of a prototype built in the laboratory. In order to demonstrate the remarkable flexibility inherent in the new technique employed, a few interesting applications will now be considered briefly.

5.3. Applications.

Apart from the most obvious application as an analogue-to-digital converter, the apparatus can find a variety of uses for rather more general laboratory purposes. A selection of examples, covering various fields of application for which the converter is well suited, will now be outlined.

It is evident from the specifications already listed that mere addition of a forward backward counter and of adequate display circuits, would transform the system into a fast digital voltmeter. Such an instrument would preserve the interesting features of the quantizer,

including among others, circuit simplicity and notable flexibility.

Another scheme would utilize the equipment as part of an analogue multiplier. In this case, one of the signals to be multiplied is fed to the quantizer while the other is applied, through a number of parallel coded resistive networks, to the input of a summing amplifier. A simple gating circuit, controlled by the converter output pulses, would then suffice to complete the multiplier, for example, as follows. A short circuit could be removed from one coded resistor in the gating network for each positive pulse, thus increasing the analogue output product. Occurrence of a negative pulse would disconnect a corresponding input resistor causing the product to decrease proportionally. This scheme requires the addition to the quantizer of a relatively simple gating network; it takes advantage of digital techniques to produce a stable, accurate and reasonably fast analogue multiplier.

A further application would allow use of the converter as a digital integrator in the following way. The signal to be integrated is fed directly to the quantizer. A pulse generator is connected to drive a counter at a repetition rate proportional to the net number of pulses (positive minus negative) that have appeared at the converter output since zero time. (An easy way of

controlling the effective repetition rate is to direct the driving pulses, via a gating matrix, to stages of different significance in the counter, according to past sequences of pulses from the converter.) Assume that the repetition rate can effectively become negative by using a reversible counter and, for example, inverting the driving pulses according to the input signal polarity. It is clear that the counter would then provide at every instant a digital representation of the integrated input signal starting from any desired initial conditions. This application could certainly be effected by the digital voltmeter mentioned previously, employing the same counter and display, but with the introduction of an additional control network and a pulse generator.

Numerous applications of a slightly different type suggest themselves if it is noted that a peak of input signal is indicated in the quantizer by a reversal of output pulse polarity. To turn the instrument into a direct-coupled kicksorter, for instance, a gating matrix similar to that used in the integrator already described, could be employed to feed a pulse to a corresponding channel on occurrence of this sign inversion. Following the same argument, a quantizer of this type can operate as an holding sampler or a level-preserving pulse stretcher. In these cases, the level detector gate (section 4.1.5.) is

switched on with an auxiliary bistable circuit, whenever a peak is reached, (or at any other desirable instant); consequently, no more output pulses can be generated and a digital sample of the input signal, taken effectively at an instant immediately preceding the pause, can be stored in a counter until action is taken to reopen the gate. This facility is inherent in the quantizer and could be utilized in all applications already considered.

One fascinating prospect for a device of this type is in the broad field of signal analysis. A large number of statistical measurements on signals could be readily performed with the quantizer utilizing techniques illustrated in the previous examples. Simple or joint amplitude distributions of signals, for instance, could be investigated using the system to control a pulse generator (for time measurements) and a counter. In these applications, the new converter not only performs the analogue-to-digital transformation, most useful for data handling, but it can facilitate the analysis considerably by adjusting its performance according to some characteristics of the input signal itself. It follows, for example, that more efficient use of equipment and of storage facilities can result from employing this type of quantizer (as compared to ordinary sampling systems) on voltage waveforms having a wide spectral range. This last usage could be extended

to include accurate quantization of rapid voltage transients exceeding the speed limit of the apparatus, provided that the input signal is fed initially through an adequate smearing filter. Smearing techniques consist basically in the utilization of filters capable of distributing the energy of sharp signals over longer times, generally resulting in waveforms of much lower amplitudes. The original signal can be recovered using inverted filters. In this way, it may be possible for the maximum input rate of change for a given transient to be reduced sufficiently to fall within a range acceptable to the quantizer.

This list of general applications for a quantizer of this type could certainly be extended. However, it is clear from these few examples that a system, automatically adjusting its pace to suit the input signal being transformed, is inherently versatile. As pointed out in Chapter 1, the additional flexibility gained in choosing a completely asynchronous approach has undoubtedly outweighed the small loss which may arise in certain cases due to the absence of a fixed clock pulse frequency. It is realized that most applications mentioned earlier could be fulfilled separately by a number of existing instruments. However, combining all of these properties into a single potentially-inexpensive apparatus constitutes a very attractive proposition. It is fair to say that as a

portable general laboratory instrument, the quantizer described in this thesis possesses undeniable merits. An apparatus could be built employing the basic quantizer and a pulse counter as its main elements and a number of plug-in units would make it suitable for an ever widening range of uses.

In view of the preceding considerations and results, it is believed that the aims defined in the introduction and in Chapter 1, have been met satisfactorily. To sum up this work, two general comments will now be made with regard to the potential adaptability of the quantizer and on the significance of the design method, developed in the course of this research for tunnel diode-transistor hybrid circuits.

5.4. Conclusion.

Little more need be added to the matters discussed already in this chapter and to the concluding comments of section 5.3. However, two significant results of this project demand special consideration.

In the introduction, an ultimate aim was defined of producing a potentially adaptive circuit in view of its possible application in the design of highly flexible laboratory equipment. This general orientation has

significantly influenced the over-all design of the quantizer. The prototype described in this thesis has demonstrated a high degree of flexibility inherent in the technique employed. Furthermore, it may be noted that various means are potentially available within the present system to permit a closer control of its transfer characteristic. For instance, additional feedback loops or external connections to the decoder unit, could be used to alter the quantization interval according to any desired function of input signal or of outside parameters. Special inputs to the summing junction, controlled by the digital read-out through extra decoding networks, could also vary the effective transformation, depending on the past history of the input signal. The first method may suffer certain limitations as nonlinearities introduced in the decoder could interfere with the normal cycling operation of the staircase generator. With the latter approach, however, the present stepping reference and decoder are left unchanged such that the arrangement may be readily applicable to the prototype itself.

Therefore, the quantizer has shown sufficient flexibility to justify the hopes expressed in the introduction. It is believed that further investigations in the line just mentioned could very well lead to a type of circuit possessing a high degree of adaptability.

Another interesting aspect of the present research was the comprehensive study of tunnel diode-transistor hybrid switching circuits. Apart from a detailed investigation on the use of tunnel diodes as accurate voltage stepping references, a general design method was developed to cover a wide variety of these hybrid switching circuits. The technique is simple as it results from an analysis based on a piecewise-linear approximation of the tunnel diode characteristic. Numerous examples described in the thesis have shown that a precision better than $\pm$ 5% can be achieved in most designs for operating frequencies up to about 20Mc/s. Circuits like monostables, bistables, multivibrators, and many others, employing transistors as sole active elements, could be replaced advantageously in certain applications by hybrid equivalents designed with this simple method. It is to be noted, for instance, that extensive use of the tunnel diode-transistor combination has permitted a considerable reduction of circuit complexity in the quantizer.

It is believed that far too little attention has been paid by circuit designers to the advantages of using such hybrid tunnel diode-transistor combinations in medium speed circuits. Indeed, the circuits developed here to this end, show clearly certain of these advantages.

It is further believed that the method described in Chapter 2, offers interesting possibilities as a new and powerful tool in circuit design, particularly in view of its simplicity and of the remarkable circuit features which result. These aspects represent what is considered to be a significant contribution arising out of this research; the primary result of which has been the practical realization and assessment of the flexible quantization scheme discussed here.

APPENDIX A.1.

THE TUNNEL DIODE CHARACTERISTIC.

A.1.1. Linear Approximation of the Tunnel Diode Characteristic.

In order to avoid the solution of nonlinear differential equations, in the analysis of the tunnel diode switching process, a linearized characteristic can be used in place of the exact curve reproduced here from Figure 3. The approximation shown in Figure 67, has been suggested in the Tunnel Diode Manual[32], page 51. The slopes can be determined from a few simple empirical equations.

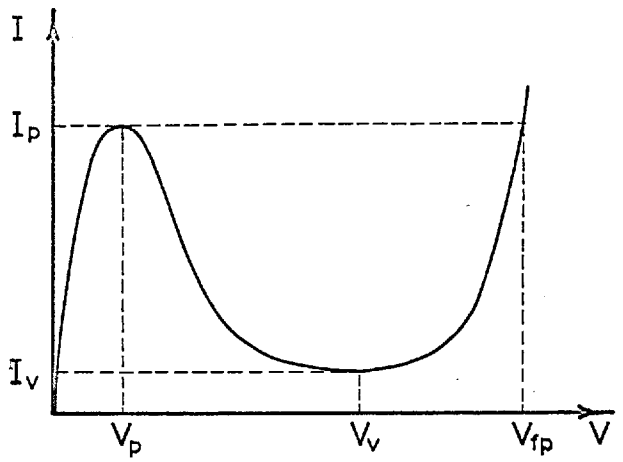
$$R_{d1} = \frac{0.75V_p}{I_p} \qquad .. (A.1)$$

$$V'_v = \frac{V_{fp} + V_v}{2} \qquad .. (A.2)$$

$$R_{d2} = \frac{V_{fp} - V'_v}{I_p - I_v} \qquad .. (A.3)$$

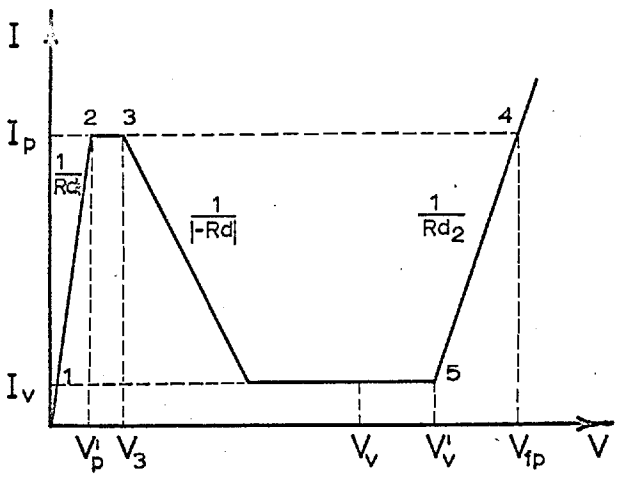
$$V_3 = 1.25V_p \qquad .. (A.4)$$

The design of a tunnel diode relaxation oscillator using the above equations is described in section 2.5. An improved version of this equivalent characteristic is given in Appendix A.2. and a comparison of the accuracies of the two methods can be found in Appendix A.3.



TUNNEL DIODE CHARACTERISTIC

Fig. 3.



LINEARIZED CHARACTERISTIC

Fig. 67.

APPENDIX A.2.

THE TUNNEL DIODE RELAXATION OSCILLATOR.

A.2.1. Linear Approximation of the Tunnel Diode Characteristic: (Improved Accuracy).

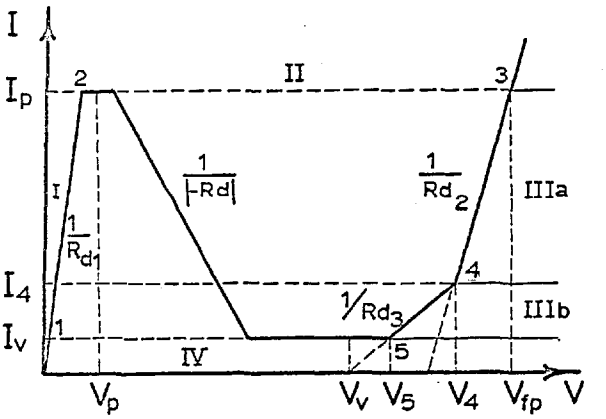
The expressions derived in section 2.5. for the switching times of the tunnel diode relaxation oscillator were relying on the validity of the approximations defined by Equations (A.1) to (A.4). The following empirical equations (see Figure 68), lead to a much more accuracte linear model for the tunnel diode. The linearization of the characteristic below the valley voltage point, V_v, remains unchanged. Point 4 was chosen such that V_4 and I_4 would be easy to calculate (see Equations (A.5) and (A.6)) while providing the desired accuracy.

Summary of the procedure: (see Figure 68).

1. Equations(A.5) and (A.6) define a point which lies very close to the tunnel diode characteristic and were obtained from measurements on a number of diodes (1N2941).

2. R_{d3}, given by Equation (A.7), is defined by a line joining point 4 to point V_v on the voltage axis.

3. R_{d2} passes through point (V_{fp}, I_p) and point 4.



PIECEWISE-LINEAR APPROXIMATION
OF THE TUNNEL DIODE CHARACTERISTIC.

Fig. 68.

$$Rd_1 = \frac{0.75Vp}{Ip} \qquad ..(A.1)$$

$$V_4 = \frac{(Vv + 3Vfp)}{4} \qquad ..(A.5)$$

$$I_4 = \frac{(Ip + Iv)}{3} \qquad ..(A.6)$$

$$Rd_3 = \frac{V_4 - Vv}{I_4} \qquad ..(A.7)$$

$$Rd_2 = \frac{(Vfp - V_4)}{(Ip - I_4)} \qquad ..(A.8)$$

$$V_5 = Vv + Rd_3 Iv \qquad ..(A.9)$$

4. The voltage, V_5, is the intersection of the line $1/R_{d3}$ with the level of the valley current I_v.

If this piecewise-linear approximation is applied to the analysis of the tunnel diode relaxation oscillator (Figure 24), the same equivalent circuits can be used (Figure 26), and the same equations are obtained. In the high voltage region, however, Equation (29) must be replaced by two expressions of exactly the same form but operating between different initial and ending points. Region I, II and IV are not affected (compare Figure 25 to Figure 68), and Equations (25), (27) and (31) are valid.

Region I: from 1 to 2, Figure 68.

$$t_{1-2} = \tau_1 \ln \left[\frac{(E_s - R_{t1} I_v)}{(E_s - R_{t1} I_p)} \right] \qquad .. (25)$$

Region II: from 2 to 3, Figure 68.

$$t_{2-3} = \frac{(V_{fp} - V_p)C}{(I_p - I_v)} \qquad .. (27)$$

Region IV: from 5 to 1, Figure 68.

$$t_{5-1} = \frac{(V_v - V_1)C}{(I_p - I_v)} \qquad .. (31)$$

Region IIIa: from 3 to 4, Figure 68.

If $(V'_v - R_{d2} I_v)$ is replaced by $(V_4 - R_{d2} I_4)$ in the third equivalent circuit of Figure 26, Equation (29)

gives the time from 3 to 4 as interpreted in Figure 68. It must be remembered that R_{d2} is now defined by Equation (A.8) instead of Equation (A.3) and that the initial current is still I_p but the final condition is I_4.

$$t_{3-4} = \tau_2 \ln \left[\frac{E_s - V_4 + R_{d2}I_4 - R_{t2}I_p}{E_s - V_4 + R_{d2}I_4 - R_{t2}I_4} \right] \quad .. (A.10)$$

where $\tau_2 = L_s/R_{t2}$

$R_{t2} = R_s + R_{d2}$

R_{d2} is given by Equation (A.8)

Region IIIb: from 4 to 5, Figure 68.

Following exactly the same derivation as for Region IIIa, but introducing different end conditions, Equation (A.11) is obtained.

$$t_{4-5} = \tau_3 \ln \left[\frac{E_s - V_v - R_{t3}I_4}{E_s - V_v - R_{t3}I_v} \right] \quad .. (A.11)$$

where $\tau_3 = L_s/R_{t3}$

$R_{t3} = R_s + R_{d3}$

R_{d3} given by Equation (A.7).

A comparison between the accuracy of these last expressions and that of Equations (25), (27), (29) and (31) alone, can be found in Appendix A.3.

APPENDIX A.3.

TEST ON THE ACCURACY OF THE TWO METHODS OF ANALYSIS OF THE TUNNEL DIODE RELAXATION OSCILLATOR.

Table III presents an interesting comparison between the two methods developed for the analysis of the tunnel diode relaxation oscillator.

Notes Regarding Table III.

1. The bias voltage, E_s, was obtained from a 10 volts regulated power supply through a resistance potential divider. The smaller resistance represented the external series resistance.

2. R_s = (Source resistance) + (resistance of the inductance, L_s).

3. The values of the inductances were measured at frequencies from 2 to 10 Mc/s on a Marconi Q meter.

4. T_m is the period of oscillation of the relaxation oscillator, measured on a 545A Tektronix oscilloscope. The accuracy of the time base of the oscilloscope used was checked with the aid of a frequency meter and an RF signal generator. For time bases from 10μsec/cm to .02μsec/cm, the error was always less

than ± 3% and generally of the order of 1%. The frequency meter itself was calibrated with the 200 kc/s signal emitted by the B.B.C. (Droitwich) and was found to be accurate to ± 1 division on the vernier (error less than ±.02%). The error in the measured values of T_m can therefore be considered to be less than ±3%.

5. T_{c1} and T_{c2} are the periods of oscillation computed respectively with the first and the second series of equations.

It can be seen from Table III, that both methods predict a period T_c, slightly smaller than the real value, T_m. The first method introduces an error smaller than 5% of the period for $E_s < 160$ mv. The accuracy of the second series of equations is better than the precision of the oscilloscope (±3%), even for E_s as large as 97% of the valley voltage, V_v.

				1st Method. Eqs.(25),(27),(29),(31).		2nd Method. Eqs.(25),(27),(A.10),(A.11),(31).	
E_s	R_s	L_s	T_m	T_{c1}	$100\left[\frac{T_c-T_m}{T_m}\right]$	T_{c2}	$100\left[\frac{T_c-T_m}{T_m}\right]$
mv	ohms	μh	μsec	μsec	%	μsec	%
90	5.4	1.1	.140	.134	-4.1	.135	-3.8
	5.5	5.7	.653	.651	-0.38	.653	-0.02
	5.7	24.	3.12	2.75	-11.8	2.76	-11.4
	6.7	410.	Close to stability about point V_p.				
150	5.4	1.1	.070	.0695	-.74	.070	+.06
	5.5	5.7	.316	.312	-1.2	.315	-.25
	5.7	24.	1.28	1.280	0	1.292	+.94
	6.7	410.	22.86	22.15	-3.1	22.35	-2.2
200	26.3	1.1	.086	.076	-10.9	.083	-2.8
	26.4	5.7	.389	.348	-10.6	.385	-1.0
	26.6	24.	1.725	1.463	-15.2	1.613	-6.5
	27.6	410.	30.5	28.52	-6.5	28.68	-6.0
300	26.3	1.1	.059	.046	-21.3	.061	+4.9
	26.4	5.7	.248	.190	-23.5	.2474	-.24
	26.6	24.	1.006	.7631	-24.1	1.004	-.20
	27.6	410.	17.43	16.71	-4.2	17.03	-2.3
350	26.3	1.1	No oscillation; stable close to V_v.				
	26.4	5.7	.265	.175	-34.0	.248	-.64
	26.6	24.	1.09	.700	-35.8	1.06	-3.1
	27.6	410.	18.04	16.87	-6.5	17.74	-1.7

TABLE III

Comparison of the two methods of analysis for the tunnel diode relaxation oscillator.

APPENDIX A.4.

ACCURACY OF THE ANALYTICAL EXPRESSIONS FOR THE TUNNEL DIODE RELAXATION OSCILLATOR LOADED BY A TRANSISTOR.

The accuracy of Equations (25), (27), (31), and (32) for the computation of the period of a tunnel diode relaxation oscillator loaded by a transistor, was checked using the procedure described in Appendix A.3. Table IV contains the results for two values of E_s and R_s and for three different transistors. In all cases, the error is less than the maximum inaccuracy of the measurements (±3%).

Conditions	L μh	Period T_c	Period T_m	Error $\left[\frac{T_c-T_m}{T_m}\right]100$	Remarks
E_s = 150mv R_s = 5.3Ω ASZ21	1.1 5.7 24 410	74.8nsec 335.6nsec 1.36μsec 24.11μsec	75nsec 336nsec 1.38μsec 23.95μsec	-0.3% -0.1% -1.4% +0.7%	T_m was obtained from an average of 3 measurements.
E_s = 200mv R_s = 26.2Ω ASZ21	5.7	407nsec	411nsec	-1%	
E_s = 150mv R_s = 5.3Ω 2N797	5.7 5.7	336nsec 336nsec	335nsec 345nsec	+ .3% -2.7%	2 different 2N797

TABLE IV

APPENDIX A.5.

CONSTANT CURRENT SOURCE.

The design of a constant current source with a single transistor biased in the common-base configuration presents no special difficulties. However, the mere negligence of one or two minor points may seriously increase the sensitivity of the source to temperature and supply voltage fluctuations. The circuit of Figure 69 will be analysed to illustrate this fact and its final performance as a constant current source will also be deduced. For practical purpose, the current, I_S, can be expressed by Equation (A.12).

$$I_S = \left[\frac{V_z - V_{eb}}{R_e}\right] \cdot \frac{\beta}{\beta + 1} \qquad .. (A.12)$$

where I_S = collector current in transistor TR.

V_z = voltage across the zener diode.

V_{eb} = voltage from emitter to base measured at the terminals of the transistor.

R_e = total external resistance in series with the emitter.

β = common-emitter current gain.

CONSTANT CURRENT SOURCE

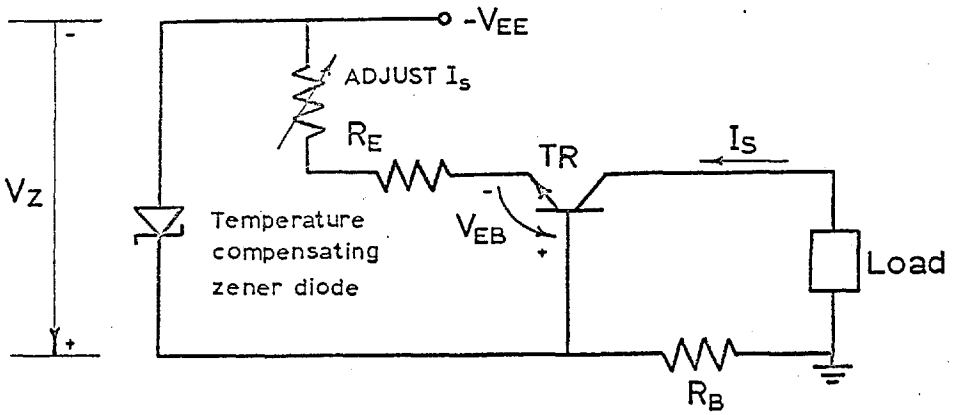


Fig. 69.

Components:

Transistor = OC139 for negative current source
OC71 for positive current source

Zener diode = OAZ208 (Mullard)

Rb = 3.9Kohms

R_{EE} = 1.38Kohms

V_{EE} = +25volts (or -25volts according to polarity of source)

Performance:

Collector Current Is = 3.3ma

Output Resistance R_{out} = 760Kohms

Thermal Coefficient $\Delta Is/\Delta T$ = +0.3μA/°C or +0.009%/°C

Sensitivity to Supply Fluctuations $\Delta Is/\Delta V_{EE}$ = +11.5μA/volt

A.5.1. Sensitivity to Supply Fluctuations.

The above expression for the current, I_s, is independent of the drift in the supply voltage, V_{EE}, in so far as the zener voltage, V_z, is constant for small changes in the diode current, I_z. If Equation (A.12) is differentiated with respect to V_{EE}, the effect of ΔV_{EE} on I_s may be found.

$$\frac{\Delta I_s}{\Delta V_{EE}} \cong \frac{R_z}{R_b R_e} \qquad .. (A.13)$$

where R_z = dynamic resistance of the zener diode.

R_b = see Figure 69.

Note that the factor $\beta/(\beta+1)$ was dropped in this last expression as it is normally negligible. The dynamic resistance, R_z, of a zener diode is usually small and the sensitivity of I_s to supply voltage fluctuations can be reduced simply by choosing R_b and R_e very large. If in the circuit of Figure 69, the position of R_b and of the zener diode were interchanged, the base voltage would be fixed at a value, V_z, above ground level. The expression for the current, I_s, would include the factor, V_{EE}, and the sensitivity of I_s to supply fluctuations would become $1/R_e$. It can be seen that Equation (A.13) gives a much smaller $\Delta I_s/\Delta V_{EE}$ owing to the extra factor R_z/R_b. This is a basic point in the bias stability of a common-base transistor but it may be easily overlooked.

A.5.2. Thermal Drift.

If now Equation (A.12) is differentiated with respect to the temperature, T, the thermal coefficient of I_s is obtained.

$$\frac{\Delta I_s}{\Delta T} \equiv \frac{1}{R_e}\left[\frac{\Delta V_z}{\Delta T} - \frac{\Delta V_{eb}}{\Delta T}\right] - I_s \cdot \frac{\Delta R_e}{\Delta T}\cdot\frac{1}{R_e} \qquad .. (A.14)$$

The factor $\beta/(\beta + 1)$ was again ignored as its effect would be negligible for normal room temperature variations. At low current levels, the presence of the leakage current, I_{co}, would have to be taken into account unless silicon transistors were used. In any case, all of these effects can be compensated over a certain temperature range by adequate adjustment of $\Delta V_z/\Delta T$. The thermal coefficient of a zener diode is a function of its zener voltage and it can be positive, negative or zero. After selection of a zener diode with approximately the right voltage, V_z, the final adjustment of $\Delta V_z/\Delta T$ may be carried out by altering the current, I_z, through the diode until the net thermal coefficient of I_s is as close to zero as desired. In most cases, there is no need to go to that extreme and the design values give satisfactory results without any further adjustment.

A.5.3. Output Impedance of the Current Source.

However, the performance of a current source depends in the first place on the magnitude of its output impedance. For a common-base transistor, Z_{out} is very large and tends rapidly towards the collector resistance, r_c, as the source resistance, R_e, is increased above a few hundred ohms[39, page 51].

A.5.4. Performance of Current Source.

An OC139 germanium transistor and an OAZ208 zener diode were used in the circuit of Figure 69 with V_{EE} = -25volts, R_b = 3.9KΩ , R_e = 1.38KΩ and R_z = 62ohms. From Equations (A.12) to (A.14), the following specifications were calculated.

Collector current	I_s	= 3.3ma
Output resistance	R_{out}	= 760KΩ
Thermal coefficient	$\Delta I_s / \Delta T$	= + 0.3 μA/°C
		or + .009%/°C

Sensitivity to supply fluctuations

$$\Delta I_s / \Delta V_{EE} = +11.5\ \mu A/volt$$

These results were checked experimentally on two circuits using different sets of components and they were found to agree closely with the measured performance.

If the regulated supply voltage is adjusted after a warm-up period of 30 minutes, the maximum drift in a day was found never to exceed 10mv and has a typical value of 2 to 5mv. It means that the maximum effect on I_S is equal to 0.12μA or .0035% in a day. The thermal coefficient of the current source is three times larger and constitutes the main cause of the drift in I_S.

APPENDIX A.6.

TRIMMING OF THE TUNNEL DIODE CHAIN FOR IMPROVED ACCURACY.

The magnitude of the voltage steps generated by a tunnel diode chain can be adjusted independently of one another by the addition of individual resistances across the diodes. A qualitative description of the underlying principle is given in section 2.3.6., and is self-explanatory in relation with Figures 70 and 71. In order to derive simple equations for the amount of trimming introduced by a resistance, R_p, a linear approximation of the tunnel diode characteristic will be utilized as in Figure 72. From that figure, the following equations can be written.

Voltage step before trimming = $V_3 - V_1$ .. (A.15)

Voltage step after trimming = $V_4 - V_2$ .. (A.16)

Correction in voltage step = (Step after trimming) - (Step before trimming)

Correction = $(V_4-V_2) - (V_3-V_1)$

or Correction = $(V_1-V_2) - (V_3-V_4)$ .. (A.17)

The first term, (V_1-V_2), is the change in the low voltage state caused by the shunting of part of I_s through the resistance, R_p.

$$V_1-V_2 = R_{d1}\left[\frac{R_{d1}}{R_{d1} + R_p}\right].I_s \qquad .. (A.18)$$

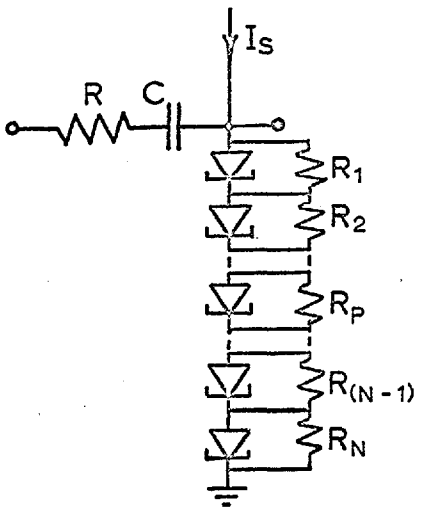


Fig. 70.

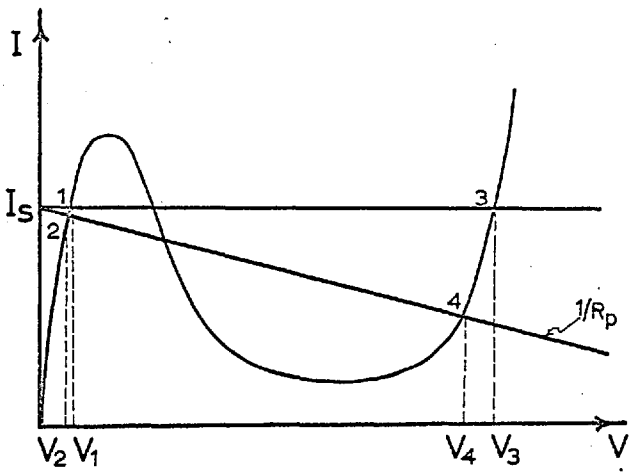


Fig. 71.

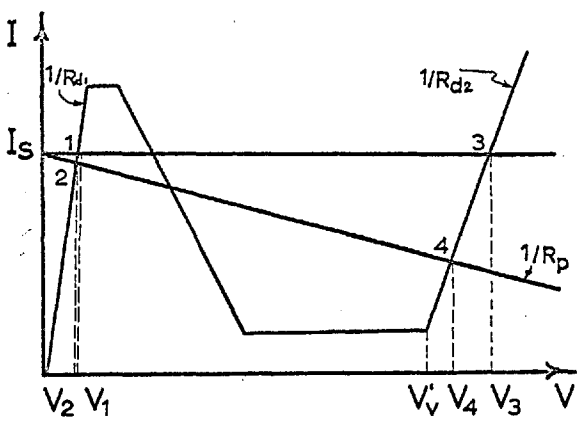


Fig. 72.

Similarly, the second term, (V_3-V_4), represents the decrease in the high voltage state due to the diversion of a current, I_{rp}, by the resistance, R_p. An expression for the current, I_{rp}, can be written directly from Figure 72 with the help of the simple parallel resistance concept.

$$I_{rp} = \frac{V'_v - R_{d2}I_v}{R_p} + \left[I_s - \left(\frac{V'_v - R_{d2}I_v}{R_p}\right)\right] \frac{R_{d2}}{R_{d2} + R_p}$$

or $$I_{rp} = \frac{V'_v - R_{d2}I_v}{R_{d2} + R_p} + \frac{R_{d2}}{R_{d2} + R_p} . I_s \qquad .. (A.19)$$

The second term, V_3-V_4, of Equation (A.17), is therefore the product of the resistance, R_{d2}, with I_{rp}.

$$V_3 - V_4 = R_{d2} \left[\frac{V'_v - R_{d2}I_v}{R_{d2} + R_p} + \frac{R_{d2}I_s}{R_{d2} + R_p}\right] \qquad .. (A.20)$$

Replacement of Equations (A.20) and (A.18) into Equation (A.17), leads to the expression (A.21) for the voltage correction produced by a trimming resistance, R_p.

$$\text{Correction} = R_{d1} \left[\frac{R_{d1}}{R_{d1} + R_p}\right] I_s - R_{d2} \left[\frac{R_{d2}}{R_{d2} + R_p}\right] (I_s - I_v) - \frac{R_{d2}}{R_{d2} + R_p} . V'_v \qquad .. (A.21)$$

The trimming obtained from two possible values of the resistance, R_p, were calculated from Equation (A.21). The characteristics of a typical 1N2941 tunnel diode are given in Appendix A.9 and the parameters, R_{d1}, R_{d2} and V'_v, were

derived from Equations (A.1), (A.3) and (A.2) of Appendix A.1. The results are listed in Table V for I_s = 3.3ma.

R_p	Correction of Voltage Step.	
ohms	mv	%
1000	-8	-1.9
470	-17.15	-3.9

TABLE V

It was found in practice that the above results were slightly optimistic as a consequence of the particular equivalent characteristic used for the tunnel diodes. In the regions of interest, the actual magnitudes of the dynamic resistances of the diodes are smaller than their linear replacements R_{d1} and R_{d2} defined by Equations (A.1) and (A.3) in Appendix A.1. The equivalent characteristic shown in Figure 72, was intended for switching problems and the present application would necessitate new definitions of its parameters. However, the trimming resistances have to be adjusted experimentally and there is no need for more accurate equations. Measurements have shown that a resistance of 470Ω would in fact reduce the step by about -2% instead of -3.9%. Resistances smaller than 470Ω can be used as long as their approximate values are taken into account while

selecting for peak currents. In this case, the diverted current, I_{rp}, for $v = V_p$, should be added to I_p to find the effective peak current of a diode in the chain.

APPENDIX A.7.

CHARACTERISTICS OF THE TUNNEL DIODE CHAINS.

Chain No. 6B			1st Stage -ve	
Diode No.	I_p ma	ΔI_p μa	Steps mv	ΣDev. mv
51	4.526		446.7	-19.1
54	4.618	92	458.9	-26.0
43	4.647	29	464.5	-27.3
25	4.695	48	457	-36.1
34	4.739	44	462	-39.9
72	4.788	49	475	-30.7
71	4.859	71	485	-11.5
44	4.887	28	489	-11.7
59	4.912	25	454	- 0.1
35	5.100	88	---	----

All values measured at T = 22.2° C.

Average step = 465.8mv

Minimum = 446.7mv (-4.10%)

Maximum = 489mv (+4.98%)

Acceptable input pulse range: 3.2volts ±13%

CHARACTERISTICS OF THE TUNNEL DIODE CHAINS.

Chain No. 7B			1st Stage +ve	
Diode No.	I_p ma	ΔI_p μ a	Steps mv	ΣDev. mv
62	4.558		465.5	-2.5
70	4.584	26	471.5	+1.0
27	4.622	38	471	+4
61	4.675	53	472	+8
53	4.723	48	470	+10
74	4.747	24	467	+9
48	4.795	48	460	+1
50	4.839	44	477	+10
64	4.843	4	458	0
47	4.896	57	---	---

All values measured at T = 22.2° C.

Average step = 468.0mv

Minimum step = 458mv (-2.14%)

Maximum step = 477mv (+1.92%)

Acceptable input pulse range: 3.0volts ±20%

CHARACTERISTICS OF THE TUNNEL DIODE CHAINS.

Chain No. 3B			2nd Stage -ve	
Diode No.	I_p ma	ΔI_p μa	Steps mv	Σ Dev. mv
38*	4.442		463.7	+2.9
11	4.555	113	461.4	+3.5
63	4.610	55	456	-1.3
6	4.670	60	456	-6.1
7	4.766	96	465	-1.9
68	4.792	26	461	-1.7
32	4.839	47	465	+2.5
40**	4.928	89	463	+4.7
46	4.956	28	456	-0.1
49	5.008	42	---	----

All values measured at T = 22.33° C.

Average step = 460.8mv

Minimum step = 456mv (-1.04%)

Maximum step = 465mv (+0.91%)

Acceptable input pulse range: 3.2volts ±11%

* Diode No. 38 trimmed with 680ohms.

** Diode No. 40 trimmed with 470ohms and also with 15pf to ground.

CHARACTERISTICS OF THE TUNNEL DIODE CHAINS.

Chain No. 5B			2nd Stage +ve	
Diode No.	I_p ma	ΔI_p μ a	Steps mv	Σ Dev. mv
55	4.301		485.3	+1.2
57	4.398	97	483.6	+0.7
60	4.458	60	487	+3.6
42	4.526	68	480	-0.5
39	4.566	40	482	-2.6
45	4.655	89	488	+1.3
69	4.917	262	480	-2.8
58	4.956	39	489	+2.1
28	4.968	12	482	0
10	4.852	-116	---	---

All values measured at T = 22.3° C.

Average step = 484.1mv

Minimum step = 480mv (-0.85%)

Maximum step = 489mv (+1.01%)

Acceptable input pulse range: 3.2volts ±13%

APPENDIX A.8.

MEASUREMENTS OF THE THERMAL COEFFICIENTS OF THE CHAINS.

The following measurements were taken on the four tunnel diode chains described in Appendix A.7.

Chain No.	$\overline{V}_s$ *	$\frac{\Delta E_o}{\Delta T}$ **	$\frac{\Delta e_o}{\Delta T}$ ***	$\frac{\Delta e_o}{(e_s - E_o)\Delta T}$
	mv	mv/°C	mv/°C	%/°C
7-B	467.2	+0.408	-8.67	-0.206
6-B	465.0	+0.587	-8.73	-0.209
5-B	483.4	+0.336	-8.70	-0.200
3-B	459.7	+0.430	-9.28	-0.224

TABLE VI

* $\overline{V}_s$ = Average step at T = 23°C.

** $\Delta E_o / \Delta T$ = Temperature coefficient of the output voltage of a chain measured when all tunnel diodes are in the low voltage state.

*** $\Delta e_o / \Delta T$ = Temperature coefficient of the output voltage of a chain measured when nine of the tunnel diodes are already in the high voltage state and the remaining one lies in the low voltage state.

To obtain the results of Table VI, all voltages were measured with a digital voltmeter on a scale giving an accuracy better than ±1mv. The temperature was monitored with a thermometer graduated to 0.1°C and sufficient time was allowed before the readings for thermal stability to be attained. It has been estimated that the precision on the temperature coefficients would be of the order of ±3%. This limit was imposed mainly by the temperature measurements. The values given in Table VI represent the averages of the results from three or four series of measurements taken on every chain.

The temperature coefficients, D_L and D_H, described in section 3.3. for a tunnel diode in a chain, can now be checked against experimental results. From the column of $\Delta E_o/\Delta T$, it can be seen that D_L ranges from +34μV/°C to +60μV/°C, suggesting that in all cases, the effect of negative $\Delta I_p/\Delta T$ is dominating over that of $\Delta V_p/\Delta T$. Similarly, combining $\Delta E_o/\Delta T$ with $\Delta e_o/\Delta T$ and dividing by 9, the magnitude of D_H is found to lie between -0.97mv/°C to -1.04mv/°C. The theoretical value was chosen equal to -1.0mv/°C.

Before the temperature coefficients of Table VI can be compared with one another, they must be normalized. The average step of chain No. 6-B was chosen as the standard and the transformed coefficients are given in Table VII.

Chain No.	W. *	Normalized Results	
		$\Delta E_o / \Delta T$ mv/°C	$\Delta e_o / \Delta T$ mv/°C
7-B 1st Stage +ve	1.00473	+0.406	-8.63
6-B 1st Stage -ve	1.	+0.587	-8.73
5-B 2nd Stage +ve	0.10396	+3.23	-83.7
3-B 2nd Stage -ve	0.09886	+4.35	-93.9

TABLE VII

* W = weighing factor taking into account the differences between the average steps of the chains. It also includes the factor of ten used in the weighing resistors to make the steps in the second decades proportionally larger.

The values listed in Table VII can be used directly for the calculation of the compensation effect between the chains of opposite polarities in the same decades. Table VIII shows the net thermal drift of the zero output from the Staircase Reference Unit when the chains are either all at zero or all at the 9th level.

Decade	$\Delta E_o / \Delta T$ mv/°C	$\Delta E_o / \overline{V_s} \Delta T$ %/°C	$\Delta e_o / \Delta T$ mv/°C	$\Delta e_o / \overline{V_s} \Delta T$ %/°C
1st Stage	-0.181	-0.04	+0.10	+0.022
2nd Stage	-1.12	-0.24	+10.2	+2.2

TABLE VIII

From Table VIII, it can be seen that the compensation effect between the chains constitutes an efficient means of reducing the sensitivity of the Reference Unit to temperature fluctuations. For instance, a rise of 10°C in the temperature would shift the zero by less than -3% of the Unit step. In the worst case, when the zero output is defined by the difference between two full chains, the drift would still be only +2.2% of the Unit step per degree Centigrade rise in the temperature.

The maximum absolute thermal drift in the staircase generator output is produced at full scale when one side is at the 99th level while the other is at zero. From Table VII, a value of -0.23% of full scale per degree Centigrade can be computed for this condition. It was shown in section 3.3, that this figure (-0.23% of output level per degree C) is maintained for most of the range of the staircase waveform. The compensation effect illustrated by the results of Table VIII is efficient enough to justify the hypothesis used for the derivation of Equation (52) in section 3.3.

APPENDIX A.9.

TUNNEL DIODE SPECIFICATIONS.

Electrical Characteristics of the 1N2941 Tunnel Diode at 25°C.

		Min.	Typ.	Max.	
Peak Point Current	I_p	4.2	4.7	5.2	ma
Valley Point Current	I_v		0.6	1.04	ma
Peak Point Voltage	V_p		60		mv
Valley Point Voltage	V_v		350		mv
Forward peak point Voltage	V_{fp}	450	500	600	mv
Negative conductance	$-G$		30×10^{-3}		mho
Total capacity	C		15	50	pf
Series Inductance (Leads 1/8")	L_s		6×10^{-9}		henries
Series Resistance.	R_s		0.5	2.0	ohms

APPENDIX A.10.

TRANSIENT RESPONSE OF THE RESETTING TRANSISTOR.

Three fundamental methods are generally accepted for computing the transient response of a given transistor in a given circuit[41, Chapter 6]. These are: the equivalent circuit approach, the charge control analysis, and the diffusion equation solution. A number of variations of the first approach, for instance, may be used depending on the application considered. The equations adopted here, to compute the switching times of the transistors, are described in Chapter 4 of the reference 42. They were derived for constant current drive but can still serve as useful approximations in the present case.

A.10.1. Current Available from Monopulser.

When a transistor is connected to a tunnel diode monopulser as in Figures 27 or 31, the drive on the base of the transistor cannot be classified as a true current or voltage source. On the other hand, the transistor can be considered advantageously as a current operated device and the tunnel diode itself was defined in terms of currents throughout the design of the monopulser. The amount of charge fed into the base of the transistor during the

switching of the tunnel diode, may be expressed in a number of ways. If, for instance, a constant current applied to the base, can supply the same amount of charge in the same time, the switching time of the transistor is not changed. In the following analysis, the charge available from the tunnel diode, was transformed in each case into an equivalent constant current drive in order to use the simple equations of reference 42 to compute the switching times of the transistor.

Figure 30 can serve as a guide to investigate the forward drive current, I_{bf} , and the reverse drive current, I_{br}, supplied by the tunnel diode to the base of the transistor. The time delay introduced by the transistor before the collector starts switching on, is of the order of a few nanoseconds (see data sheets for ASZ21 and 2N797), and the tunnel diode will be close to the high voltage state within that time. As long as the transistor risetime is much shorter than the pulse width of the monopulser, the relevant forward base current to switch the transistor "on", may be expressed as $(\underline{I_a} - \overline{I_v})$ or 2.16ma. A value of I_{bf} = 2ma can be chosen.

The reverse drive current, I_{br}, is slightly more difficult to determine because it is applied for a very short time. The peak amplitude of that reverse current is $(\underline{I_p} - \overline{I_v})$ or 3.16ma. The slope of the tunnel diode characteristic suggests a simple way of estimating the

equivalent constant current drive for the "switching off" of the transistor. Firstly, the representation of the reverse current as a function of time may be approximated by a triangle of base t_1 and of height I_h = 3.16ma. In line with the assumptions made for the analysis of the monopulser, the switching time between points 5 and 6 (Figure 30), is a linear function of the voltage (i.e. constant current switching). In this case, the base t_1 of the triangle would be proportional to $2V_p$ or 120mv. If it is noted that V_{tr} is about three times as large (V_{tr} = 400mv), it can be said that the equivalent constant current reverse drive would be applied for a duration $3t_1$. But the height of a rectangle of base $3t_1$ must be 1/6 of that of a triangle of base t_1 if their surfaces are equal. The constant reverse current drive can therefore be taken as 3.16ma divided by 6 or $I_{br} \cong 0.5$ma.

A.10.2. Risetime at the Output of the Chain.

The approximate risetime at the output of the chain when the resetting transistor is being switched on, can be computed in two steps. Assume first that the discharge of the total parallel capacitance, C_t, across the chain takes place at constant current; the corresponding time may be extracted from Equation (A.22).

$$\underline{I_c} - \overline{I_s} = C_t \frac{\Delta V}{\Delta t} \qquad .. \text{(A.22)}$$

However, the low impedance of the chain in parallel with the resetting transistor in fact causes the discharge to be an exponential with a time constant computed from Equation (A.22). The risetime at the output of the chain is therefore approximately three such time constants (95% of the discharge) if a true exponential is assumed. The minimum collector current (for use in Equation (A.22)) for a forward base drive, I_{bf}, equal to 2ma, depends on the current gain of the transistor. Because the transistors used have normal risetimes much shorter than the pulse width of the monopulser, the most representative value of β may be chosen as the d-c value to the edge of the saturation region. The specified minimum h_{fe} for ASZ21 transistors at V_{ce} = -2volts and I_c = 10ma is 35. A design value of $\underline{\beta_o}$ = 15 has been used throughout the computation, unless otherwise stated, in order to keep a safe margin. The resulting $\underline{I_c}$ is 15 x 2ma or 30ma. From Figure 31, the total parallel capacitance C_t may be estimated as 100pf. From Equation (A.22), using ΔV = 10 x 0.5 = 5volts, and $\overline{I_s}$ = 3.4ma, Δt equals 18.8nsec. The risetime at the output of the chain is therefore equal to 3 x 18.8 = 56nsec. The measured value under the same conditions using a sampling oscilloscope was about 50nsec (see Figure 73).

RESETTING TIME OF TUNNEL DIODE CHAINS

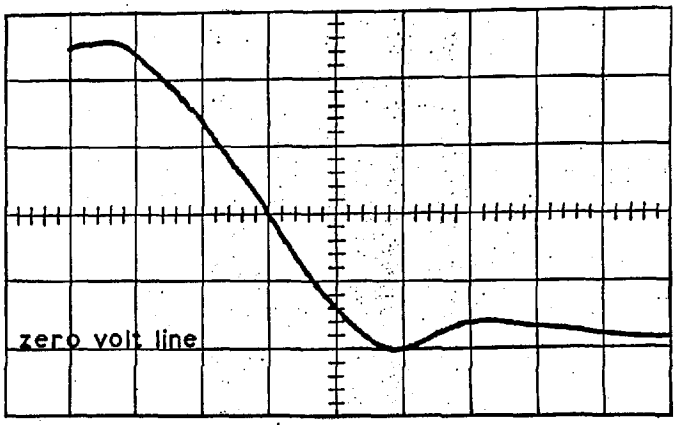


Fig. 73.

Trace. Voltage step appearing across a positive tunnel diode chain when resetting to zero.

Scales. Horizontal: 10 nsec/cm

Vertical : 1 volt/cm

Notes. 1- Sampling oscilloscope was used (see note 2, figure 37.)

2- High impedance probe used: 50x, 10Mohms, 1.8pf. Oscilloscope was triggered externally on the same waveform with a 5.6pf capacitor.

3- This photograph represents the first positive decade driving the following stage normally.

A.10.3. "Switching On" of the Resetting Transistor.

It has been assumed for the computation of the risetime at the output of the chain that the transistor could switch on in a time considerably shorter than the 0.1μsec pulse width of the monopulser. This hypothesis will now be verified.

The expression obtained from reference 42 for the risetime of the current at the collector of a transistor is given in Equation (A.23).

$$t_r = T_{ce} \ln \left[\frac{I_{bf}. \beta_o}{I_{bf} \beta_o - I_c} \right] \quad .. (A.23)$$

$$T_{ce} = \frac{\beta_o}{2\pi f_{\alpha co}} \quad .. (A.24)$$

Where t_r = time for the collector current of a transistor to rise from zero to a value I_c.

β_o = common-emitter d-c. current gain to the edge of saturation for a base current equal to I_{bf}

I_{bf} = constant forward base current.

$f_{\alpha co}$ = alpha cut-off frequency, the frequency at which the common-base current gain has fallen to $1/\sqrt{2}$ of its low frequency value.

For most high speed switching transistors, the alpha cut-off frequency is not given in the data sheet. Instead, the frequency, f_T (sometimes called f_1), at which the common-emitter current gain, β, has fallen to 1, is specified. Using the well known relationships $\beta_o = \alpha_o/(1 - \alpha_o)$ and $|\beta| = \beta_o/\sqrt{1 + [f/f_{\alpha co}(1 - \alpha_o)]^2}$, it can be shown that f_T is a good approximation of $f_{\alpha co}$. These expressions are valid for an idealized transistor in which $\alpha = \alpha_o/(1 + jf/f_\alpha)$. In fact, most high speed switching transistors contain an accelerating field in the base region. In such cases, the above equalities must be corrected by the introduction of an "excess phase factor". The alpha cut-off frequency is then generally equal to 1.4 to 2.5 times f_T, depending on the magnitude of the excess phase factor[43, page 12-13; 44, page 49]. Nevertheless, in the following calculations of the switching times of the transistors, the alpha cut-off frequency, $f_{\alpha co}$, was chosen equal to f_T, as no information was readily available regarding the magnitude of the excess phase factors for the transistors used. This simplification is justified because the present analysis aims at determining the maximum possible switching times of the transistors under the worst conditions. The choice of a smaller value for $f_{\alpha co}$ therefore ensures that the results are always on the safe side. For the ASZ21 and the

2N797, the minimum f_T specified for typical biasing conditions are respectively 300Mc/s and 600Mc/s. A rise-time, t_r = 9.8nsec, may be obtained according to Equation (A.23), for an ASZ21 transistor, with $I_c = 30ma/\sqrt{2}$, I_{bf} = 2ma, and $\beta_o = 15$. The full value of collector current, I_c = 30ma, must not be used in Equation (A.23) because it was obtained from the same values I_{bf} and β_o employed in that expression, and would give a time, t_r, equal to infinity. Equation (A.23) may be used directly only when I_{bf} corresponds to an over-drive current for the chosen values of I_c and β_o. The transistor response in the present condition is certainly much shorter than the pulse width of the monopulser and the assumptions made previously in that respect were justified.

It has been seen up to now that the collector current of the resetting transistor increases from 0 to 21ma in less than 10nsec after the switching of the mono-pulser and that the discharge of C_t should be completed in less than 60nsec. One more condition must be met to ensure complete resetting of all the tunnel diodes in the chain: $\overline{V_{ce}}(sat) < \underline{V_D} \times 10$ or $\overline{V_{ce}}(sat) < 500mv$, for $I_c \cong \overline{I_s}$. Both the ASZ21 and the 2N797 satisfy that requirement with specified maximum saturation voltages, for I_c = 10ma, of 350mv and 140mv respectively.

A.10.4. "Switching Off" the Resetting Transistor.

At the end of the signal from the monopulser, the resetting transistor must cut off rapidly for the chain to be ready for the next input pulse.

Just before the monopulser switches back to the low voltage state, the current in the tunnel diode has decreased to I_v and the voltage across the input of the transistor is V_v. Assuming $\overline{V_v}$ = 380mv, the V_{be} vs I_b curve for the ASZ21 transistor gives a base current, for that voltage, of the order of 0.2ma. The worst conditions will be met with a transistor displaying a large current gain. If β_o = 50 is chosen, the corresponding collector current would be 10ma and the transistor would be in saturation because the current could be limited to $\underline{I_s}$ = 3.2ma. In that case, the storage time, t_{sd}, may be computed from Equation (A.25).

$$t_{sd} = T_s . \ln\left[\frac{\beta_o I_{b1} - \beta_o I_{b2}}{I_c - \beta_o I_{b2}}\right] \qquad .. (A.25)$$

where t_{sd} = storage time of the transistor defined as the time for the transistor to come out of saturation under the prevailing circuit conditions.

T_s = inverted time constant of the transistor measured when the collector is used as an

emitter and vice versa. A conservative value of 50nsec was used for both types of transistor. T_s was taken as the storage time of the ASZ21 without reverse drive. Equation 4.30 on page 4-81 of reference 42 may be used to show that this assumption is justified in the present case.

I_{b1} = forward base current just before the application of the reverse drive.

I_{b2} = constant reverse base current drive.

I_c = collector current just at the edge of saturation = $\underline{I_s}$.

For an ASZ21, using values already computed, $I_{b1} = -0.2$ma, $I_{b2} = I_{br} = 0.5$ma, $\beta_o = 50$, $T_s = 50$nsec, and $I_c = \underline{I_s} = 3.2$ma, the storage time is given by Equation (A.25) as $t_{sd} = 10.8$nsec. It should be noted that, if the transistor is still in saturation when the valley point of the tunnel diode is reached, the switching time of the monopulser to the low voltage state, given by Equation (31), is increased by a few nanoseconds.

The turn off time, t_f, may be computed from Equation (A.26).

$$t_f = T_{ce} \cdot \ln\left[\frac{\beta_o I_{BR} - I_{c1}}{\beta_o I_{BR}}\right] \qquad .. (A.26)$$

where t_f = turn off time of the transistor from the edge of saturation.

β_o = common-emitter d-c current gain estimated at the edge of saturation for a forward base current equal to I_{br}.

I_{br} = constant reverse base current drive.

I_{cl} = collector current at the edge of saturation.

If the following values are used, $\beta_o = 15$, $I_{br} = 0.5$ma, $T_{ce} = 8$nsec, $I_{cl} = 3.2$ma, the turn off time becomes $t_f = 2.8$nsec. The transistor is therefore cut off in approximately $t_{sd} + t_f = 14$nsec after the valley point has been reached in the monopulser.

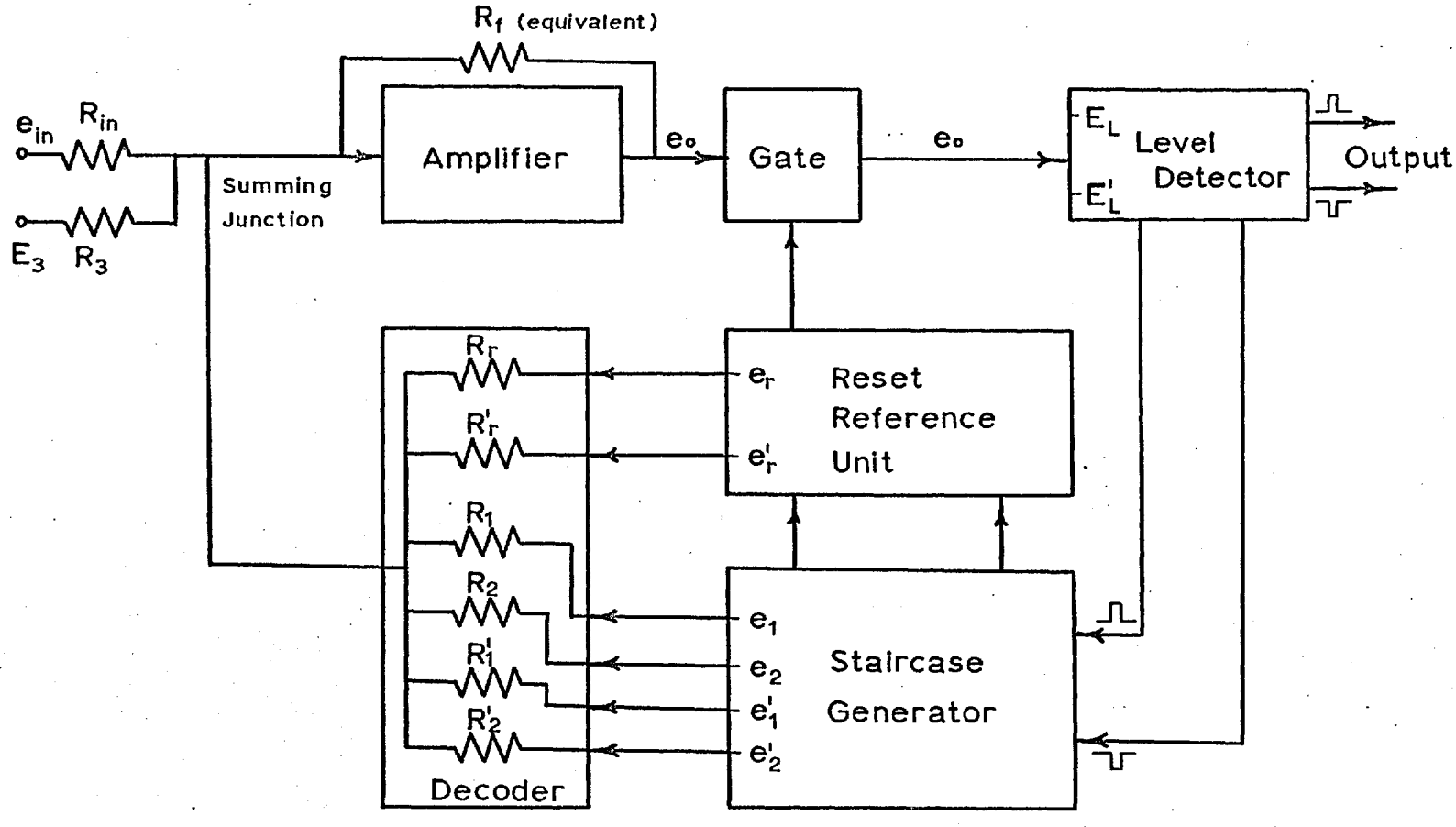
It can therefore be concluded that the resetting of the chain is completed after a time equal to the summation of the monostable pulse width plus the total "switch off" time of the transistor or 0.1 + 0.014 = 0.114μsec. The computatiom is not repeated for the 2N797 because this transistor has a cut-off frequency twice as high as that of the ASZ21 and its transient response is even shorter.

APPENDIX A.11.

ANALYSIS OF PRECISION REQUIREMENTS IN THE QUANTIZER.

In this appendix, the precision requirements in the quantizer are investigated using the block diagram of Figure 74. The ultimate aim is to derive an expression for the required tolerance and linearity of the staircase generator as a function of all causes of inaccuracy introduced by auxiliary units in the quantizer. It is convenient to center the analysis round the amplifier unit and a basic equation is established at first, relating the output voltage, e_o, to the summation of input and reference voltages. This equation is then divided in two parts. The first one represents the zero conditions in the quantizer and it is used to establish expressions for E_z and its range of adjustment, leading to the design of the set zero circuit. The second part is obtained by adjusting E_z to cancel out the zero condition terms in the basic equation.

From this second expression, all precision requirements are derived to meet the following general condition: no overload of the summing amplifier can occur at any time when an arbitrarily slow input voltage ramp sweeps the quantizer over its full range of operation.



BLOCK DIAGRAM FOR ANALYSIS OF QUANTIZER

Fig. 74.

At first, the maximum acceptable deviations, X_1 and X_2, of the steps in each chain are investigated assuming that no cycling action occurs. Following a similar approach, the precision requirements during the cycling process are studied in three parts: firstly, when the Reset Reference Unit is switched on, secondly, during the stepping up of both chains simultaneously, thirdly, when the Reset Reference Unit is switched off. It will be seen that the most general expression is obtained from the second subdivision.

A.11.1. List of Symbols.

The following list of symbols is intended for use in Appendix A.11 and A.12., and does not necessarily apply elsewhere. The symbols (mostly illustrated in Figure 74) appear in the list in logical order from input to output and back via the feedback loop. Capital letters are assigned to nominal and to maximum values and lowercase letters, to instantaneous magnitudes of variables. Only symbols describing positive quantities have been listed. The quantizer being symmetrical, the negative equivalents are to be obtained by the addition of an apostrophe to the corresponding positive symbols (e.g. A and A'). All resistors are marked in the same way as the corresponding voltages, the symbols being indicated on Figure 74.

e_{in} = instantaneous value of input voltage signal.

E_{in} = a value of input signal equal to an exact multiple of the quantization interval.

E_z = nominal value of correction voltage at the input used to adjust the zero level of the quantizer.

X_z = maximum relative drift of E_z from its nominal value.

G = R_F/R_{in}, basic voltage gain of summing amplifier (defined as a function of R_{in}). This gain is assumed constant as any drift would be included in E_d.

e_o = instantaneous value of output voltage from amplifier including noise and drift.

E_d = maximum voltage drift appearing at the output of the summing amplifier for a constant input signal and for a given temperature range. (Does not include drift due to weighing resistors).

E_n = peak amplitude of the noise at the output of the summing amplifier.

X_n = fractional equivalent noise in the summing amplifier as referred to the input of the quantizer.

e_L = instantaneous value of the positive voltage level actually detected by the level detector (including drift in the detector).

E_L = nominal value of the positive voltage level detected by the level detector unit.

E_{dL} = maximum voltage drift on the positive side of the level detector as referred to its input including thermal effects and error of adjustment.

X_L = fractional equivalent drift due to the level detector as referred to the input of the quantizer.

e_1 = instantaneous voltage output from the first decade on the positive side of the staircase generator.

e_2 = instantaneous voltage output from the second decade on the positive side of the staircase generator.

E_{10} = nominal voltage at the output of the first positive decade in the staircase generator corresponding to the zero level for that chain at the chosen standard temperature.

E_{20} = nominal voltage at the output of the second positive decade in the staircase generator corresponding to the zero level for that chain at the chosen standard temperature.

X_{10} = maximum relative drift in E_{10}.

X_{20} = maximum relative drift in E_{20}.

E_1 = nominal value of the average voltage step for the first positive decade in the staircase generator at the chosen standard temperature.

E_2 = nominal value of the average voltage step for the second positive decade in the staircase generator at the chosen standard temperature.

n_1 and n_2 = see notes at end of section A.11.2.

X_1 = maximum relative deviation from E_1 of any of the steps in the first positive decade.

X_2 = maximum relative deviation from E_2 of any of the steps in the second positive decade.

X_{1d} = magnitude of X_1 when the first positive decade is at the 9th level (to be used only with the corresponding value of $n_1 = 9$).

X_{2d} = magnitude of X_2 when the second positive decade is at the 9th level (to be used only with the corresponding value of $n_2 = 9$).

x_{1a} = maximum relative deviation from E_1 of any of the steps in the first positive decade at the chosen standard temperature.

e_r = instantaneous value of the quiescent voltage on the positive side of the Reset Reference Unit. (The side generating a positive pulse during the cycling process).

E_{ro} = nominal value of e_r.

E_{rd} = maximum value of the voltage drift of e_r from E_{ro}.

E_r = nominal amplitude of the positive voltage pulse generated by the Reset Reference Unit.

X_r = maximum relative drift from E_r of the positive pulse generated by the Reset Reference Unit.

q = E_L/G, voltage amplitude equal to one quantization interval as referred to the input of the quantizer.

A.11.2. Basic Equation.

The following analysis of the quantizer is derived from a fundamental expression relating the output of the summing amplifier to its inputs. Equation (A.27) can be written directly from Figure 74, remembering that $G = R_f/R_{in}$.

$$e_o = G\left\{e_{in} + R_{in}\left[\frac{E_3(1\pm X_3)}{R_3} + \frac{e_1}{R_1} - \frac{e_1'}{R_1'} + \frac{e_2}{R_2} - \frac{e_2'}{R_2'} - \frac{e_r}{R_r} + \frac{e_r'}{R_r'}\right] \pm E_d + E_n\right\} \quad ..(A.27)$$

General Notes.

1. The voltage symbols in the various equations represent absolute values and their signs are taken into account in the equations themselves.

2. For simplicity reason, the double signs (±) preceding E_n, E_d, E_{rd} and all Xs (see Equation (A.31)), have been replaced in the following equations by single positive signs. It is therefore assumed that these particular symbols can take both positive or

negative values. For the derivations, their signs have been chosen in a way corresponding to worst-case conditions.

The instantaneous voltages contained in Equation (A.27) can be expressed as functions of their nominal values plus or minus drift terms. Only those equations describing the positive half of the quantizer have been listed for reasons given before (section A.11.1.).

$$e_1 = E_{10}(1 + X_{10}) + n_1 E_1(1 + X_1) \qquad .. (A.28)$$

$$e_2 = E_{20}(1 + X_{20}) + n_2 E_2(1 + X_2) \qquad .. (A.29)$$

$$e_r = E_{ro} + E_{rd} \qquad .. (A.30)$$

Replacing Equations (A.28) to (A.30) into Equation (A.27) yields Equation (A.31).

$$e_o = GR_{in}\left[\frac{E_3(1 + X_3)}{R_3} + \frac{E_{10}(1 + X_{10})}{R_1} - \frac{E'_{10}(1 + X'_{10})}{R'_1}\right.$$

$$+ \frac{E_{20}(1 + X_{20})}{R_2} - \frac{E'_{20}(1 + X'_{20})}{R'_2} - \frac{E_{ro} + E_{rd}}{R_r}$$

$$\left. + \frac{E'_{ro} + E'_{rd}}{R'_r}\right] \qquad .. (A.31)$$

Equation (A.31) continued on next page.

End of equation (A.31).

$$+ G\left\{e_{in} + R_{in}\left[\frac{n_1E_1(1 + X_1)}{R_1} - \frac{n_1'E_1'(1 + X_1')}{R_1'} + \frac{n_2E_2(1 + X_2)}{R_2} - \frac{n_2'E_2'(1 + X_2')}{R_2'}\right]\right\} + E_d + E_n \quad ..(A.31)$$

Notes on Equations (A.28) to (A.31).

1. The factors n_1, n_2, n_1' and n_2' are integers whose values depend on the levels reached by the corresponding chains of the staircase generator. In the terms n_1E_1, n_2E_2, $n_1'E_1'$ and $n_2'E_2'$, the multiplying factors, n, can vary from 0 to 9.

2. Choosing the magnitude of n in the terms of the same type as $n_1E_1X_1$, for instance, necessitates some knowledge of the various components of X_1. For the part of X_1 due to the thermal coefficient of E_1, n is the same as for the related term n_1E_1 (see note 1). On the other hand, it is safe to assume that in the worst case, the deviations of the steps from their average, E_1, are equal to the maximum, x_{1a}, and are positive for the first five steps and negative for the remaining ones. Consequently, the magnitude of n cannot exceed 5 in the terms similar to n_1x_{1a}.

3. Equation (A.31) is valid for normal operation of the stepping reference unit as long as the cycling process is not initiated.

4. The tolerances and drifts of the resistors in Equation (A.31) and in the remaining derivations are included in the corresponding X appearing in each term. It can be shown that, as a first approximation, these factors belonging normally to the denominators can be added directly to the numerators of the same expressions.

A.11.3. Computation of Zero Conditions.

The first part of Equation (A.31) describes the zero conditions in the quantizer when $e_{in} = 0$ and all chains are at the zero level ($n_1 = n_2 = n_1' = n_2' = 0$). In this case, the second part is reduced to zero and the output voltage, e_{oo}, from the summing amplifier is given by Equation (A.32).

$$e_{oo} = GR_{ir}\left[\frac{E_3}{R_3} + \frac{E_{10}}{R_1} - \frac{E'_{10}}{R'_1} + \frac{E_{20}}{R_2} - \frac{E'_{20}}{R'_2} - \frac{E_{ro}}{R_r} + \frac{E'_{ro}}{R'_r}\right]$$

$$+ GR_{in}\left[\frac{X_3E_3}{R_3} + \frac{X_{10}E_{10}}{R_1} - \frac{X'_{10}E'_{10}}{R'_1} + \frac{X_{20}E_{20}}{R_2} - \frac{X'_{20}E'_{20}}{R'_2}\right.$$

$$\left. - \frac{E_{rd}}{R_r} + \frac{E'_{rd}}{R'_r}\right] + E_d + E_n \qquad .. (A.32)$$

A.11.3.1. Nominal Value of E_3.

The nominal value for the voltage, E_3, necessary to reduce e_{oo} to zero under ideal conditions can

be obtained from Equation (A.32) simplified as follows:

1. $X_3 = X_{10} = X'_{10} = X_{20} = X'_{20} = 0$

2. $E_{rd} = E'_{rd} = 0$

3. $E_n = 0$ This term cannot be corrected by E_3 in any case.

4. $E_d = 0$ The long term drift can be compensated by adjusting E_3.

$$E_3 = - R_3\left[\frac{E_{10}}{R_1} - \frac{E'_{10}}{R'_1} + \frac{E_{20}}{R_2} - \frac{E'_{20}}{R'_2} - \frac{E_{ro}}{R_r} + \frac{E'_{ro}}{R'_r}\right] \quad .. \text{(A.33)}$$

The magnitude of E_3 is different from zero because the resistors are adjusted according to the average steps of each chain (Appendix A.7) and are not necessarily proportional to the zero level conditions.

A.11.3.2. Range of Adjustments of E_3.

The range of adjustments of E_3 necessary to correct for the net drift of the zero level in the quantizer can be derived from the second part of Equation (A.32) as given by Equation (A.34).

$$\Delta E_3 = \pm R_3\left[\frac{X_3E_3}{R_3} + \frac{X_{10}E_{10}}{R_1} - \frac{X'_{10}E'_{10}}{R'_1} + \frac{X_{20}E_{20}}{R_2} - \frac{X'_{20}E'_{20}}{R'_2} - \frac{E_{rd}}{R_r} + \frac{E'_{rd}}{R'_r} + \frac{E_d}{GR_{in}}\right] \quad .. \text{(A.34)}$$

The design of the "set zero" circuit (see Figure 53) was based on results obtained from Equations (A.33) and (A.34). If R_z in front of Equation (A.34) is replaced by R_{in}, the equation represents the voltage drift of the zero level in the quantizer as referred to the input.

A.11.4. Summary of Prevailing Conditions for the Remaining Part of the Analysis.

The remaining part of this appendix is concerned with the analysis of the dynamic behaviour of the system in the presence of an input signal. Equation (A.31) is still used but the following general conditions prevail.

1. The input signal is equal to an exact number of quantization intervals.
2. The first part of Equation (A.31), dealing with the zero conditions and with the drift terms E_d, E_{rd} and E'_{rd}, have been reduced to zero by adequate adjustment of E_z.
3. The two series of notes of section A.11.2. still apply.

A.11.5. The Decoder Unit.

The nominal values for the weighing resistors of the decoder unit (see Figure 74) can be derived from Equation (A.31). Two additional conditions must be added

to those listed in section A.11.4.: all error and drift terms are nil (all X = 0) and the noise voltage is ignored ($E_n = 0$). In this case, Equation (A.31) reduces to Equation (A.35).

$$e_o = Ge_{in} + GR_{in}\left[\frac{n_1E_1}{R_1} - \frac{n_1'E_1'}{R_1'} + \frac{n_2E_2}{R_2} - \frac{n_2'E_2'}{R_2'}\right] \quad .. (A.35)$$

A.11.5.1. Computation of R_1.

Suppose that the input signal is negative and equal to one quantization interval, q, and that all of the chains are at the zero level except the first positive decade such that $n_1 = 1$ and $n_1' = n_2 = n_2' = 0$ in Equation (A.35).

$$e_o = -Ge_{in} + GR_{in}\left[\frac{E_1}{R_1}\right] \quad .. (A.36)$$

The magnitude of R_1 necessary to reduce e_o to zero in Equation (A.36) is given by Equation (A.38).

$$R_1 = R_{in}\left[\frac{E_1}{q}\right] \quad .. (A.38)$$

The quantization interval is determined by the ratio E_L/G (see Figure 74). Any error in the gain, G, due to R_{in}, can be compensated by adjusting E_L. Equations similar to Equation (A.38) can be derived for all other resistors in the decoder. However, only one resistance value must be computed in that way as the others are

calculated from the weighing factors listed in Table VII of Appendix A.8.

A.11.6. Precision in Tunnel Diode Chains (No Cycling Operation).

For the quantizer to operate normally until the cycling process is initiated in the stepping reference unit, certain precision requirements must be met by the tunnel diode chains. The conditions listed in section A.11.4. are still applied to Equation (A.31). Every time a factor, n, in the resulting expression increases by one unit, the correction in e_o must equal $|E_L|$ with an error always less than that value. If this last condition were not fulfilled, the error would exceed one quantization interval and the amplifier would overload temporarily; more than one pulse would be generated by the level detector in correcting for that error.

A.11.6.1. First Decades.

An expression for the error introduced in the quantizer by any new step being generated in the first positive decade can be derived from Equation (A.31) if e_{in} is decreased by one quantization interval and n_1 is stepped up by one unit, all other terms remaining unchanged. Subtraction of the two resulting e_o gives the error voltage, $e_{o\epsilon}$, which should ideally be zero.

$$e_{o\varepsilon} = GR_{in}\left[\frac{X_1 E_1}{R_1}\right] + 2E_n \qquad .. (A.39)$$

By definition.

$$e_L = E_L \pm E_{dL} = G.(q) \pm E_{dL} \qquad .. (A.40)$$

Making $e_{o\varepsilon}$ smaller than e_L and combining with Equation (A.38) give the upper limit for X_1.

$$\bar{X}_1 = 1 - (X_L + 2X_n) \qquad .. (A.41)$$

where by definition:

$$X_L = \frac{E_{dL}}{G.q} \quad \text{and} \quad X_n = \frac{E_n}{G.q} \qquad .. (A.42)$$

Equation (A.41) gives the maximum relative difference that can be tolerated between two successive voltage steps in the first positive chain in order to avoid overloading of the amplifier under normal operating conditions. An identical expression could also be derived for the corresponding negative decade. It is interesting to note that the total deviations of the chains from the ideal staircase waveform do not interfere with the normal operation of the quantizer until the cycling process is initiated. However, these causes of error influence the instantaneous accuracy of the analogue-to-digital conversion.

A.11.6.2. Second Decades.

The same procedure can be used to derive an expression for the upper limit of X_2.

$$\overline{X}_2 = 0.1 - \frac{1}{10}(X_L + 2X_n) \qquad .. (A.43)$$

As long as Equations (A.41) and (A.43) are satisfied, the positive side of the staircase generator can operate from zero to its maximum output without producing an overload of the summing amplifier. It is assumed that the net deviation in the first decade is zero when the 9th level is reached such that the tenth diode is triggered when the input signal is equivalent to exactly ten quantization intervals. This situation is real as the resistance, R_1, is adjusted according to the average step, E_1 (see Appendix A.7). Similar conclusions hold for the negative side of the stepping reference.

A.11.7. Precision Required in the Voltage References during the Cycling Process.

Additional precision requirements are imposed on the staircase generator during the cycling process and the deviations of e_1, e_2, e_1' and e_2' from exact multiples of "q" as well as the errors in E_r and E_r' must remain below certain limits in order to prevent overloading of the

summing amplifier. In the following analysis, the process has been divided in three parts depending on the state of the Reset Reference Unit:

1. Reset Reference Unit switched on.
2. Both chains being stepped simultaneously.
3. Reset Reference Unit switched off.

A.11.7.1. Reset Reference Unit Switched On.

The present situation arises when the positive staircase has reached its 99th level and when the input signal decreases sufficiently to bring the output voltage of the summing amplifier to an amplitude equal to $(E_L \pm E_n)$. At that precise moment, the resetting of the positive side of the staircase generator to zero and the introduction of the voltage step, E_r, reduces the output by an amount $|E_L \pm \text{error}|$. As stated before, the resulting voltage error must not exceed $|E_L|$. The negative chains may contain any number of steps between zero and ninety-nine. An expression for the output voltage of the amplifier, just before the positive chains start resetting, can be obtained from Equation (A.31) under the conditions listed in section A.11.4.

$$e_{oa} = -E_L + E_n = -GE_{in} + GR_{in}\left[\frac{9E_1}{R_1} + \frac{9E_2}{R_2} - \frac{n_1'E_1'}{R_1'} - \frac{n_2'E_2'}{R_2'}\right]$$

$$+ GR_{in}\left[\frac{n_1E_1X_1}{R_1} + \frac{n_2E_2X_2}{R_2} - \frac{n_1'E_1'X_1'}{R_1'} - \frac{n_2'E_2'X_2'}{R_2'}\right] + E_n \quad .. (A.44)$$

After the positive chains have returned to zero and the positive voltage step, E_r, has been switched on but before the beginning of the 10Mc/s stepping operation, the output from the summing amplifier is given by Equation (A.45). It is assumed that the input signal, E_{in}, has not changed appreciably.

$$e_{ob} = -GE_{in} + GR_{in}\left[-\frac{n_1'E_1'}{R_1'} - \frac{n_2'E_2'}{R_2'} + \frac{E_r}{R_r}\right]$$

$$+GR_{in}\left[-\frac{n_1'E_1'X_1'}{R_1'} - \frac{n_2'E_2'X_2'}{R_2'} + \frac{E_rX_r}{R_r}\right] + E_n \quad .. (A.45)$$

By definition,

$$R_{in}\left[\frac{E_r}{R_r}\right] = 100q = R_{in}\left[\frac{9E_1}{R_1} + \frac{9E_2}{R_2}\right] + q \quad .. (A.46)$$

Equation (A.45) can be simplified if the difference, $e_{ob} - e_{oa} = E_L \pm 2E_n$, is carried out using Equation (A.44) and if Equation (A.46) is introduced in the new expression. If then, $e_{oa} = E_L$ is subtracted from the result, Equation (A.47) for e_{ob} is obtained.

$$e_{ob} = GR_{in}\left[\frac{E_r X_r}{R_r}\right] - GR_{in}\left[\frac{n_1 E_1 X_{1d}}{R_1} + \frac{n_2 E_2 X_{2d}}{R_2}\right] \pm 2E_n \qquad .. (A.47)$$

The factors X_{1d} and X_{2d} represent the magnitudes of X_1 and X_2 when the positive chains are at the 9th levels. Corresponding values of n_1 and n_2 equal to nine must be used. As a close approximation, X_{1d} and X_{2d} can be replaced by the relative thermal coefficients of the average steps, E_1 and E_2.

Ideally, the error voltage, e_{ob}, should equal zero but, in practice, it must never exceed $\pm E_L$. Making $e_{ob} < |E_L|$ in Equation (A.47), extracting X_r and using Equation (A.46) and Equation (A.42) to simplify the results, yields Equation (A.48) for the upper limit of X_r.

$$\overline{X}_r = .01 - .02X_n - (.09X_{1d} + 0.9X_{2d}) \qquad .. (A.48)$$

As long as Equation (A.48) is satisfied, the resetting of the positive chains in the staircase generator and the introduction of E_r at the beginning of the cycling process does not overload the summing amplifier. It can be seen from Equation (A.48) that a precision much better than 1% may be needed for the voltage step, E_r, in the Reset Reference Unit. Some compensation effect can be used advantageously if E_r shows a temperature coefficient equal to that of the positive chains such that X_r contains

a term equal to $(.09X_{1d} + 0.9X_{2d})$. Similar results can be obtained for the negative half of the voltage references.

A.11.7.2. Both Chains Being Stepped Simultaneously.

The most stringent precision requirements are imposed on the voltage references in the quantizer during that part of the cycling process when the 10Mc/s pulse generator is stepping up both sides simultaneously. In this case, the linearity of the chains together with the precision of the Reset Reference Unit must be taken into account.

The output voltage from the summing amplifier prior to the switching on of the 10Mc/s pulse generator was given earlier by Equation (A.45). As soon as the second decades start stepping up, Equation (A.49) can be used to describe the new voltage, e_{oc}.

$$e_{oc} = -GE_{in} + GR_{in}\left[\frac{n_2E_2}{R_2} - \frac{n_1'E_1'}{R_1'} - \frac{n_2'E_2'}{R_2'} + \frac{E_r}{R_r}\right]$$

$$+GR_{in}\left[\frac{n_2E_2X_2}{R_2} - \frac{n_1'E_1'X_1'}{R_1'} - \frac{n_2'E_2'X_2'}{R_2'} + \frac{E_rX_r}{R_r}\right] + E_n \quad .. \text{(A.49)}$$

In Equation (A.49) the factor n_1' remains constant while n_2 and n_2' are increasing simultaneously (n_2 increases from zero and n_2' starts from whatever initial value it had at the beginning of the cycling process).

Provided that the input signal does not change appreciably during the cycling process, the voltage e_{oc}, of which e_{ob} is a special case for $n_2 = 0$, is due to inaccuracies introduced by the various units of the quantizer. The initial voltage, e_{ob}, was itself different from zero as expressed by Equation (A.47). Increments of e_{oc} from e_{ob}, for values of n_2 between 1 and $(10 - n_2')$, are given by Equation (A.50) obtained from Equations (A.45) and (A.49).

$$e_{oc} - e_{ob} = GR_{in}\left[\frac{n_2E_2X_2}{R_2} - \frac{n_2E_2'X_2'}{R_2'}\right] + 2E_n \qquad .. (A.50)$$

It should be noted that, in deriving Equation (A.50), the initial value of n_2' has been cancelled out in the subtraction and only its increment equal to n_2 has remained.

If the summation of the voltages given by Equations (A.47) and (A.50) is always smaller than $\pm E_L$, the amplifier does not overload at any time during the operation of the 10Mc/s pulse generator. A general expression based on the above statement was derived describing the most stringent precision requirements to be imposed on the voltage references in the quantizer. The result is given in Equation (A.51); it was obtained directly from the addition of Equations (A.47) to (A.50) and finally simplified with Equations (A.38) and (A.42).

$$100X_r + 10(n_2X_2 - n_2X_2') - 9(X_{1d} + 10X_{2d}) < 1 + 2X_n \quad .. \quad (A.51)$$

Notes on Equation (A.51).

1. For $n_2 = 0$, Equation (A.51) is reduced to Equation (A.48). Equation (A.51) is more general as it includes an additional term taking into account the total deviations in the chains. The influence of these deviations on the choice of the factor n_2 has been discussed in Appendix A.12.
2. Some parts of X_2 and X_2' are due to thermal effects and can be subtracted from one another (see section 3.3. and Appendix A.8).
3. Those components of X_2 and X_2' due to the tolerances on the steps in the chains and on R_2 and R_2' must be added together in agreement with the worst-case approach.

A.11.7.3. Reset Reference Unit Switched Off.

The precision needed in the quantizer when the reset reference voltage, E_r, is removed at the end of the cycling process, can be analysed in a manner illustrated in sections A.11.7.1. and A.11.7.2. The rather complex derivations are not reproduced here as the resulting expression is a special case of Equation (A.51) and would contribute no additional information to the analysis of the quantizer which has been summarized in this appendix.

APPENDIX A.12.

COMPUTATION OF THE PRECISION REQUIREMENTS IN THE QUANTIZER.

In this appendix, the relevant characteristics of all circuits in the quantizer are introduced in the theoretical equations derived in Appendix A.11. In this way, equations are obtained describing the maximum relative deviation factors, X_1 and X_2, as functions of the temperature range. An analytical expression is derived for the reset reference voltage step, E_r, from which the relative drift factor, X_r, is obtained. All circuits described in Chapter 4 are then investigated in turns for their contribution to the over-all error in the quantizer; the results are used to express X_r as a function of the temperature range. This value of X_r is replaced in Equation (A.51) of Appendix A.11. to find the upper limit of the tolerances, x_{2a} and x'_{2a}, on the steps in the chains as a function of the temperature range. A table of values is calculated from the resulting expression, permitting the choice of the maximum acceptable tolerances in the second decades, for three different temperature ranges and for various chain linearities.

A.12.1. List of Symbols Used in Appendix A.12.

The following list of symbols contains only the

terms used in Appendix A.12. which were not included in the definitions at the beginning of Appendix A.11.

x_{1a} = maximum relative deviation of any step in the first positive decade at the chosen standard temperature.

x_{1b} = part of X_1 due to the temperature coefficient of the average step, E_1, of the first positive decade.

x_{1c} = part of X_1 due to the inaccuracy introduced in E_1 by the weighing resistor, R_1.

x_{2a} = maximum relative deviation of any step in the second positive decade at the chosen standard temperature.

i_T = instantaneous value of the current flowing at the output of the current source on the positive side of the Reset Reference Unit (see Figures 54 and 75).

i_b = instantaneous value of the current flowing in the base of the transistor in the overload detection unit (see Figure 75).

i_c = instantaneous value of the current flowing into the resistor, R_c, in the Reset Reference Unit and defining e_r (see Figure 75).

x_c = maximum relative variation of i_c due to the thermal coefficient of the resistor, R_c.

i_{co} = instantaneous value of the collector current in the switching transistor on the positive side of the Reset Reference Unit when the base and the emitter are connected together and V_{ce} is equal to E_{ro} (see Figure 75).

i_r = instantaneous value of the current produced into the resistor, R_r, by the voltage, e_r.

I_T, I_b, I_c, I_{co}, I_r = nominal value of the current, i_T, i_b, i_c, i_{co}, i_r, respectively, measured at the chosen standard temperature.

x_T, x_b, X_c, x_{co}, x_i = maximum value of the relative variation of the current i_T, i_b, i_c, i_{co}, i_r, respectively, for a given temperature range.

x_{ce} = maximum relative thermal drift of the saturation voltage, $V_{ce(sat)}$, of the switching transistor on the positive side of the Reset Reference Unit.

k = temperature coefficient of the current, i_T.

x_d = temperature coefficient of the average step in the chains.

X_{ra} = part of X_r caused by the inaccuracy in the adjustment of R_r.

A.12.2. Sources of Error in the Chains.

The factor, X_1, described in Appendix A.11, may be expressed as the summation of three terms representing the main sources of error in the first positive decade.

$$X_1 = x_{1a} + x_{1b} + x_{1c} \qquad .. (A.52)$$

These fractional error terms have been defined at the beginning of the present appendix and are related respectively to the precision of the steps, the thermal coefficient of the chain and the influence of the resistor, R_1, on the accuracy of E_1.

The first term, x_{1a}, is smaller than ±2.2% as given in Appendix A.7. for the chain No. 7B. From Appendix A.8. and section 3.3.it is seen that x_{1b} is equal to $(-.0023/^oC).\Delta T$. The last term, x_{1c}, is made up of two parts: the tolerance on the resistor, R_1, and its temperature coefficient. The weighing resistor, R_1, was

adjusted to better than ±0.1% of its nominal value. The maximum temperature coefficient specified for the metal oxide resistors employed in the decoder was ±0.025%/°C. Replacing these figures in Equation (A.52) yields Equation (A.53) for X_1 as a function of the temperature range, ΔT.

$$X_1 = x_{1a} - .0023(\Delta T) + (\pm.001 \pm .00025\,\Delta T) \quad .. (A.53)$$

Identical expressions could be derived in the same way for X_1', X_2 and X_2'.

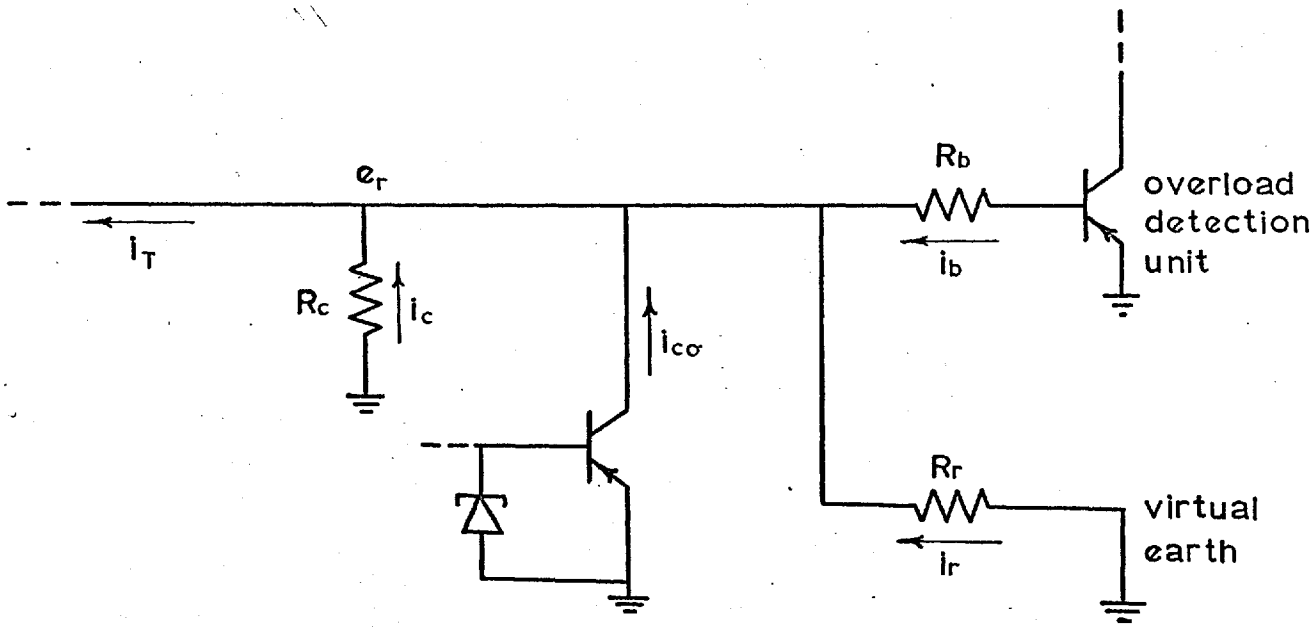
$$X_2 = x_{2a} - .0023(\Delta T) + (\pm.001 \pm .00025\,\Delta T) \quad .. (A.54)$$

A.12.3. Sources of Error in the Reset Reference Unit.

In order to analyse the different sources of error affecting the voltage step, E_r, of the Reset Reference Unit, part of Figure 54 has been reproduced in Figure 75. This figure shows the source current, i_T, divided between the precision resistor, R_c, defining e_r, the attached switching transistor, the decoder resistor, R_r, and the base resistor, R_b, of the overload detection unit.

A.12.3.1. Analytical Expressions for Reset Reference Voltages.

The following equations can be written directly from Figure 75, using the symbols defined in section A.12.1. of this appendix.



BASIC CIRCUIT DIAGRAM FOR RESET REFERENCE UNIT

Fig. 75.

$$e_r = I_c(1 + X_c)\, R_c(1 + x_c) \qquad .. (A.55)$$

which can be approximated by

$$e_r \cong R_c I_c + R_c I_c X_c + R_c I_c x_c \qquad .. (A.56)$$

The factor X_c takes into account the variations of e_r due to changes in I_c, assuming the resistance, R_c, to be constant. Similarly, x_c deals with the effect on e_r of a thermal drift of R_c, for a constant value of I_c. This assumption and the simplification of Equation (A.56) are valid as long as x_c is very small. The voltage e_r is measured in place for the calculation of R_r and the tolerance on R_c does not enter into x_c which depends only on the temperature coefficient of a metal oxide resistor. Following this argument, the node equation for the circuit of Figure 75 can be used to derive an expression for the term $I_c(1 + X_c)$.

$$I_c(1 + X_c) = i_T - (i_b + i_{co} + i_r) \qquad .. (A.57)$$

If the currents in Equation (A.57) are expressed as functions of the circuit parameters shown in Figure 75, Equation (A.58) is obtained after separation of the nominal values from the error terms.

$$I_c(1 + X_c) = I_T - \left[\frac{(E_{ro} - V_{be})}{R_b} + I_{co} + \frac{E_{ro}}{R_r}\right] + I_T(x_T)$$

$$- \left[\frac{(E_{ro} - V_{be})}{R_b}(x_b) + I_{co}(x_{co}) + \frac{E_{ro}}{R_r}(x_i)\right] \quad .. (A.58)$$

The first two terms in Equation (A.58) equal I_c and the last two represent the variation I_cX_c. Replacing Equation (A.58) into (A.56) gives Equation (A.59) as the general expression for the voltage, e_r.

$$e_r = E_{ro} + R_cI_T(x_T) - R_c\left[\frac{(E_{ro} - V_{be})}{R_b}(x_b) + I_{co}(x_{co}) + \frac{E_{ro}}{R_r}(x_i)\right] + E_{ro}(x_c) \quad .. (A.59)$$

where $E_{ro} = R_cI_c$ is given by Equation (A.60).

$$E_{ro} = \frac{I_T - I_{co} + V_{be}/R_b}{\frac{1}{R_c} + \frac{1}{R_b} + \frac{1}{R_r}} \quad .. (A.60)$$

The step generated by the positive side of the Reset Reference Unit when the switching transistor saturates, is given by Equation (A.61).

$$E_r(1 + X_r) = e_r - V_{ce}(sat)\left[1 + x_{ce}\right] \quad .. (A.61)$$

Replacing Equation (A.59) into Equation (A.61) and separating the error terms from the nominal values give Equation (A.62) and Equation (A.63) for E_r and X_r respectively.

$$E_r = R_c I_T - R_c\left[\frac{(E_{ro} - V_{be})}{R_b} + I_{co} + \frac{E_{ro}}{R_r}\right] - V_{ce(sat)} \quad .. (A.62)$$

$$X_r = \frac{R_c I_T(x_T)}{E_r} - \frac{R_c}{E_r}\left[\frac{E_{ro}(x_b + x_i)}{R_b} - \frac{V_{be}(x_b)}{R_b} + I_{co}(x_{co})\right]$$

$$+ \frac{E_{ro}x_c}{E_r} - \frac{V_{ce(sat)}}{E_r}\left[x_{ce}\right] \quad .. (A.63)$$

The term $E_{ro}(x_i)/R_r$ has been replaced in Equation (A.63) by $E_{ro}(x_i)/R_b$. The error introduced in the equation by this simplification is negligible.

A.12.3.2. Calculation of E_r and i_T.

The voltage steps, E_r, and E'_r were chosen equal to +5 volts and -5 volts respectively in order to use identical values for the weighing resistors, R_r and R'_r and to operate the switching transistors in the Reset Reference Unit at a safe collector-to-emitter voltage. Noting that E_r, for instance, is the difference between E_{ro} and the saturation voltage of the corresponding transistor, the necessary magnitude of E_{ro} can be obtained. The voltage E'_{ro} can also be derived in a similar way. At 23°C, the saturation voltages for the ASZ21 and the 2N797 transistors are respectively -0.262 volt and +.095 volt when driven by a tunnel diode as illustrated in Figure 54. It was therefore necessary to adjust E_{ro} to -5.262 volts and E'_{ro}

to +5.095 volts. From Equation (A.60) and its negative equivalent, I_T = 8.00ma and I'_T = 7.56ma can be obtained using the above results with the following parameters: I_{co} = 2 μA, I'_{co} = 1 μA, $V_{be} = V'_{be}$ = 0.38 volt, R_b = 22Kohms, R'_b = 224Kohms, $R_c = R'_c$ = 680ohms, $R_r = R'_r$ = 120kohms (approx.).

It should be remembered that these figures represent design values and that I_T and I'_T were finally adjusted in place.

A.12.3.3. Investigation of the Various Error Terms.

Expressions will now be derived for the factors x_T, x_b, x_i , x_{co}, x_c and x_{ce}, contained in Equation (A.63), from the characteristics of the circuits described in Chapter 4. All of these factors have been defined in section A.12.1. of this appendix.

(1) $x_T = \Delta I_T / I_T$

The current, i_T, in the Reset Reference Unit is defined by a circuit of the type described in Appendix A.5. where it can be seen that the two major causes of variations in i_T are the temperature fluctuations and the sensitivity of the source to changes in the supply voltage.

The first item will be taken into account at this stage by assigning a symbol, k, to the temperature coefficient, $\Delta I_T/I_T . \Delta T$, of the current source. In order to show that the second item could be neglected, measurements were carried out in the laboratory on the +25v. and the -25v. regulated supplies. The maximum drift recorded has never exceeded $\pm$40mv per day after a five minute warm-up period. The resulting change in i_T is less than $\pm.007\%$ per day as computed from Equation (A.12) and Equation (A.13) of Appendix A.5. An expression for x_T can therefore be written as in Equation (A.64).

$$x_T = k . \Delta T \qquad .. (A.64)$$

(2) x_b - from $i_b = I_b(1 + x_b)$

The current, i_b, can be affected only by the temperature changes in V_{be}, e_r and R_1. Directly from Figure 75, i_b, can be expressed as follows,

$$i_b = (e_r - V_{be})/R_1 \qquad .. (A.65)$$

which, after differentiation with respect to temperature, gives Equation (A.66).

$$\frac{\Delta i_b}{\Delta T . i_b} = \frac{\left[\frac{\Delta e_r}{\Delta T} - \frac{\Delta V_{be}}{\Delta T}\right]}{e_r - V_{be}} - \frac{\Delta R_1}{\Delta T} . \frac{1}{R_1} \qquad .. (A.66)$$

Approximating $\Delta e_r/\Delta T$ by kE_{ro}, making $e_r = 5.26v$, $V_{be} = .38v.$ and $E_{ro} = 5.262\ v.$ and replacing $\Delta V_{be}/\Delta T$ by $-2.5mv/^oC$ into Equation (A.66), give the following expression for x_b.

$$x_b = (1.1k + .00053 \pm .00025).\ \Delta T \qquad .. (A.67)$$

(3) x_i - from $i_r = I_r(1 + x_i)$

In this case, the procedure is very similar to that used above for x_b. Only temperature effects on R_r and e_r are worth considering. From Figure 75, $i_r = e_r/R_r$, which after differentiation with respect to temperature gives Equation (A.68).

$$\frac{\Delta i_r}{\Delta T.i_r} = \frac{\Delta e_r}{\Delta T.e_r} - \frac{\Delta R_r}{\Delta T}.\frac{1}{R_r} \qquad .. (A.68)$$

The first term in Equation (A.68) can be approximated by the temperature coefficient, k, of i_T and the second one is the thermal coefficient already quoted for the metal oxide resistors used. In this way, Equation (A.69) is obtained from Equation (A.68).

$$x_i = (k \pm .00025).\ \Delta T \qquad .. (A.69)$$

(4) x_{co} - from $i_{co} = I_{co}(1 + x_{co})$

The following currents were measured at the collectors of ASZ21 and 2N797 transistors for a collector-

to-emitter voltage equal to 5 volts and with a short circuit between the base and the emitter.

I_{co} = 1 to 2 μA for ASZ21

I'_{co} = 0.4 to 1 μA for 2N797

For the present application, these leakage currents can be assumed to double for every 10°C rise in temperature and Equation (A.70) can be written directly for x_{co}.

$$x_{co} = + 0.1(\Delta T) \quad .. (A.70)$$

(5) x_{ce} - takes into account the temperature effect on $V_{ce}(sat)$.

The temperature coefficients of the saturation voltages of ASZ21 and 2N797 transistors, driven by a tunnel diode, were measured in the laboratory. For both types of transistors, a thermal coefficient of the order of -0.04%/°C was obtained, leading to Equation (A.71) for x_{ce}.

$$x_{ce} = -.0004(\Delta T) \quad .. (A.71)$$

(6) x_c - as explained in section A.12.3.1, x_c is reduced to the effect of the temperature coefficient of the metal oxide resistor used for R_c.

$$x_c = \pm.00025(\Delta T) \quad .. (A.72)$$

A.12.3.4. Expression for X_r as a Function of the Termperature Range.

An expression for the maximum relative drift, X_r, of the reset reference voltage step, can be obtained as a function of the temperature range if the above equations for x_T, x_b, x_i, x_c, x_{co} and x_{ce} are introduced into Equation (A.63) together with $E_r = 5.0$ volts, $E_{ro} = 5.262$ volts, $V_{ce}(sat) = .262$ volt, $V_{be} = 0.38$ volt, $R_c = 680$ohms, $R_b = 22$Kohms, $I_{co} = 2\,\mu A$, $I_T = 8.00$ma.

$$X_r = (1.023k + 0.226x10^{-3}).\,\Delta T + X_{ra} \qquad .. (A.73)$$

Similarly, a corresponding expression can be derived for X'_r, if $E'_r = 5.0$ volts, $E'_{ro} = 5.095$ volts, $V'_{ce}(sat) = 0.095$ volt, $V'_{be} = 0.38$ volt, $R'_c = 680$ohms, $R'_b = 224$Kohms, $I'_{co} = 1\,\mu A$ and $I'_T = 7.56$ma.

$$X'_r = (1.022k' + 0.245x10^{-3}).\,\Delta T + X'_{ra} \qquad .. (A.74)$$

The extra terms, X_{ra} and X'_{ra}, were added to the above equations in order to take into account the inaccuracy in the adjustment of R_r and R'_r. It was more convenient to ignore these error terms until this point to deal exclusively with the temperature effects on X_r and X'_r.

A.12.4. Precision Requirements for the Chains.

The minimum accuracy requirements for the

chains in the staircase generator have been expressed in Appendix A.11. by Equation (A.41) and Equation (A.43). These equations are valid as long as the cycling process is not initiated. From Equation (A.42), the factors $X_L = .000513(\Delta T)$ and $X_n = \pm.0282$ can be obtained, using data available from Chapter 4 on the level detector and the summing amplifier units. The maximum tolerances, x_{1a} and x_{2a}, on the steps in the first and second decades can be computed by replacing Equation (A.53) and Equation (A.54) in Equation (A.41) and Equation (A.43) respectively. The results for a $\pm 5^{o}C$ temperature range are: $x_{1a} = x'_{1a} = \pm 92.8\%$ and $x_{2a} = x'_{2a} = \pm 8.1\%$.

Much more stringent precision requirements must be met by the chains when the cycling process is taken into account as will now be seen.

A.12.4.1. Precision Requirements During the Cycling Process.

Equation (A.51), derived in Appendix A.11, can be used to establish the linearity and precision requirements for the second decades in the staircase generator.

The factor X_r, from Equation (A.73), is replaced into Equation (A.51) and the temperature dependent parts in X_r are adjusted (see section A.12.4.2.) to cancel out the

term $9(X_{1d} + 10X_{2d})$. Equation (A.54) and its negative equivalent, for X_2 and X_2' respectively, are then introduced in the resulting expression, leading to Equation (A.75) for the maximum tolerances, x_{2a} and x_{2a}', (i.e. to ensure that no overload of the summing amplifier occurs during the cycling process independently of the gating system) in the last two tunnel diode chains as a function of the temperature range.

$$x_{2a} + x_{2a}' = \frac{1}{n_2}\left[0.1 - 0.2X_n - 10.X_{ra}\right] - .002 - .0005(\Delta T) \quad .. \text{(A.75)}$$

The last term in the above equation could be ignored if the temperature coefficients of R_2 and R_2' were matched.

The tolerance required in a chain can be found directly from Table IX as a function of the maximum deviation and of the temperature range. These results were computed from Equation (A.75), with the following additional assumptions:

(a) The maximum tolerances on the steps in both chains are equal, $x_{2a} = x_{2a}'$.

(b) The deviation of each step from the average in the chains is equal to plus or minus the upper limit of the tolerance, i.e. x_{2a}.

(c) The maximum total deviation in each chain is given

by the number of times, n_2, that the tolerance, x_{2a}, can be repeated with the same polarity in successive steps.

(d) The weighing resistors, R_2 and R_2', were adjusted to $\pm 0.1\%$ while R_r and R_r' were adjusted to $\pm .01\%$.

ΔT \ n_2	5	3	1
$\pm$ 5°C	$\pm$ 0.71%	1.33%	4.4%
$\pm$ 1°C	0.81%	1.43%	4.5%
0°C	0.83%	1.45%	4.6%

TABLE IX

Maximum Permitted Tolerance, x_{2a}, on the Chains as a Function of the Deviation and the Temperature Range.

A.12.4.2. Temperature Coefficient of the Reset Reference Unit.

In the derivation of Equation (A.75), it was assumed that the temperature coefficient of the Reset Reference Unit was adjusted to match the deviation, due to thermal drift, appearing at the output of the staircase generator at the beginning of the cycling process. The term $9(X_{1d} + 10X_{2d})$ in Equation (A.51) is a function of

the temperature coefficient, x_d, of the average step in the chains and is approximately equal to $99.x_d$. The coefficients $x_d = -0.21\%/^oC$ and $x'_d = -0.23\%/^oC$, for the positive and the negative chains respectively, can be deduced from the experimental results given in Appendix A.8. From the first part of Equation (A.73) and from its negative equivalent, the thermal coefficients, $k = -0.23\%/^oC$ and $k' = -0.25\%/^oC$, for the current sources in the Reset Reference Unit, can be calculated with the above values for x_d and x'_d. The voltage drift (normalized to a 465mv step) of the complete positive staircase waveform resting at the 99th level adds up to $-96mv/^oC$ (Table VII, Appendix A.8.). Multiplying this figure by the corresponding weighing factor $R_r/R_2 = E_r/10.E_2$ and adding the thermal drift of the saturation voltage, $V_{ce}(sat)$, obtained from Equation (A.71), the necessary thermal drift in e_r is found to equal $-10.5mv/^oC$. Similarly, the negative chains have a thermal drift of $-108mv/^oC$ at full scale and the coefficient $\Delta e'_r/\Delta T$ must be adjusted to $-11.6mv/^oC$. An average value of $-11mv/^oC$ must be chosen in order to operate both sides of the Reset Reference Unit with identical temperature coefficients.

It is interesting to note that with this technique, the temperature range, ΔT, in Table IX, has only a very small influence on the maximum tolerance,

x_{2a}, acceptable in the chains. Without this matching of thermal coefficients between the Reset Reference Unit and the staircase generator, it would be impossible to satisfy Equation (A.51) for $\Delta T = \pm 5^{o}C$, regardless of the tolerance on the steps.

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