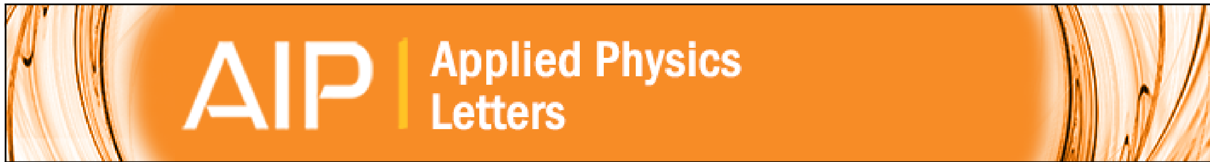

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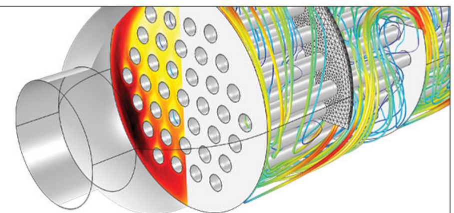

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A memory cell with single-electron and metal-oxide-semiconductor transistor integration

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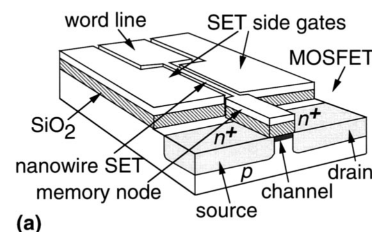
A single-electron transistor memory cell with metal-oxide-semiconductor field-effect transistor sensing has been fabricated in silicon-on-insulator material. The single-electron transistor, coupled to a memory node, is defined in the upper silicon layer. The memory node forms the gate of a metal-oxide-semiconductor field-effect transistor with its channel in the substrate silicon. At 4.2 K, there are two different states of the memory-node voltage, separated by the single-electron transistor Coulomb gap. These states are sensed at high-current output levels by the metal-oxide-semiconductor transistor. The metal-oxide-semiconductor transistor current also shows evidence of gate-dependent conductance oscillations in the coupled single-electron transistor. © *1999 American Institute of Physics.* [S0003-6951(99)03009-0]

In recent years, there has been considerable interest in single-electron devices using the Coulomb blockade effect for future large-scale integrated circuit applications. A single-electron memory cell can offer the advantages of small size, low power, and the precise control of a small number of electrons. For flexibility of integration with present-day systems, a single-electron memory cell compatible with complementary metal-oxide-semiconductor (CMOS) technology is required. Several designs of single-electron memory cells in silicon have been demonstrated,[1–3] where single-electron charging in a single island or a distribution of nanocrystalline islands is sensed as a shift in the threshold voltage of a transistor. Stone and Ahmed[4] have demonstrated an alternative configuration, where a single-electron transistor (SET) consisting of a multiple tunnel junction in silicon-on-insulator (SOI) material precisely controls a small number of stored electrons on a memory node. The charge is then sensed in the current of a SET electrometer. However, a SET has low voltage gain (typically less than 1), and an amplification stage may also be necessary before integration with CMOS devices is possible.

In this letter, we discuss the design and operation of an integrated SET/metal-oxide-semiconductor field-effect transistor (MOSFET) memory cell, or lateral single electron memory (L-SEM),[5] where the SET is in the form of a multiple tunnel junction. The negligible conductance of the SET when it operates within the Coulomb gap is used to control the charge on a memory node, leading to two different states of the memory-node voltage separated from each other by the Coulomb gap. The memory node forms the MOSFET gate and the memory states are sensed in the MOSFET current. Because of the SET/MOSFET integration in this memory design, our device is a gain cell with the advantage that it can be directly integrated with conventional CMOS circuitry.

The integrated SET/MOSFET memory cell is fabricated in SOI material, as shown in the schematic in Fig. 1(a). A nanowire SET[6] is defined in the upper silicon layer of the SOI material and connected to the memory node, which is also the gate of an n-channel MOSFET fabricated in the substrate silicon layer. In a common-source configuration, the SET and MOSFET are biased using word-line voltage V_{ws} and drain-source voltage V_{ds}, respectively. The SET



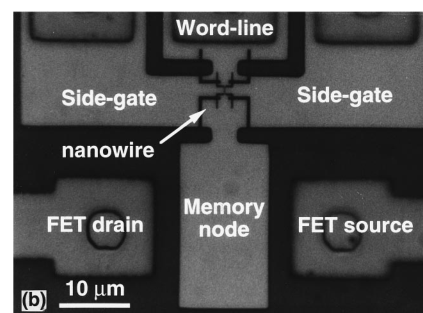


FIG. 1. (a) Schematic of an integrated SET/MOSFET memory cell fabricated in SOI material. A side-gated nanowire SET is coupled to a memory node and fabricated in the upper silicon layer. The memory node is also the gate of a MOSFET with the source, drain, and channel in the substrate silicon layer. (b) Optical micrograph of a complete memory cell. The SOI has a ~40-nm-thick upper silicon layer and ~40-nm-thick buried oxide. The metallization is supported on a 500-nm-thick sputtered silicon dioxide layer.

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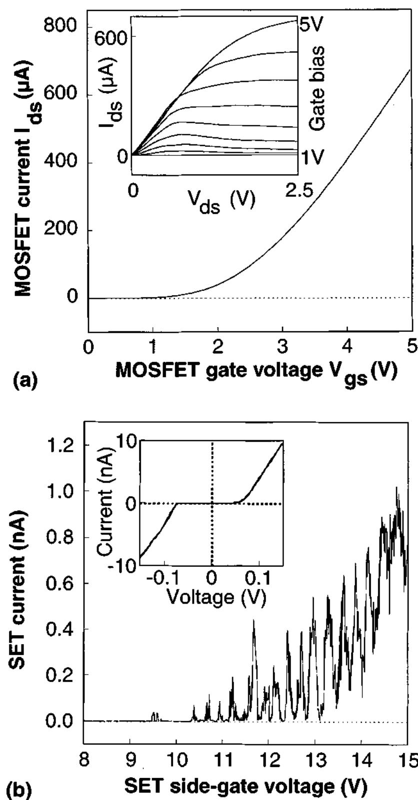

FIG. 2. (a) Drain-source current as a function of gate voltage in a MOSFET test device at 4.2 K. A constant drain-source voltage of 2 V is used. The inset shows the corresponding drain-source current–voltage characteristics. The gate voltage is increased in 0.5 V steps. (b) Single-electron conductance oscillations as a function of side-gate voltage in a SET test device at 4.2 K. The nanowire cross-section is approximately $20\,\text{nm}\times 20\,\text{nm}$ and the nanowire voltage is 10 mV. The inset shows the nanowire current–voltage characteristics at 9 V side-gate voltage. A Coulomb gap of 0.12 V can be seen.

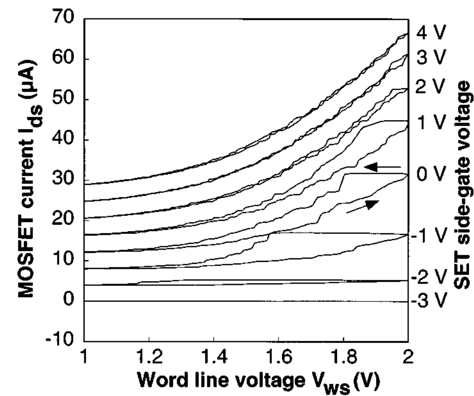

FIG. 3. Electrical characteristics of an integrated SET/MOSFET memory cell at 4.2 K. Hysteresis occurs in the MOSFET drain-source current when the word-line voltage is swept cyclically, corresponding to an offset in the memory-node voltage determined by the SET Coulomb gap. The hysteresis is modulated by the SET side-gate voltage. A constant MOSFET drain-source voltage of 1 V is used. The curves are offset by 4 μA for each SET side-gate voltage step for clarity.

Coulomb gap is varied by applying a voltage on the side gates, shown in Fig. 1(a). An optical micrograph of an L-SEM cell fabricated in SOI with a ~40-nm-thick upper silicon layer, ~40-nm-thick buried oxide, and a lightly doped *p*-type substrate is shown in Fig. 1(b). The upper silicon layer was heavily doped *n* type by arsenic implantation ($8\times 10^{13}\,\text{cm}^{-2}$ at 35 kV). The channel region was implanted *p* type with boron ($2\times 10^{12}\,\text{cm}^{-2}$ at 55 kV and $5\times 10^{12}\,\text{cm}^{-2}$ at 75 kV). The substrate source/drain contact regions, separated by 8 μm, were heavily doped *n* type by phosphorous implantation ($2\times 10^{15}\,\text{cm}^{-2}$ at 75 kV). A heavily doped *p*-type substrate contact was also defined using boron implantation ($1\times 10^{15}\,\text{cm}^{-2}$ at 50 kV). High-resolution electron-beam lithography using polymethylmethacrylate electron-beam resist, followed by etching in a $CF_4/SiCl_4$ reactive-ion plasma defined the SET (a 50-nm-wide and 1-μm-long side-gated nanowire) and the memory node. An oxide layer of ~20 nm thickness was thermally grown to thin and passivate the nanowire.

The drain-source current as a function of the gate voltage at 4.2 K in a MOSFET without a coupled SET is shown in Fig. 2(a). The inset shows the corresponding drain-source current–voltage characteristics. The peak transconductance is 14 mS/mm. Figure 2(b) shows single-electron conductance oscillations in the nanowire of a SET test device as a function of the side-gate voltage at 4.2 K. The inset shows the corresponding nanowire current–voltage characteristics at a fixed side-gate voltage, where there is a zero-current Coulomb gap of 0.12 V. If the side-gate voltage is reduced, the gap tends to increase until eventually the current pinches off. If the side-gate voltage is increased, the gap tends to decrease, and ultimately single-electron charging effects disappear completely. The process is accompanied by an oscillation in the width of the gap as a function of side-gate voltage. The single-electron charging effects result from the creation of a multiple tunnel junction system associated with nonuniformity in the dopant distribution and in the surface structure along the nanowire.[6] The quantitative characteristics of the multiple tunnel junction depend on the exact device structure and can be controlled by the side-gate electric field.

The electrical characteristics of an integrated SET/MOSFET memory cell at 4.2 K are shown in Fig. 3. A clear hysteresis is seen in the MOSFET drain-source current when the word-line voltage is swept cyclically, corresponding to a shift in the operating point of the MOSFET. The hysteresis is strongly modulated by the SET side-gate voltage. The characteristics are not strongly dependent on sweep rate and the hysteresis can be observed for sweep times in excess of one hour. We explain the hysteresis with reference to the schematic of Fig. 1(a) assuming for simplicity a fixed, symmetric Coulomb gap in the SET between $-V_c$ and $+V_c$. With the word-line voltage initially at zero, the voltage across the SET is within the Coulomb gap and the SET current is zero. As the word-line voltage increases such that the SET voltage exceeds V_c, charge is transferred onto the memory node in order to maintain the SET voltage at V_c. The increase in the memory-node voltage is detected as an increase in the MOSFET current. If the word-line voltage sweep is now reversed, the SET voltage immediately falls below V_c so that it is not possible for the memory node to discharge, and a constant MOSFET current is sensed. Finally, when the SET voltage falls to $-V_c$, the memory node begins to discharge and the MOSFET current falls. There are two different memory-node states corresponding to memory-node voltages separated by the total SET gap of $2V_c$, and this leads to a hysteresis in the MOSFET characteristics. Experimentally,

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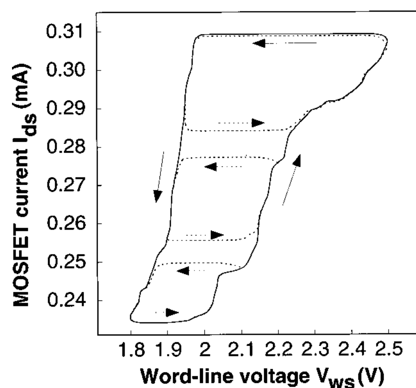

FIG. 4. Hysteresis in the MOSFET drain-source current of a memory cell at 4.2 K, when the word-line voltage is swept cyclically between 1.8 and 2.5 V (solid line). Voltage sweeps in three smaller ranges (dotted lines) are also shown. The MOSFET drain-source voltage is 4 V and the SET side-gate voltage is 0 V. The shape of the hysteresis is universal in the different sweeps. Clear current steps can also be seen in the characteristics.

the width of the hysteresis is not constant because the SET Coulomb gap is not invariant. This behavior is discussed in more detail later.

The hysteresis in Fig. 3 is influenced by the SET side-gate voltage. When the side-gate voltage is −3 V, conduction in the nanowire is pinched off, isolating the memory node from the word line, and the MOSFET current is nearly constant. At the other extreme of +4 V, nanowire conduction is enhanced to an extent that a Coulomb gap does not exist. The SET acts as a resistor in series with the memory node and the memory cell characteristics are not hysteretic. At all intermediate side-gate voltages, the Coulomb gap in the SET separates the memory-node voltage and a hysteresis is seen. With higher side-gate voltages, the Coulomb gap tends to become smaller and the hysteresis is reduced, as seen in Fig. 3. Figure 4 shows the hysteresis in a memory cell at 0 V SET side-gate voltage and 4 V drain-source voltage, as the word-line voltage is swept between 1.8 and 2.6 V. Four different sweeps over different voltage ranges demonstrate that the hysteresis is universal. The rounding of the hysteresis curve corners is caused by a nonabrupt transition between the conducting and Coulomb gap regions in the SET.

The memory cell described here incorporates a relatively large MOSFET and the two memory states correspond to a difference of around 10^6 electrons on the memory node. However, the memory node is easily scalable to much smaller sizes and can potentially operate with very few electrons. The low capacitance in such a scaled-down cell should give fast read and write cycles. Higher temperature operation up to 77 K or more may also be possible by optimizing the SET design.

An interesting feature in Figs. 3 and 4 is the observation of clear steps in the MOSFET current which we attribute to the effect of single-electron conductance oscillations in the SET. Although the applied SET side-gate voltage is fixed, increasing the word-line and memory-node voltage implies effective reduction in the side gate to nanowire voltage. The nanowire conductance therefore oscillates in a manner qualitatively similar to the characteristics in Fig. 2, accompanied by a modulation of the width of the Coulomb gap. If the Coulomb gap increases, the SET moves into the zero-current regime and the memory-node voltage remains constant until the new Coulomb gap is overcome at a higher word-line voltage. We observe this as a step in the MOSFET current. We also note that with increasing word-line voltage, the relative side-gate to nanowire voltage ultimately falls to an extent that the SET is pinched off and the MOSFET current saturates. This effect can be seen in the characteristics in Fig. 3 where the side-gate voltage is −2 V.

In conclusion, we have described the operation of a new memory cell, the L-SEM, at 4.2 K. A side-gated nanowire SET and a memory node are defined in the upper silicon layer of SOI material. The memory node forms the gate of a MOSFET with its channel defined in the substrate of the SOI material. There are two different states of the memory-node voltage, separated by the single-electron transistor Coulomb gap. The L-SEM is a gain cell which can be directly coupled to CMOS circuitry. Optimization of the SET should permit the operation of this cell at 77 K or higher temperatures.

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