Schottky-barrier lowering in silicon nanowire field-effect transistors prepared by metal-assisted chemical etching

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We investigate the influence of Schottky barrier lowering in Si nanowire field-effect transistors, using nanowires prepared by metal-assisted chemical etching. The experimental electrical characteristics of a $p$-channel transistor are modeled using thermionic emission of holes across the reverse-biased source Schottky barrier. This barrier is lowered by the image-force potential, and by the electric field generated by both source-drain and gate voltages. The gate voltage lowers the barrier height directly and in addition, modulates the effect of the source-drain voltage on barrier lowering.

Silicon nanowires (SiNWs) have, in recent years, shown great promise for the development of nanoelectronic, thermoelectric, solar cell, and biological/chemical sensing devices.\textsuperscript{1–3} In particular, SiNWs have attracted interest for high-performance field-effect transistor (FET) applications.\textsuperscript{4,5} Here, a SiNW forms the FET channel and provides a means to obtain good gate-control with high scalability. SiNW FETs are also, in principle, compatible with large-scale integrated processes. However, in many cases, Schottky barriers (SBs) exist at the metal contacts to the SiNW,\textsuperscript{2} forming a SB FET. The gate voltage then modulates the SB and strongly influences the FET characteristics.

SiNWs with minimum diameters $<10$ nm, and lengths up to $\sim 100$ nm, are often prepared by vapor-liquid solid growth or high-resolution lithographic techniques.\textsuperscript{6,7} More recently, SiNWs have been prepared by metal assisted chemical etching (MACE) of Si wafers. Here, electroless deposition of a silver dendritic network on a Si wafer catalyzes subsequent chemical etching of a vertical, densely packed SiNW array. SiNWs with diameter from $\sim 20$ to $300$ nm and length up to $\sim 150$ $\mu$m have now been demonstrated for FET, thermoelectric, and solar cell applications.\textsuperscript{4,8,9} In comparison with other preparation techniques, the MACE process is low cost and only requires wet-etching of a Si wafer. Furthermore, SiNWs may be formed over the entire wafer surface,\textsuperscript{9} with density $\sim 10^9$/cm$^2$.

In this paper, we demonstrate that the lowering of a reverse-biased SB may be used to explain the electrical characteristics of FETs using SiNWs prepared by MACE. The SBs are formed using Ti$_x$Si$_{1-x}$/Al silicide contacts. We find that in $p$-channel FETs, the experimental $I_{SD}/V_{SD}$ source-drain output characteristics, at various gate voltage $V_G$, may be modeled using thermionic emission of holes across the reverse-biased source SB. This barrier is lowered by the image-force potential, and by the local electric field caused by $V_{SD}$ and $V_G$. We find that once $I_{SD}$ begins to saturate, SB lowering is sufficient to explain both the drain and gate voltage dependence of the characteristics.

Our SiNWs were synthesized as follows. A [100] Si sample ($p$-type, doped with boron at $10^{18}$/cm$^3$) was immersed in hydrofluoric acid (HF)/AgNO$_3$ solution at room temperature for 5 min. In solution, several processes occur simultaneously. Ag particles deposit on the substrate by electroless metal deposition, a network of Ag dendrites grows from these particles, and the Si substrate is etched. Etching is accelerated using nitrate ions as an oxidizing agent. Left for 2 h, this produces a densely packed, vertical, SiNW array with NWs $\sim 150$ $\mu$m long. HNO$_3$ is then used to remove the Ag. Figure 1(a) shows a scanning electron micrograph of the SiNW array, where SiNW diameters vary from 40 to 300 nm and the NW density is $\sim 10^9$/cm$^2$. The SiNWs can be extremely long, with maximum aspect ratio $\sim 3000$. Figure 1(b) shows a transmission electron micrograph of a SiNW. The NW surface roughness is $\sim 1–5$ nm, and there is a $\sim 5$-nm-thick surface oxide layer. After etching, the SiNWs can be dispersed in isopropyl alcohol (IPA) using ultrasonic agitation.

Our SiNW $p$-FETs, shown schematically in Fig. 1(c), are fabricated as follows. A $p$-type Si wafer with a thermally-grown 150-nm-thick oxide layer forms the device substrate,
above $V_{SD} \sim 1.5$ V. $I_{SD}$ rises throughout the saturation region, increasing more rapidly at higher $V_{SD}$. As $V_G$ varies from +4 to −4 V, the channel conductance $g_{SD} = \partial I_{SD} / \partial V_{SD}$ increases. The inset to Fig. 2(a) shows the corresponding $I_{SD}$-$V_{SD}$ transfer characteristics. The maximum on-off ratio $I_{on} / I_{off} \sim 1500$, for $V_{SD}=2$ V. The peak value of the extrinsic transconductance $g_m = \partial I_{SD} / \partial V_{BG}=19$ nS, at $V_{SD}=5$ V and $V_{BG}=-2$ V, and the minimum sub-threshold swing $S = 750$ mV/decade. Figure 2(b) shows the $I_{SD}$-$V_{SD}$ characteristics on a log-log plot. The characteristics shift to higher $V_{SD}$ as $V_G$ increases from −4 to +4 V, implying an increase in $I_{SD}$ with $V_G$.

We explain the device characteristics by considering SB lowering at the source contact, as a function of $V_{SD}$ and $V_G$. Figure 3 shows schematically the energy band diagram in a p-channel SB SiNW FET. At $V_{SD}=V_G=0$, SBs lie along the conduction path at both source and drain contacts [Fig. 3(a)]. For $V_{SD}>0$ V, the source SB is reverse-biased and the drain SB is forward-biased. Current flow then consists of holes injected into the NW across the source SB. At small $V_{SD}$, the drain SB is not completely forward-biased and forms a potential barrier along the current path [Fig. 3(b)]. As $V_{SD}$ increases further, the drain SB is fully forward-biased [Fig. 3(c)]. $I_{SD}$ is then controlled solely by the reverse-biased source SB.

We find that the $I_{SD}$-$V_{SD}$ characteristics in the saturation region (Fig. 2) can be modeled by thermionic emission of holes across the reverse-biased source SB, and lowering of the SB height with $V_{SD}$ and $V_G$. We approximate the voltage drop across the SB as a fraction $C$ of the voltage applied across the device. $I_{SD}$ is then given by the equation for thermionic-emission current across a reverse-biased SB:

$$I_{SD} = S A^* T^2 \exp \left( \frac{-e(\phi_B - \Delta \phi_B)}{kT} \right) \left\{ \exp \left( \frac{eC V_{SD}}{kT} \right) - 1 \right\},$$

where $S$ is the SiNW channel cross-sectional area, $T$ is the absolute temperature, $\phi_B$ is the SB height at zero bias [Fig. 3(a)], $e$ is the electronic charge, and $k$ is the Boltzmann constant. $A^*$ is the effective Richardson constant. $\Delta \phi_B$ represents SB lowering [Fig. 3(c)], and is given by the following expression:

![Figure 2](image1.png)

![Figure 3](image2.png)
\[ \Delta \phi_B = 2 \left( \frac{eE_{SD}}{16 \pi \varepsilon_r} \right)^{1/2} + \alpha E_{SD} + \beta E_G, \]

where \( \varepsilon_r \) is the static semiconductor permittivity, and \( E_{SD} \) and \( E_G \) are the maximum values of the electric field at the source SB, caused by \( V_{SD} \) and \( V_G \), respectively. Here, we have extended the basic model to include \( E_G \) explicitly. The first term in Eq. (2) gives image force lowering of the SB due to charge near the metal surface.\(^{12} \) The second term is a first order approximation of the contribution of \( E_{SD} \) to SB lowering.\(^{12,13} \) The final term approximates the direct contribution of \( E_G \) to SB lowering. The factors \( \alpha \) and \( \beta \) determine the proportion of SB lowering caused by \( E_{SD} \) and \( E_G \), respectively. Together, \( \alpha \) and \( \beta \) determine the distance \( x \) from the interface to the SB potential maximum [Fig. 3(c)]. Finally, we allow \( \alpha \) to vary with \( V_G \), as the contribution of \( V_{SD} \) to SB lowering can vary at different \( V_G \).

We use Eqs. (1) and (2) to model the experimental \( I_{SD}-V_{SD} \) characteristics in the saturation region (\( V_{SD} > 1.5 \) V). \( E_{SD} \) is calculated using the depletion approximation, \( E_{SD} = \sqrt{2eN_d/\varepsilon_r} (\phi_B - CV_{SD} - \xi - kT/e), \)\(^{11} \) where \( N_d \) is the doping density and \( \xi \) is the valance band \( E_V \) to Fermi level \( E_F \) offset in the SiNW. The theoretical fits to the data (solid lines, Fig. 2) match the data well. The zero-bias SB height, extracted from our fits, is \( \phi_B = 0.4 \) eV. The inset to Fig. 2(b) shows the relationship of \( \alpha \) and \( \beta E_G \) with \( V_G \). As \( V_G \) increases from -4 to +4 V, \( \alpha \) increases from 0.23 to 1.7 nm, and \( \beta E_G \) reduces from 0.15 to -0.43 V. The increase in \( \alpha \) implies a greater contribution to SB lowering \( \Delta \phi_B \) by \( V_{SD} \) as the FET turns “off” [Eq. (2)]. In contrast, \( \beta E_G \) reduces as the FET turns off, tending to enhance the SB at positive \( V_G \). This implies a reduction in \( \Delta \phi_B \) and an increase in the total SB height \( \phi_B - \Delta \phi_B \). The combined effect of \( \alpha \) and \( \beta E_G \) gives the change in both the magnitude and slope of \( I_{SD} \) with \( V_{SD} \) and \( V_G \). Figure 3(d) shows the gate dependence, at constant \( V_{SD} = 4 \) V, of the three SB lowering terms constituting Eq. (2), i.e., the image force lowering [first term, Eq. (2)], \( \alpha E_{SD} \) and \( \beta E_G \). In our model, image force lowering does not depend on \( E_G \) and is constant. The net effect of these terms is a reduction in the magnitude of \( \Delta \phi_B \) as \( V_G \) increases, corresponding to reduced SB lowering.

Finally, the low bias region (\( V_{SD} < 1.5 \) V) may be modeled by assuming that \( C \), the proportion of \( V_{SD} \) that drops across the SB, increases with \( V_{SD} \). This is because at low bias, the drain SB also contributes to the source-drain resistance [Fig. 3(b)]. Furthermore, there may be voltage drops along the SiNW due to potential barriers in the NW,\(^2 \) e.g., if \( |\xi| \) is increased locally due to increased surface depletion. As \( V_{SD} \) increases, both the drain SB and any NW barriers are pulled-up relative to the source Fermi energy and ultimately, the source SB dominates [Fig. 3(c)]. We find that \( I_{SD} \) increases very rapidly, with \( C = 0.044 V_{SD} \)\(^3 \) for \( V_{SD} < 1.5 \) V. For \( V_{SD} > 1.5 \) V, where the source SB dominates, \( C = 0.15 \).

In conclusion, we consider the influence of SB lowering in SiNW FETs using NWs prepared by MACE. The reverse-biased source SB is lowered by the image-force potential, and by the local electric field caused by both \( V_{SD} \) and \( V_G \). In the saturation region, SB lowering is sufficient to explain both the drain and gate voltage dependence of the device characteristics.

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