Monolithic Large-Signal Transimpedance Amplifier for Use in Multi-Gigabit, Short-Range Optoelectronic Interconnect Applications

Antonio Vilches, Rodney Loga, Mouhamed Rahal, Kristel Fobelets, Christos Papavassiliou, and Trevor J. Hall

***Abstract*—A novel large-signal transimpedance amplifier front-end, intended for monolithic integration with a Si p-i-n diode and employing HBT-CMOS technology for use in short-range optoelectronic interconnects is proposed. Simulated bandwidth and gain are >4 Gbits/s and 43 dBΩ, respectively, while driving a 100-fF load to TTL voltage levels.**

***Index Terms*—BiCMOS, front-end, integrated, monolithic, optoelectronic interconnect, transimpedance amplifier, wide-bandwidth.**

I. Introduction

INCREASING bandwidth demand on data networks linked by photonic routers (intranet/internet) has resulted in the need for short-distance; high-speed fiber-optic interconnects which incorporate low complexity "pixel" (photodiode plus amplifier) receiver front-ends capable of increased throughput [1]. The availability of media-access-control (MAC) chipsets that include encoding–decoding functionality and deskewing circuitry means that the most important issues governing the development of the photoreceiver front-end is increasing its bandwidth while reducing size, cost and thermal dissipation [2]. Transimpedance (TZ) amplifiers have been widely used to convert the detected photocurrent to the voltage levels necessary for driving successive logic stages and designers have traditionally turned to costly III-V group technologies for the implementation of high-bandwidth TZ amplifier stages [3], [4] but the emerging availability of deep-submicron CMOS technologies offer a cheaper alternative with the added advantage of complete monolithic integration with subsequent CMOS logic circuitry. Bandwidth-enhancements by the application of a capacitive peaking technique to simple CMOS TZ amplifiers have been reported [5], [6] but these amplifiers still rely on linear operation to detect the large-signal pulsed inputs typical of photonic communication systems. A better approach would be to use a large-signal amplifier for the purpose. In this paper, we introduce a novel large-signal BiCMOS variant of the "classic" CMOS TZ amplifier in which no feedback resistor is used and yet bandwidth and stability are greatly increased by the negative current-feedback technique employed. The theory of "classic" linear transimpedance amplifiers is revisited in Section II-A and our proposed large-signal TZ amplifier/buffer variant is discussed in Section II-B. Simulated results are presented in Section III, while conclusions are outlined in Section IV.

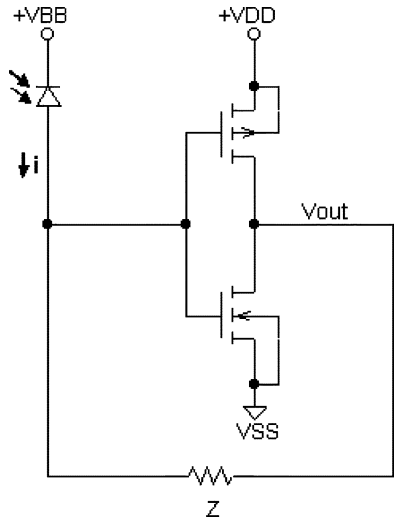

Fig. 1. A simple CMOS transimpedance amplifier.

II. Methods

A. Classic CMOS Transimpedance Amplifier Design

In classic linear CMOS monolithic transimpedance amplifier design, it has become standard practice to use the channel of a MOSFET as the feedback "resistor" integrated with an inverter/amplifier. An example circuit is shown in Fig. 1. Provided the source and drain voltages remain close, the MOSFET behaves as a resistor with a value determined by the voltage between the gate and the channel. The advantage of this arrangement is a significantly smaller parasitic capacitance than can be achieved by using either integrated or external resistors with the additional facility of automatic gain control [7], [8].

However, the MOSFET only behaves as a linear resistor for small signal output, rendering the approach unsuitable for applications requiring a large signal to be generated using a minimum of stages, i.e. as in optoelectronic interconnect applications in which the footprint and power consumption of the photoreceiver

Manuscript received April 25, 2002; revised February 26, 2004. The paper was recommended by Associate Editor K. Pedrotti.

A. Vilches, R. Loga, M. Rahal, K. Fobelets, and C. Papavassiliou are with the Department of Electrical and Electronic Engineering, Imperial College London, London SW7 2BT, U.K. (e-mail: a.vilches@ic.ac.uk).

T. J. Hall is with the School of Information Technology and Engineering (SITE), University of Ottawa, Ottawa, ON K1N 6N5, Canada.

Digital Object Identifier 10.1109/TCSII.2004.840111

are issues. The output of a classic (linear) transimpedance amplifier is given by

$$v_{\text{out}} = -\left[\frac{\text{A}}{(\text{A}+1)}\right] iZ \cong -iZ \tag{1}$$

where A is the closed-loop amplification, i is the input current, and Z is the value of the feedback resistance. As the gain-bandwidth product is fixed, it follows that maximum bandwidth is achieved with minimum gain or minimum feedback resistance. Equation (1), used extensively in operational amplifier based circuits, is applied to CMOS circuits when under the erroneous assumption that the CMOS inverter acts as an ideal voltage amplifier, with high-input impedance and low-output impedance. In practice, a CMOS inverter acts as a good transconductance amplifier, with high-input impedance and output impedance equal to the feedback MOST's small channel resistance, r_{ds}, in a small signal analysis. The correct behavior is found by making the substitution

$$Z \rightarrow Z + r_l$$
$$v_{\text{out}} \rightarrow v_{\text{out}} + ir_l$$

Where r_l is the parallel combination of the individual drain–source resistances of the two devices, with any load resistance. This gives

$$v_{\text{out}} = -\left\{\left[\frac{A}{(A+1)}\right](Z + r_l) - r_l\right\} i \tag{2}$$

$$Z_{\text{in}} = \frac{(Z + r_l)}{(A+1)}. \tag{3}$$

Deviation from expected behavior occurs when the feedback impedance is comparable to or smaller than the intrinsic output impedance of the inverter. The bandwidth is still maximized in the limit $Z \rightarrow 0$ but the *output voltage remains finite in this limit and is no longer inverted*

$$v_{\text{out}} = Z_{\text{in}} i \tag{4}$$

$$Z_{\text{in}} = \left[\frac{r_l}{(A+1)}\right] = \frac{1}{\left[g_m + \left(\frac{1}{r_l}\right)\right]}. \tag{5}$$

In this limit the "inverter" acts as a *dynamic load* with an equivalent resistance close to $(1/g_m)$ and in order to behave as a conventional transimpedance amplifier the 'inverter' must be connected to a load that has lower impedance than the feedback impedance. It is also necessary that A is kept large and this requires devices that are sufficiently large to provide a sufficient transconductance. Unfortunately, large parasitic capacitance is also associated with large devices. The gate–source capacitances of the devices add directly to the photodiode capacitance and may be effectively reduced by the transimpedance action. On the other hand the gate–drain capacitance appears directly across the feedback resistor and due to the Miller effect, this capacitance can be the limiting factor with regards to bandwidth; in a monolithic implementation the device capacitances, especially if Miller amplified, can easily dominate the photodiode capacitance.

B. Proposed Large-Signal Transimpedance Amplifier

The transimpedance amplifier design proposed here, Fig. 2, is in essence a CMOS inverter-based transimpedance amplifier without a feedback resistor, as in the classic sense. The inverter is used as a dynamic load that is driven by a current amplifier within a negative feedback loop. With "zero" feedback resistance, the output and input voltages are identical and the Miller multiplication of the gate–drain capacitance is zero (the drain–gate capacitance is shorted by the feedback connection).

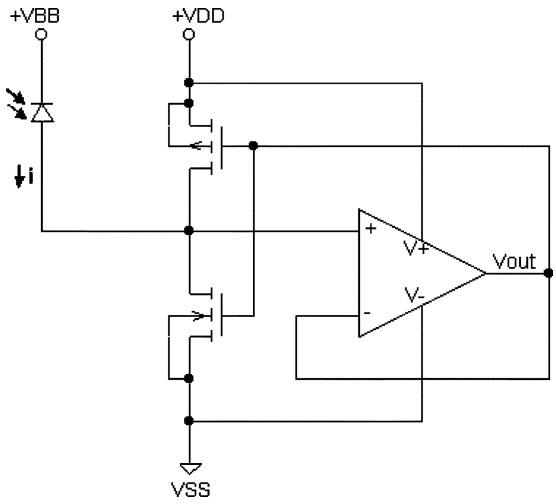

Fig. 2. A voltage follower is inserted to isolate the gate–source capacitance of the dynamic load from the photodiode and to increase output drive capability, but otherwise the circuit is identical to Fig. 1.

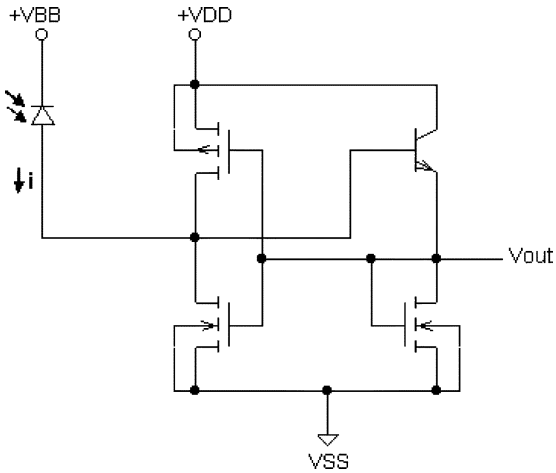

Fig. 3. Dynamic load "inverter" with BJT emitter follower and MOST active load combination as the voltage follower.

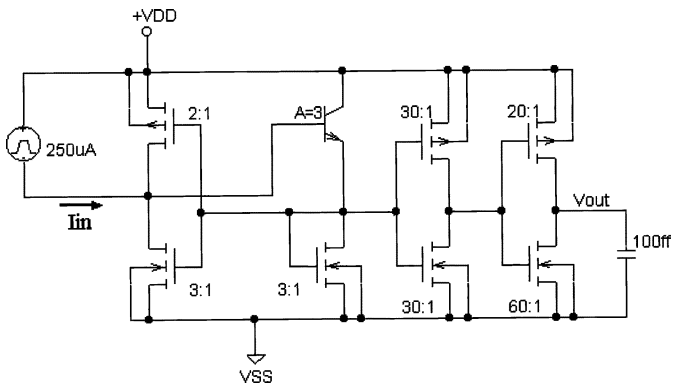

Fig. 4. The simulated current amplifier consisting of an 'inverter' dynamic load block followed by a CMOS inverter/amplifier stage.

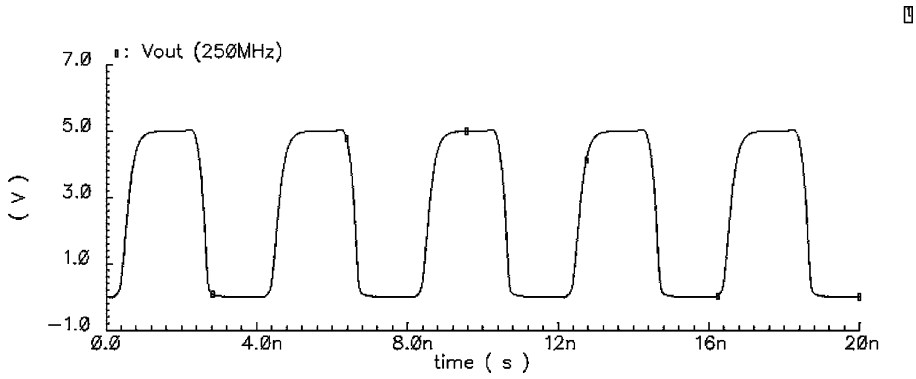

Fig. 5. Transient output voltage at 250 MHz.

The reduction of the gate source capacitances that appear across the photodiode favors smaller devices that also increase the output voltage due to the increase in $(1/g_m)$, however, this reduces the capability of the circuit to drive the next stage. This problem can be solved by inserting a voltage follower stage before the CMOS "inverter" and taking the output from the voltage follower, as shown in Fig. 2.

The unity voltage gain ensures that the circuit operates in the same manner as before and in particular the Miller effect remains absent. However, the buffering action of the voltage follower isolates the photodiode from the input capacitance of the inverter and the subsequent stage and equivalently improves the drive capability, i.e., the output impedance of the circuit is now less than the load seen by the photodiode. The best performance is achieved when the time constant of the dynamic load and photodiode capacitance just limits the bandwidth to the specified target as this offers the best compromise in gain versus bandwidth for any given photodiode/load configuration.

If the gate–source capacitance would otherwise dominate the photodiode capacitance, the insertion of the buffer will deliver a significant increase in bandwidth to the extent that it's input capacitance is much smaller than the gate-source capacitance of the dynamic load MOSTs. It is helpful in this respect that the unity feedback fraction increases the input impedance of the voltage follower, $Z_{\text{follower in}}$, and hence *decreases the effective input capacitance*, as well as decreasing the output impedance $Z_{\text{follower out}}$

$$Z_{\text{follower in}} = (1 + A_D)Z_i \tag{6}$$

$$Z_{\text{follower out}} = \frac{Z_o}{(1 + AD)} \tag{7}$$

where A_D is the intrinsic differential no-load voltage gain, Z_i is the intrinsic input impedance, and Z_o is the intrinsic output impedance of the follower gain block.

The relevant formulas[1] for a bipolar transistor emitter follower are

$$A_D = \frac{(1 + h_{fe})Z_o}{Z_i} \tag{8}$$

$$Z_i = h_{ie} \tag{9}$$

$$Z_o = \frac{1}{\left[h_{oe} + \left(\frac{1}{z_l}\right)\right]} \tag{10}$$

and for a MOST source follower

$$A_D = g_m Z_o \tag{11}$$

$$Z_i = \frac{1}{j\omega c_{gs}} \tag{12}$$

$$Z_o = \frac{1}{\left[\left(\frac{1}{r_{ds}}\right) + \left(\frac{1}{z_l}\right)\right]}. \tag{13}$$

The voltage follower has unity voltage gain but provides *current gain*: the circuit is capable of delivering a current into a load that is greater than that input by the photodiode. The origin of this current gain is the forward current gain of the transistor in the bipolar case.

In the current perspective, Kirchoff's current law at the input node ensures that an error current is passed to the voltage follower that is equal to the difference between the photodiode current and the feedback current sourced/sunk by the CMOS inverter. This feedback current is equal to the error current multiplied by the overall current gain of the voltage follower/CMOS inverter combination. The action of the overall combination as a current amplifier[2] may be considered to arise by several equivalent mechanisms.

1) The error current flowing through the input impedance of the voltage follower produces a voltage that is passed to its output via its voltage follower action, thus providing the output voltage. This voltage is converted into the feedback current via the transconductance action of the CMOS inverter (voltage follower perspective).
2) The error current flows into the input of the buffer and is amplified by the current gain of the buffer to produce an output current that flows through the buffer's load to produce the output voltage. This voltage is converted into the feedback current via the transconductance action of the CMOS inverter (emitter follower perspective).
3) The error current flowing through the intrinsic input impedance of the buffer generates a voltage that in turn produces an output current via the transconductance action of the buffer. The output current flows through the load to produce an output voltage. This voltage is converted into the feedback current via the transconductance action of the CMOS inverter (source follower perspective).

[1]These formulas must be modified if the source impedance is not small compared to the intrinsic input impedance and the load is not large compared to the intrinsic output impedance.

[2]This combination fails to be a *good current amplifier* on account of its high input impedance. The combination is best modeled as a transconductance amplifier. The error signal is, however, derived from a difference of currents.

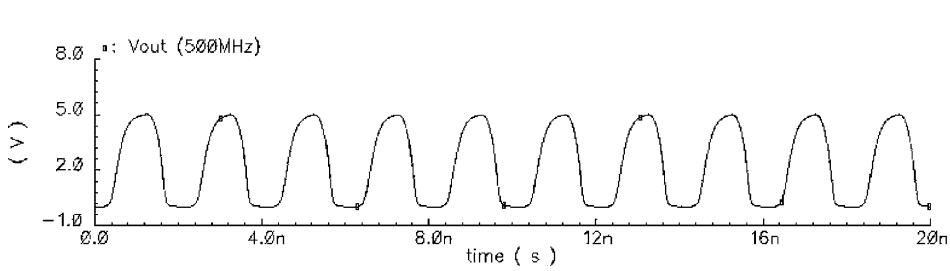

Fig. 6. Transient output voltage at 500 MHz.

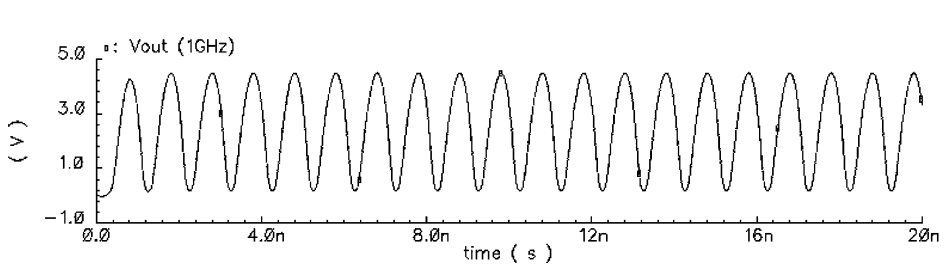

Fig. 7. Transient output voltage at 1 GHz.

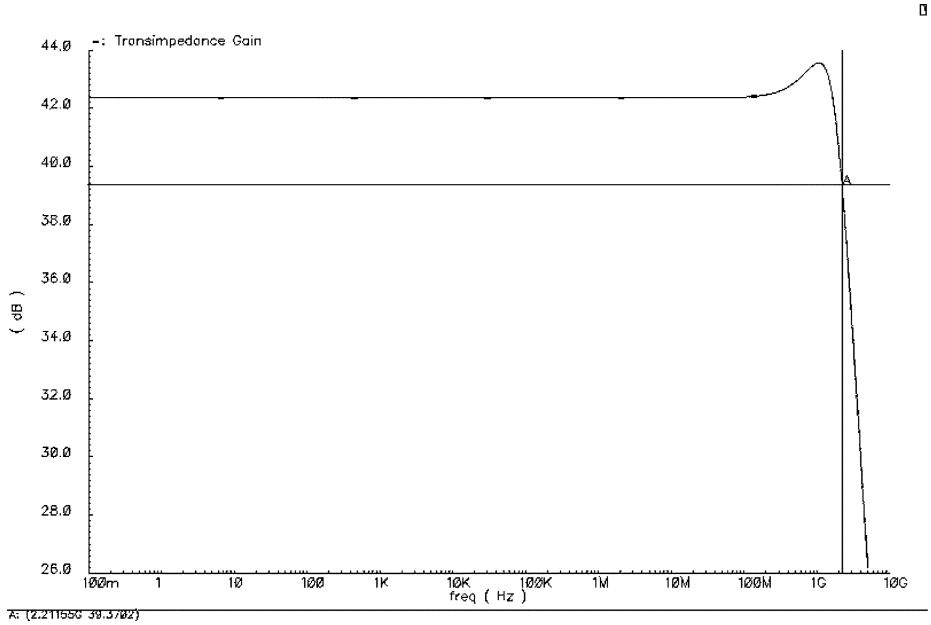

Fig. 8. Transimpedance gain versus frequency.

Whatever the perspective, the feedback action ensures that the voltage at the gates of the CMOS inverter moves in such a way as to correct a current imbalance caused by the injection into the node of the external current (photocurrent), i.e., the error current is reduced to zero (in the approximation that the buffer has an infinite input impedance). The core circuit is implemented here, as shown in Fig. 3.

The bipolar emitter follower was chosen in preference to a MOST source follower on the basis that the BJT required smaller dimensions than a MOST implementation and the base–collector capacitance of the BJT was smaller than the corresponding gate–drain capacitance of the MOST [9].

The "inverter" and HBT-nMOS "feedback" block needs to be followed by one or more voltage gain sections in order to produce the necessary logic level output voltage swing. The final circuit is then as shown in Fig. 4, and in this implementation the total circuit footprint is 123 μm^2. For greater gain, or, in order to drive a greater load, three transimpedance amplifier "blocks" consisting of the dynamic load, feedback circuitry, and a single output inverter, could be cascaded as published in [10], where a cascade of three broad-band amplifiers are used to implement a photoreceiver. Similarly, if TTL level voltage outputs are not required; the output inverters' footprint can be reduced with a consequent small increase in bandwidth.

III. Results

The circuit has been simulated using device files from the 0.8-μm BiCMOS BYS process offered by Austria Mikro Systeme [11] in CADENCE CAD software, using an equal

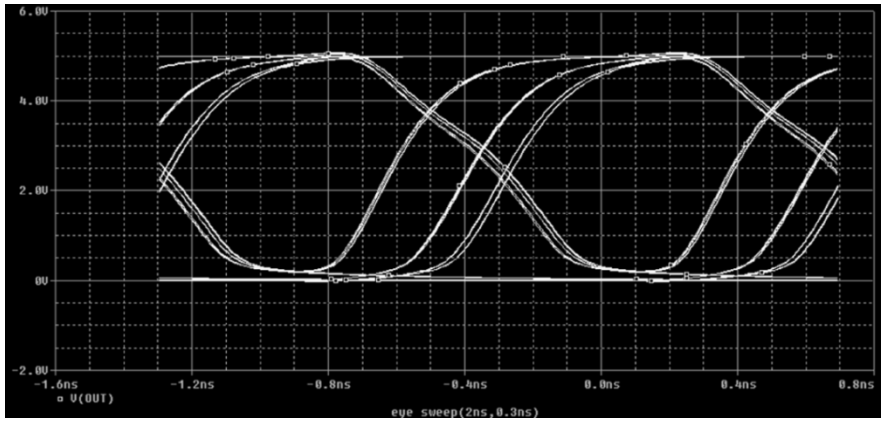

Fig. 9. A simulated eye diagram of the circuit operating at 2 Gbits/s. An 8000 sample long pseudorandom non-return-to-zero (NRZ) bit sequence employing a pulse period of 1 ns is used.

mark-space ratio, pulsed current-source input of 250 μA pk-pk, whilst driving a capacitance load of 100 fF. A 10 000 sample long, pseudorandom signal bit-stream required for the rendering of simulated eye-diagrams was generated in Matlab software (www.mathworks.com) and imported into Cadence via the independent current source component 'IPWL_File'.

Simulations at 1 GHz indicate a required sensitivity of 128 μA input to produce 1 V output at the HBT's emitter and a 44-μA input to produce 1 V output into the 100-fF capacitor load. This translates to a minimum required input of 220 μA $(5 \times 44\ \mu\text{A})$ to produce a 5-V rail-to-rail voltage swing into the capacitor load.

Figs. 5–7 illustrate the predicted transient voltage output at 250 MHz, 500 MHz, and 1 GHz, respectively, and the output can clearly be seen to switch to within 0.5 V of the 5-V supply rail. The maximum power consumption at 1 GHz is 22.8 mW. A half-power bandwidth of 2.2 GHz (4.4 Gbits/s) can be determined from the transimpedance gain versus frequency plot, Fig. 8.

A simulated eye diagram of the circuit operating at 1 GHz (2 Gbits/s), illustrating sufficient "eye" clearance to warrant operation at up to this frequency, is given in Fig. 9.

IV. Conclusions

It is concluded that the dominance of parasitic capacitance of active devices over a monolithically integrated photodiode capacitance and the requirement of a low complexity photo-receiver capable of operating in the large signal regime, leads the designer away from traditional transimpedance photo-receiver designs. An approach based on a buffered dynamic load concept and its relationship to published high performance broad-band amplifiers has been described. This design concept shows promise both for the envisaged optical interconnect application and, in its manifestation as a broad-band voltage amplifier, as a stage within photo-receivers of greater complexity based on traditional small signal transimpedance designs [10].

A single transimpedance photo-receiver, with associated common-source amplifier, capable of TTL voltage level output, has been simulated using the 0.8 μm BiCMOS BYS process offered by Austria Mikro Systeme in CADENCE CAD software resulting in a predicted bandwidth of $>$4 Gbits/s and a transimpedance gain of $>$43 dB. The circuit footprint is 123 μm^2 and power consumption is $<$23 mW at 1 GHz.

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