Average Drift Mobility and Apparent Sheet-Electron Density Profiles in Strained-Si–SiGe Buried-Channel Depletion-Mode n-MOSFETs

Kostis Michelakis, *Member, IEEE*, Antonio Vilches, Christos Papavassiliou, Solon Despotopoulos, *Member, IEEE*, Kristel Fobelets, and Chris Toumazou, *Fellow, IEEE*

***Abstract*—In this paper, we describe a simple method to extract the average drift mobility and the apparent sheet electron density versus the applied gate voltage and the vertical effective electric field in strained-Si–SiGe buried-channel depletion-mode metal–oxide semiconductor field-effect transistors (n-MOSFETs). For this, we adapted an established technique used in evaluating mobility profiles in Schottky-gate MESFETs, by taking into account the existence in our devices of the gate-oxide capacitance $C_{\rm OX}$ and by introducing an effective junction capacitance C_D, which follows the ideal Schottky's depletion approximation. By applying our method on fabricated transistors we were able to obtain the average drift mobility profile versus the applied vertical effective field and monitor values as high as 618 cm^2/Vs. We also extracted the apparent sheet electron density profile with values reaching as high as 3.4×10^{12} cm^{-2}. Although the layer design had not been optimized, the results show mobility enhancement in the strained silicon channel and, to our view, point to a unique regime of operation for these devices, which should benefit the low-power and low-voltage applications. The proposed method could be used as a nondestructive tool for monitoring the transport properties in Si–SiGe modulation-doped MOSFETs. It could also serve as a useful platform for determining explicit modeling links between the layer design and the device performance.**

***Index Terms*—Drift mobility, heterostructure, metal–oxide semiconductor field-effect transistor (MOSFET) mobility, MOS-MODFET, SiGe, silicon, strained-si MOSFETs.**

I. Introduction

STRAINED-silicon n-type metal–oxide semiconductor field-effect transistors (n-MOSFETs), which make use of the Si/SiGe heterojunction, are known to sustain inversion channels with up to 70% enhanced mobility, compared to conventional silicon n-MOSFETs [1]. These are enhancement-mode (EM) devices and have surface channels (SC). But there is little found in the literature on their depletion-mode (DM) buried-channel (BC) counterparts, despite the fact that they too can share the convenience of a standard Si MOS process, and despite the advances in n-type strained-Si–SiGe modulation-doped field effect transistors (MODFETs), where cutoff frequencies in the range of 90 GHz have been reported [2]. In BC MOSFET, the semiconductor heterostructure contains multiple layers, with the carriers not always confined in the intended strained-Si channel, and the most relevant approach is to evaluate the free carrier density and the drift mobility profiles with the depth and/or with the vertical effective field and the applied gate bias. In our case though, we feel that the most suitable figures of merit are the average effective drift mobility and the apparent sheet electron density, as these parameters reflect the operation of the device as being a whole entity. A number of techniques for mobility and carrier density profiling have been developed and matured through the years, mainly on GaAs FETs, because of the multiple layers and the varying doping profiles involved in these devices. A review on such techniques and also a discussion on the apparent nature of the carrier concentration, along with the relevance of the Debye length, can be found in [3]. In this paper, we adapted the technique by Pucel and Krumm [5], which is used in evaluating mobility profiles in Schottky-gate MESFETs, by taking into account the existence in our devices of the gate-oxide capacitance $C_{\rm OX}$ and by introducing an effective junction capacitance C_D, which follows the ideal Schottkys depletion approximation. By applying this method on fabricated long-gate transistors we were able to obtain the low-field average drift mobility profile and the apparent sheet electron density profile versus the applied gate-to-source voltage and the vertical effective electric field. The method is detailed in Section II together with the assumptions that are used. In Section III, after a description of the device fabrication procedure, the experimental setup is explained and the results are analyzed and discussed. The conclusions are finally summarized in Section IV.

II. Assumptions and Method

Our method is based on the fundamental assumption that in Si–SiGe BC DM n-MOSFETs, of which an example heterostructure can be seen in Fig. 1, the measured total gate capacitance C_M can be expressed as a series combination of the oxide capacitance $C_{\rm OX}$, which is independent of the applied vertical bias and an effective junction capacitance C_D, which is bias dependent [4]

$$C_M^{-1}(V_{\rm GS}) = C_{\rm OX}^{-1} + C_D^{-1}(V_{\rm GS}) \tag{1}$$

$C_{\rm OX}$ is calculated at the highly positive gate bias limit, where all charge is attracted to the gate oxide interface, where C_D be-

Manuscript received October 28, 2003. This work was supported by EPSRC under Grant GR/N65851/01. The review of this paper was arranged by Editor C. McAndrew.

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Digital Object Identifier 10.1109/TED.2004.832727

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Thick. nm	Layer	Ge %	Doping x 10^{17} cm^{-3}	Description
10	Si	0	0	cap layer
10	SiGe	30	n = 10	donor layer
5	SiGe	30	0	spacer layer
8	**Si**	**0**	**0**	**strained channel**
100	SiGe	30	0	spacer layer
100	SiGe	30	p = 0.5	
1000	SiGe	30	p = 5	virtual substrate
1000	SiGe	0 - 32	p = 5	graded buffer layer
p-type Si substrate				

Fig. 1. Si–SiGe layer structure. The cap layer is used up to form the gate oxide. The shown parameters are nominal values.

comes infinite and $C_{\rm OX}$ equals the total measured capacitance. From (1) we get

$$C_D(V_{\rm GS}) = \left[1 - \frac{C_M(V_{\rm GS})}{C_{\rm OX}}\right]^{-1} C_M(V_{\rm GS}). \tag{2}$$

The introduced effective capacitance C_D is assumed to be an ideal junction capacitance, which follows Schottkys depletion approximation (i.e., the Debye length is equal to zero) and involves all active layers contained between the gate oxide and the virtual substrate. In this respect, the physical location of the upper plate of C_D is fixed at the interface between the gate-oxide and the semiconductor. On the other hand, the site of the lower electrode of C_D is variable and depends on $V_{\rm GS}$ or, equivalently, on the vertical electric field. The departure from the ideal depletion approximation suggests that, for a given vertical electric field value, the physical location of the lower plate is uncertain by several Debye lengths, but we overcome this by abandoning the conventional profiling with depth and rather deal with the magnitude of C_D versus the applied gate-source bias. This is equivalent to adopting the apparent nature of the profiled carrier concentration [3]. We consider that this is a valid assumption as long as the free charge of the device, which is modulated by $\rm V_{GS}$, can be turned off. In our measurements this condition is satisfied (see Section III and Fig. 2). The capacitance-voltage measurements can be performed at a frequency of around 1 MHz, as in GaAs FETs, since our transistors are majority-type too. A device with sufficient gate area is required in order for C_M to be safely detectable by the measuring equipment, and this requirement is only met by long-gate transistors of substantial width.

According to the drift approximation, the transistor drain–source current at low lateral electric field $E_{\rm eff} = V_{\rm DS}/L$ and for a given gate-source bias, is given by

$$I_{\rm DS}(V_{\rm GS}) = e\mu_D(V_{\rm GS})WN_S(V_{\rm GS})\left(\frac{V_{\rm DS}}{L}\right) \tag{3}$$

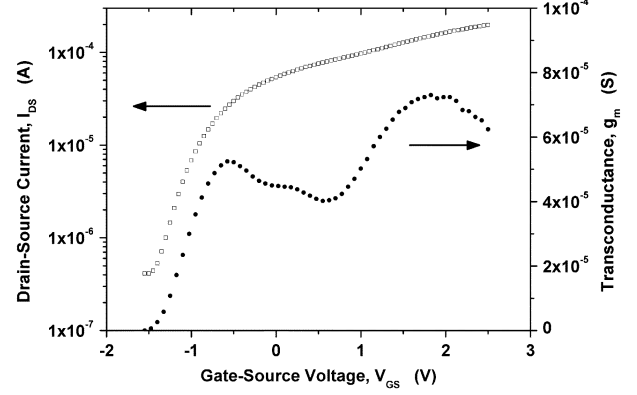

Fig. 2. Measured drain–source current and the corresponding transconductance in the linear region ($V_{\rm DS} = 0.1$ V). The threshold voltage is -1.2 V.

where e is the electron charge, μ_D is the effective low-field drift mobility and N_S is the sheet free-electron density. The current $I_{\rm DS}(V_{\rm GS})$ can be measured experimentally at dc. It is clear from the preceding discussion that both the mobility and the sheet electron density in (3) vary with varying $V_{\rm GS}$ and the introduction of C_D enables us to use one of the standard techniques [3] in order to obtain these profiles. In doing so, we opt for the method proposed by Pucel and Krumm [5], because it relates the capacitance C_D and the transconductance g_m of the transistor for each $V_{\rm GS}$

$$\mu_D(V_{\rm GS}) = \frac{g_m(V_{\rm GS})L^2}{C_D(V_{\rm GS})V_{\rm DS}}. \tag{4}$$

The correction terms in (4) have been omitted, since we experimentally deal with large area gates and we assume that the parasitic resistances are negligible compared to the channel resistance. The transconductance at a fixed drain–source voltage can be calculated from

$$g_m = \frac{dI_{\rm DS}}{dV_{\rm GS}} = g_m(V_{\rm GS}) \tag{5}$$

by using the dc measurement of $I_{\rm DS}$, but care has to be taken not to extend the calculations to high gate overdrive, where extra charge injection may occur, not accounted for by (1). Although this puts an upper limit on the voltage range in our extractions, high gate overdrive is not used in DM transistors anyway, as the device parameters deviate from their optimal values.

Having discussed the effective nature of C_D and the apparent nature of N_S under the depletion approximation, it is more than fair to expect that, the effective low-field drift mobility, as extracted via (4), will be an *average* measure of the carrier mobility at the given bias conditions, which will reflect the behavior of the device as a whole entity, at this specific bias point, *in combination* with the corresponding apparent carrier density. Furthermore, for obvious reasons, we have to make sure that both the current–voltage (*I–V*) and the capacitance–voltage (*C–V*) measurements are performed with the same voltage reference. This condition is imposed by the experimental setup, which is described in Section III.

Finally, in order to be able to compare our results with the literature, we have to perform the variable translation from $V_{\rm GS}$

to the corresponding vertical effective electric field E_{eff}. This is achieved by assuming that the field is induced by the free electron charge, according to

$$E_{\text{eff}}(V_{\text{GS}}) = \frac{eN_S(V_{\text{GS}})}{[\varepsilon_{\text{Si}} + \varepsilon_{\text{SiGe}}]/2} \qquad (6)$$

where $N_S(V_{\text{GS}})$ is calculated from (3), given the current measurement and the extracted drift mobility from (4). The average value of the permitivities of Si and SiGe appears in the denominator of (6).

III. Experiment, Results and Discussion

A. Device Fabrication Technology

The transistors were fabricated with the semiconductor structure of Fig. 1. The layer growth was performed by Qinetiq [6], using molecular beam epitaxy (MBE) on silicon and employing the SiGe *virtual substrate* approach [7]: The initial material was a high-resistivity p-type Si substrate. First, a graded-composition SiGe layer was deposited, followed by a relaxed p-type $Si_{0.7}Ge_{0.3}$ virtual substrate. The 8-nm-thick undoped strained-Si channel was then grown. An arsenic-doped (1×10^{18} cm^{-3}), 10-nm-thick $Si_{0.7}Ge_{0.3}$ donor layer then followed. This layer engineers the band gap discontinuity and donates the electron carriers to the resulting channel, within the strained-silicon layer. This is known as the *modulation doping* technique. Finally, a 10-nm undoped silicon layer was grown on top of the structure. This is used up during transistor fabrication for the formation of the gate oxide, as in conventional Si MOSFET processes. A poor-quality silicon surface channel may be present in the device after the completion of the fabrication procedure, if this cap layer is not totally consumed during oxidation.

The fabrication of the transistors started with mesa isolation. During this step, the active epitaxial layers are chemically removed around each device to a depth of 300 nm, down to the virtual substrate. Then, a standard Si MOS process was carried out, as follows: MOS device isolation consisted of 300 nm low-temperature oxide (LTO), deposited at 400 °C and the active areas were defined by patterning and etching using a buffered hydrofluoric acid (BHF) solution. Dry thermal oxidation at 800 °C for 60 min was used to grow the gate oxide. Calibration experiments showed that the resulting oxide thickness is 6 nm. 300 nm of amorphous Si were deposited and implanted with As (1×10^{15} cm^{-2}, 40 keV). Rapid thermal annealing (RTA) at 800 °C for 30 s was used to activate the polysilicon. The gate definition was carried out using electron beam lithography and dry etching. This produced gate lengths down to 300 nm and was followed by self-aligned source and drain As implant (5×10^{15} cm^{-2}, 40 keV). A 30 s rapid thermal annealing (RTA) at 825 °C was used for implant activation. The interlayer dielectric (ILD) consisted of 100-nm LTO (400 °C), followed by 200 nm of BPSG. Contact vias were then dry etched through the ILD. The metalization system consisted of sputtered Al (1% Si) with a Ti barrier layer. Devices of various dimensions became available for on-wafer characterization after processing. The required measurements for the application of our method and the experimental conditions are detailed next.

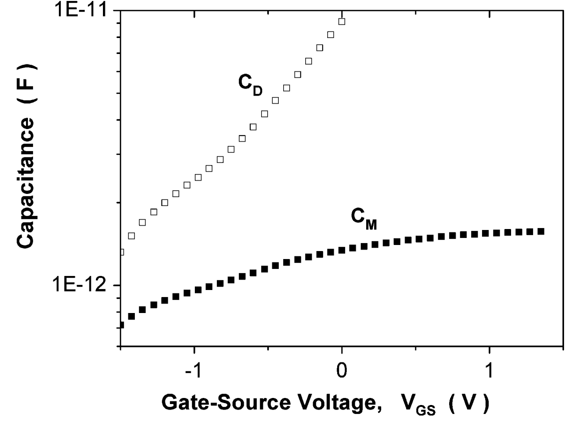

Fig. 3. Measured capacitance C_M and the extracted effective capacitance C_D plotted against V_{GS}. C_{OX} is equal to 1.575 pF.

B. Experimental Procedure and Measurements

The common-source dc *I–V* characteristic of the devices was measured using two Keithley sources, connected to the gate and the drain respectively. The *C–V* measurements were performed with the Keithley 590 CV analyzer, at a frequency of 1 MHz. Transistors with large gate area were used ($L = 20$ μm and $W = 100$ μm). This choice of large L and W ensures easily detectable capacitance values, helps keep the drain-source field low and serves as an effective means of "de-embedding" some extrinsic parasitic elements. Separate devices of the same geometry in close proximity were used for each of the combined *I–V* and *C–V* measurements and the voltage scans were started from the more negative values, to avoid irreversible effects and possible destruction of the devices at high V_{GS}. For the *I–V* measurements, the devices are treated as three-terminal, with the source grounded and the substrate floating. The V_{DS} is fixed at 0.1 V. For the *C–V* measurements, the transistors are treated as two-terminal, with source and drain tied together as one of the terminals, the gate as the second and the substrate floating. These conditions provide the same voltage reference for both the *I–V* and the *C–V* measurements. All measurements are performed at 300 K.

C. Profile Extractions

In applying our method, we first use the dc current measurement in the linear region of the transistor in order to extract the transconductance curve by differentiation, according to (5). Both the measured current and the extracted transconductance versus the applied gate-source voltage are shown in the graph of Fig. 2. The off-state current (i.e., the leakage current) of the device is measured at 4×10^{-7} A and the threshold voltage is -1.2 V. We then use the *C–V* measurement in order to extract the effective depletion capacitance $C_D(V_{\text{GS}})$, from (2). Fig. 3 shows both the measured capacitance C_{M} and the extracted capacitance C_D. C_{OX} is taken to be equal to 1.575 pF (see the relevant discussion in Section II). Having extracted $g_m(V_{\text{GS}})$ and $C_D(V_{\text{GS}})$ with matched voltage references, as pointed out previously, we may now use (4) to obtain the low-field average effective drift mobility profile versus V_{GS}. We can also obtain the apparent sheet electron density profile $N_S(V_{\text{GS}})$ from (3), given the current measurement and the extracted drift mobility

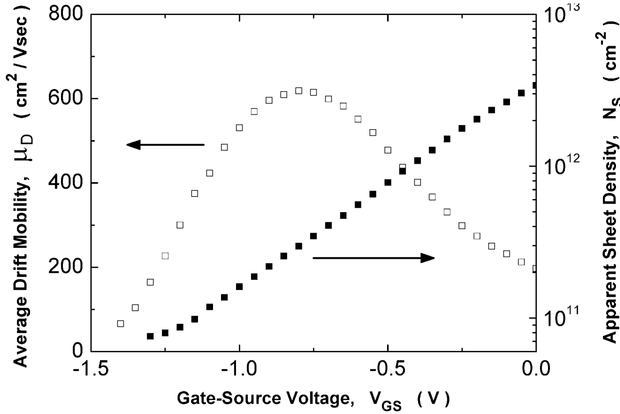

Fig. 4. The extracted low-field average effective drift mobility and the apparent sheet electron density versus the applied gate-source voltage.

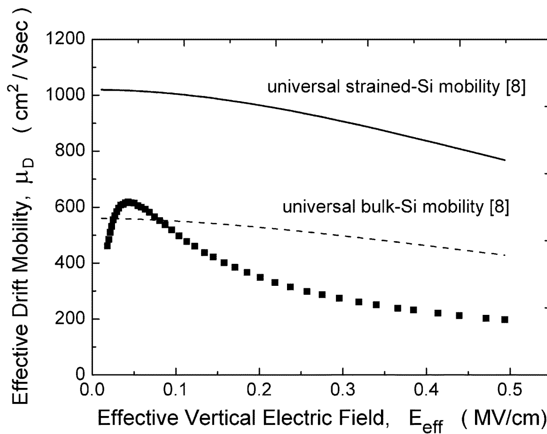

Fig. 5. Extracted low-field average effective drift mobility, plotted against the effective vertical electric field (square points). Also shown, the universal bulk-Si mobility and the strained silicon mobility from [8].

from (4). Both these profiles are included in the graph of Fig. 4. Finally, we perform the variable translation from V_{GS} to the effective vertical electric field using (6), as described in Section II, and plot the extracted average drift mobility versus the vertical electric field in Fig. 5. In the same figure and for comparison reasons, the dashed line shows the universal bulk-silicon mobility of an inverted surface channel while the solid line shows the universal mobility of a strained-Si surface channel, both from [8].

D. Discussion

In discussing these results, we should first observe the local maximum in the transconductance and the kink in the measured capacitance, both occurring at a bias around -0.75 V (see Figs. 2 and 3, respectively). Both these patterns can be qualitatively attributed to the presence of the buried transistor channel. The application of our method has quantitatively linked this information with the average drift mobility and the apparent sheet electron density profiles in our devices. In more detail and with regard to Fig. 4, N_S increases almost linearly with V_{GS} and shows saturation, while reaching the value of 3.4×10^{12} cm^{-2} (see Fig. 4). The corresponding drift mobility is low compared to bulk silicon standards (200 cm^2/Vs), after passing the maximum value of 618 cm^2/Vs, for $N_S = 3 \times 10^{11}$ cm^{-2}. This last value is apparently a measure of the maximum sheet electron density that the buried channel can support. For more positive gate-source voltage it will be reasonable to assume that the excess carriers cannot be confined within this intended channel. Observing the graph of Fig. 5 can draw a clearer picture. For low vertical electric field values, the mobility overshoots the universal curve, suggesting that a strained channel does indeed exist. But the amount of overshoot and the fact that, at very low fields an abrupt mobility drop occurs, is consistent with the presence of Coulomb scattering [8], [9]. This could mean the existence of excessive impurities or defects in the strained channel. Then, for higher electric field values, the transistor behaves as a poor-mobility device with surface-channel-like mobility degradation characteristics. As just mentioned, this degradation could be the result of poor electron confinement in the buried strained-Si channel, in which case the excess free carriers would use the heavily doped SiGe donor layer, situated directly below the gate oxide. A parasitic surface channel can also be formed if, during device fabrication, part of the silicon cap layer is left unused. In such a case, the scattering will be significant, as the layer structure has not been designed with this in mind, and there is no provision for an extra spacer layer. This parasitic channel, if present, is also bound to be very thin, a feature that is most likely to further degrade the mobility. In the worst case, both an unintentional silicon surface channel, together with poor electron confinement in the BC can be assumed. It is noted here that on-wafer S-parameter measurements on 0.5 μm gate transistors, revealed a current-gain cutoff frequency of 1 GHz, with an I_{DSS} of 126 mA/mm and a transconductance of 148 mS/mm. This poor high-frequency performance, despite the decent dc figures of merit, could be justified to a certain extent, given the extracted mobility and carrier density profiles just described.

As already mentioned, the layer structure used for this paper was not optimized. There is also room for improvements in the device fabrication process. All these are possibly reflected in the extracted transport parameter magnitudes. What could be more important though, is to observe the trends and, in doing so, it seems that there is a preferable regime of operation for the buried-channel depletion mode strained-Si–SiGe n-MOSFETs, in terms of mobility enhancement. This regime is clearly related to near-threshold and low drain-source voltage biasing conditions, according to our results. Furthermore, an important point to note regarding the proposed technique, is the use it could potentially have in device modeling.

IV. Conclusion

We have adapted simple and well-established characterization techniques to develop a method suitable for extracting the average drift mobility and the apparent sheet electron density profiles in strained-silicon buried-channel depletion-mode n-MOSFETs. By applying it on fabricated transistors we were able to assess their electrical quality and identify an optimum regime of operation. This method should be useful in establishing explicit modeling links between the layer design and

the device performance and also as a nondestructive tool for evaluating the device transport characteristics.

Acknowledgment

The authors are grateful to Dr. D. Haigh for his valuable comments. The semiconductor structure was supplied by Qinetic and the device fabrication was performed at the EPSRC Fabrication Facility, University of Southampton.

References

[1] K. Rim, J. L. Hoyt, and J. F. Gibbons, "Fabrication and analysis of deep submicrometer strained-Si n-MOSFETs," *IEEE Trans. Electron Devices*, vol. 47, pp. 1406–1415, July 2000.

[2] M. Zeuner, A. Fox, T. Hackbarth, D. Behammer, and U. Koenig, "90 GHz f_T SiGe HFET with fully optical self-aligned sub 100 nm gate," in *Proc. 60th Device Research Conf.*, 2002, pp. 53–54.

[3] K. Steiner, N. Uchitomi, and N. Toyoda, "Mobility profiles in submicrometer WN_x-BPLDD-GaAs MESFETs," *Jpn. J. Appl. Phys.*, vol. 29, no. 3, pp. 489–494, Mar. 1990.

[4] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley, 1982.

[5] R. A. Pucel and C. F. Krumm, "Simple method of measuring drift-mobility profiles in thin semiconductor films," *Electron. Lett.*, vol. 12, no. 10, pp. 240–242, 1976.

[6] [Online]. Available: www.qinetiq.com

[7] T. Hackbarth, G. Hoeck, H.-J. Herzog, and M. Zeuner, "Strained-relieved SiGe buffers for Si-based heterostructure field-effect transistors," *J. Cryst. Growth*, vol. 201/202, pp. 734–738, 1999.

[8] H. M. Nayfeh, C. W. Leitz, A. J. Pitera, E. A. Fitzgerald, J. L. Hoyt, and D. A. Antoniadis, "Influence of high channel doping on the inversion layer electron mobility in strained silicon n-MOSFETs," *IEEE Electron Device Lett.*, vol. 24, pp. 248–250, Apr. 2003.

[9] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of the inversion layer mobility in Si MOSFETs—Part I: Effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, pp. 2357–2362, Dec. 1994.

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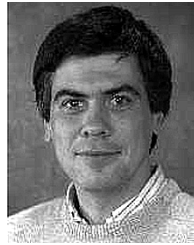

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