A 3 kW 3.39 MHz DC/DC Inductive Power Transfer System with Power Combining Converters

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***Abstract*—A 3.39 MHz, 2 kW nominal power DC/DC inductive power transfer systems has been developed and tested experimentally. It achieves 95% peak efficiency at 3 kW output, with a novel parallel push-pull Class E inverter using 650 V, 60 A GaN devices and a full bridge Class DE rectifier with 1.2 kV, 20 A SiC Schottky diodes. The entire system design procedure of the magnetic link and the converters is provided in detail. Such high frequency wireless power transfer systems are targeted towards high power applications with low coupling, where requirements for lightweight and compact receiver sides are crucial.**

***Index Terms*—inductive power transfer, resonant converters, soft-switching, wide-bandgap devices**

I. Introduction

The inverter topology with the highest power capability is the Class D full-bridge [1]. High power IPT applications at switching frequencies in the order of 10's of kHz have been demonstrated using silicon MOSFET [2] and IGBT [3] in the literature. However, at MHz switching frequencies the effect of the parasitic inductances of the printed circuit board (PCB) layout combined with the increase in switching losses and severity of electro-magnetic interference (EMI) issues because of the hard switching [4], make this kind of inverters impractical for high frequency (HF) inductive power transfer (IPT) applications.

Even though Class E type inverters are capable of operating efficiently at higher frequencies, the upper limit is set by the output capacitance of the device [5]. For this reason, granted that Si power MOSFET and IGBT modules can handle high currents and voltages, their large C_{oss}, combined with the high gate charge requirements and large parasitic inductances because of their typical packages [6], makes these power transistor technologies unsuitable at MHz frequencies.

GaN devices combined with Class E inverters overcome all of the above mentioned issues, with low input and output parasitic capacitances and compact dies that can fit in low inductance packages [7], [8]. The power capability of Class E type inverters is bound by the high drain voltage requirements, which can be much higher than the DC supply [9]. GaN transistors typically have a maximum drain voltage of 650 V [10], which is a major limiting factor for high power Class E inverters, and reduces efficiency because of the inevitable requirement of using designs with high currents and low voltages.

SiC technology offers higher breakdown voltages than GaN, with commercial devices going as high as 1.7 kV [11], and can withstand higher operating temperatures. A comparison of two Class Φ_2 2 kW IPT inverters was conducted at 6.78 MHz in [12], one being a single ended design with a custom 1.2 kV SiC for reduced parasitics, and the other a push-pull with GaN. The inverter with the GaN still had higher operating efficiency, despite having twice the amount of components and omitting the gate losses in both examples.

(a) Primary coil (b) Secondary coil (c) Link distance

Fig. 1: Photos of the primary and secondary coils used in the high power IPT DC/DC system example. Both coils are square planar made of copper tube. The outer dimension of the 3-turn Tx coil is 43 cm, with 6 cm distance between turns and 8 mm tube diameter. The outer length of the 2-turn Rx coil is 37 cm, the distance between turns is 1 cm, and the tube diameter is 10 mm.

II. Inductive Link Measurements

The design process begins with the coil impedance measurements, using the E4990A impedance analyser from Keysight, with the coils connected to their respective PCBs. Photos of the transmitter (Tx) and receiver (Rx) coils are shown in Fig. 1, with details about their dimensions in the description. The Tx coil has 3 turns for high inductance, and a large gap between turns to keep the self resonance frequency (SRF) high. The secondary coil has two turns, which enables lower gap between turns, while keeping the inductance low enough to be able to

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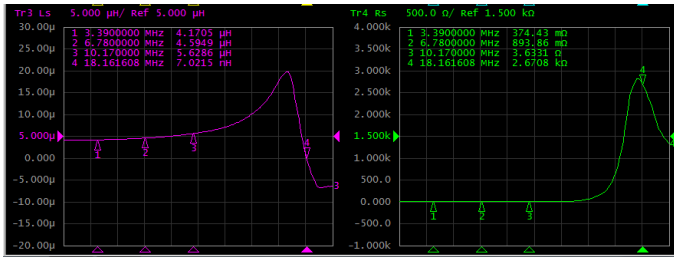
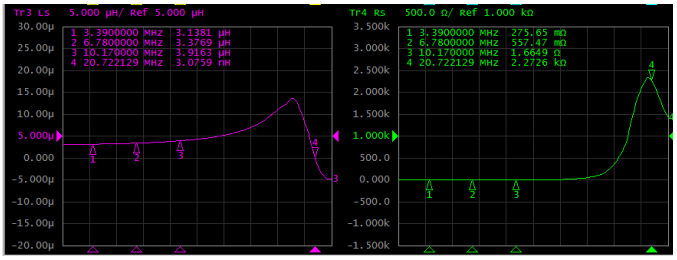


(a) Primary coil



(b) Secondary coil

Fig. 2: Impedance analyser measurements of the coils in Fig. 1. In purple are the inductance and in green are the resistance measurements. The first three frequency marks correspond to the first three harmonics of the IPT system and the fourth mark is at the resonance frequency of the respective coil.

absorb the capacitive reactance of the rectifier. Screenshots of the results of the impedance measurements for the two coils are shown in Fig. 2, based on which we determine the inductances and quality (Q) factors used in the design procedure of the converters.

The measured inductance values agree with the analytic low frequency approximations from [13], where $L_{s_1} = 4.11\,\mu\text{H}$ (Tx coil inductance) and $L_{s_2} = 3.44\,\mu\text{H}$ (Rx coil inductance). Another noteworthy observation from Fig. 2 is that the SRF of both coils is well above the operating frequency (around $20\,\text{MHz}$), which makes them well suited for the application.

The next step involves the determination of the distance between the two coils and accurately measurements of the coupling factor. For an IPT system design with high link efficiency it is important that the combination of coil distance and AC equivalent secondary load result in high enough reflected resistance to the primary at the switching frequency [14]. We performed three kinds of coupling factor measurements: impedance measurements from the primary with a resonant secondary AC load [15], open-short measurements, and coupling estimation with a frequency sweep, as explained in [14], [16]. For the case of the resonant secondary coupling measurement method, we used two different values of resistance.

A photo of the final coil configuration is shown in Fig. 1c, where the distance is $11\,\text{cm}$ and the reflected resistance at the switching frequency is around $8\,\Omega$ with a $42\,\Omega$ AC secondary load. These measurements correspond to a coupling factor in the range of $20\,\%$ to $30\,\%$ which is too low to be estimated accurately with the open-short method and too high for the AC resonant load method [15], leaving the frequency sweep method [14], [16] as the preferred estimation approach.

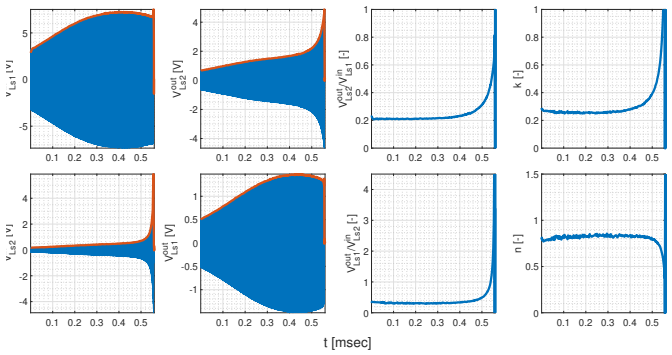


Fig. 3: Frequency sweep measurement results for the IPT link in Fig. 1c. In the first two columns the wavefomrs are in blue and the envelopes of the waveforms are in orange. The curves in the last two columns are derived using the envelope data of the first two. The final values of the coupling factor and transformer ratio are derived from the flat part of the respective curves.

The results of the frequency sweep measurements for coupling factor estimation are shown in Fig. 3. The signal source is the $50\,\text{MHz}$ Aim-TTi function generator and the voltage measurements across the coils are performed using the optical probes from Tektronix, to minimise the capacitive loading on the coils, although this measurement method inherently absorbs the effect of the coil capacitance. The range of the frequency sweep is from $100\,\text{kHz}$ to the resonant frequency of the coils. The voltage measurements are performed by stimulating first the primary and then the secondary, while measuring both sides of the IPT link. The coupling factor k and the transformer ratio n are given by

$$k = \sqrt{\frac{V^{\text{out}}_{L_{s_1}} V^{\text{out}}_{L_{s_2}}}{V^{\text{in}}_{L_{s_1}} V^{\text{in}}_{L_{s_2}}}}, \tag{1}$$

$$n \equiv \sqrt{\frac{L_{s_2}}{L_{s_1}}} = \sqrt{\frac{V^{\text{in}}_{L_{s_2}} V^{\text{out}}_{L_{s_2}}}{V^{\text{in}}_{L_{s_1}} V^{\text{out}}_{L_{s_1}}}}. \tag{2}$$

The transformer ratio value matches the individual impedance measurements of the two coils, which is a confirmation of valid results. The exact estimation value of the coupling factor using the frequency sweep method is $24.5\,\%$. The open-short method gave an underestimation of the coupling factor, and the two measurements with the resonant Rx loads gave an overestimation, with significant deviation between the two instances, which is an indicator of unreliable estimations for these two measurement methods in our example.

III. Full-bridge Class DE Rectifier Design

Once the IPT link has been established and well characterised we then design the HF rectifier. We choose the current driven Class DE rectifier topology, for the high power capability, resonant operation with soft switching, absorption of the non-linearities of the diode capacitances, and lack of inductors [1], [17]–[19]. Also, the current driven topologies are in general preferred for IPT applications, since they are series tuned and changes in the equivalent AC load of the rectifier

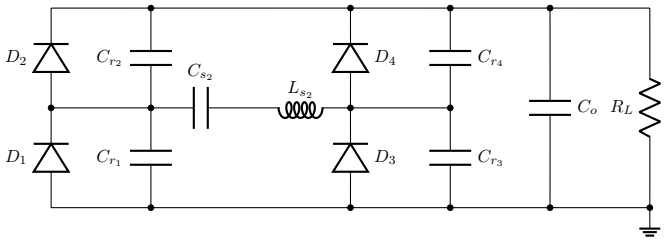


Fig. 4: Circuit diagrams of the full-wave current driven Class DE rectifier for IPT applications.

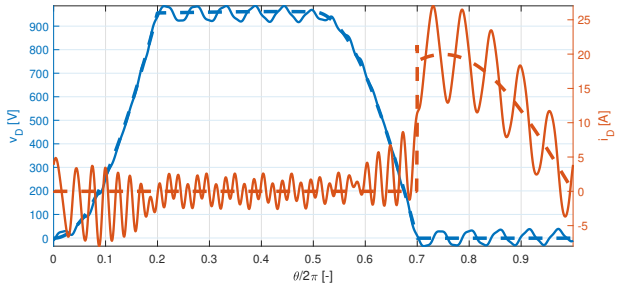
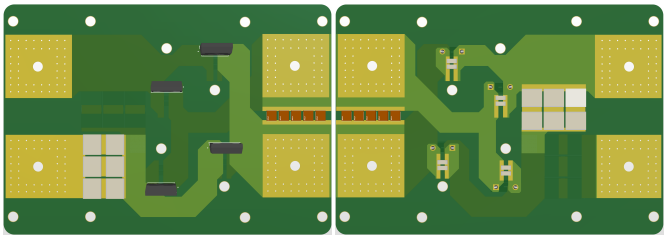


Fig. 5: Voltage and current on the diodes of the current driven full-bridge Class DE at example 8 kW operation. The dashed line represents the ideal diode waveforms and the solid line is for the waveforms of the C4D20120H SiC Schottky diode. The ringing is caused by the resonance of stray inductance of the TO-247-2 package with the parasitic capacitance of the diode.

do not affect the equivalent reactance [20]. The objectives are 8 kW peak power using the C4D20120H SiC Schottky diodes with a full-bridge configuration equivalent to a 40 Ω AC load.

The component values are determined by the design process of half-bridge version with half the equivalent AC resistance and 30 % duty cycle, in order to remain within the voltage and current limits of the diodes. The full-bridge equivalent version has the same shunt capacitances but half the DC load of the half-bridge. The voltage and current waveforms for both versions are the same, as long as the the DC load is transformed accordingly. The full-bridge Class DE rectifier circuit diagram is shown in Fig. 4. Then we replace the ideal diodes in the simulation with the real diode model, and reduce the value of the shunt capacitors until the current and voltage waveforms match, as displayed in Fig. 5. In our example it is 70 % of the ideal case, and it practically does not affect the equivalent reactance of the rectifier, since the Class DE topology inherently absorbs the non-linearities of the parasitic capacitance of the diodes.

The top and bottom view of the rectifier PCB are shown in Fig. 6. The exact values of the NP0 shunt capacitors and the DC resistance are measured, and the ideal components in the LTspice simulation are replaced accordingly. The first order equivalent input impedance of a resonant current driven rectifier is a capacitance C_r in series with a resistance R_r. The exact value of the equivalent impedance of the rectifier is calculated by driving it with an AC input current source at the nominal amplitude and deriving the first harmonic of the voltage across it. Then, the series resonant capacitor can be



(a) Top view (b) Bottom view

Fig. 6: PCB of the full bridge current driven Class DE circuit. The parallel impedance transformation capacitor is left unpopulated in the experimental setup.

computed using the relation

$$C_{s_2} = \frac{C_r}{\omega_S^2 L_{s_2} C_r - 1}. \tag{3}$$

Once the Rx side is fully defined, the next objective is to calculate the reflected resistance to the primary, while minimising the reflected reactance. A close initial approximation of the amplitude of the primary coil current is given by

$$I_{L_{s_1}} = \frac{I_{L_{s_2}} (R_{s_2} + R_r)}{\omega_S k \sqrt{L_{s_1} L_{s_2}}}, \tag{4}$$

where $I_{L_{s_{1/2}}}$ is the peak current on the corresponding coil, R_{s_2} is the intrinsic resistance of the Rx coil, and ω_S is the Tx angular switching frequency.

Then, we simulate the complete secondary coupled to the Tx coil, driven by the current from (4). If needed, we fine tune the primary current amplitude to achieve the required output power, and the series secondary capacitance to minimise the reflected reactance to the primary. Specifically, in our example the primary current was increased by 3 % an the secondary resonant capacitor was increased by 2 %. Now, the value of the reflected resistance can be approximated by the real part of the first harmonic of the voltage across the Tx coil divided by the primary current.

IV. Parallel Push-pull Class E Inverter Design

Now that the objectives for the primary driver are determined, we proceed with the design of the inverter. We introduce the parallel push-pull Class E inverter topology, because the lack of ϕ-branch provides superior efficiency at high power over the Class EF topology, with 50 % duty cycle for maximum power capability [21] and 7 kW nominal power output. The design procedure is based on the method proposed in [22], adjusted to the simpler Class E configuration, combined with the impedance transformation required for the parallel push-pull (PP) connection.

A visual example of such parallel push-pull configuration based on two Class E inverters (but can be any kind of resonant topology) driving a single Tx coil is shown in Fig. 7. There are four discrete points of connection in this topology: A, B, C, and GND. The common power supply is connected between points A and GND, and the primary coil is connected between

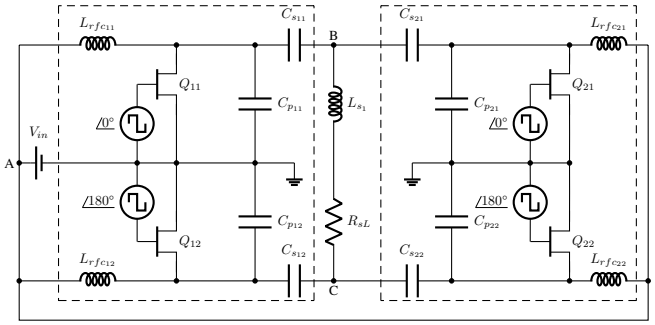
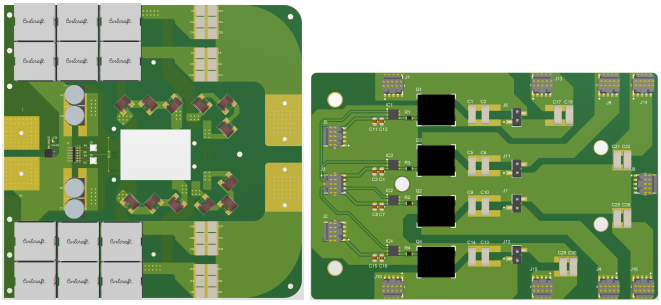


Fig. 7: Parallel connection of two push-pull Class E inverters on a common loaded primary coil, supplied by a common voltage source, to form a parallel push-pull configuration.



(a) FR4 inverter mother board (b) IMS inverter daughter board

Fig. 8: PCBs comprising the parallel push-pull Class E inverter. The boards are capable of providing both Class E and Class EF configurations. The daughter board is connected to the bottom of the mother board under the cutout.

points B and C. The input of each PP inverter is connected to point A and the outputs are connected to B and C. It is important that each of the points B and C is only connected to the same phase branch of the PP part. As already known, the PP topology has twice the power output of the equivalent single-ended (SE) one. In turn, the parallel PP topology of Fig. 7 has twice the power capability of a single PP stage, i.e. quadruple the power of a SE inverter. Of course, this kind of configuration in not limited to only to PP stages as shown in Figure 7.

The design method for a parallel push-pull topology is similar to the simple PP case, with some key modifications. For a given primary coil loaded impedance $\overline{Z}_{sL}$ and output power P_o of each SE stage, the corresponding PP configuration has $2\overline{Z}_{sL}$ loaded primary coil impedance and $2P_o$ total output power. In turn, a parallel PP configuration of N stages using the above SE design has a loaded output impedance of $2\overline{Z}_{sL}/N$ and total output power $2NP_o$. The rest of the inverter components, including the input voltage remain unchanged from the SE stage. An interesting observation for the special case when $N = 2$, as in Fig. 7, is that both for the discrete SE inverters as well as for the whole parallel PP system, the output impedance is equal, which simplifies the design process, as well as the dynamic analysis of the inverter behaviour under varying load.

The PCB's of the inverter are shown in Fig. 8. It consists of two individual boards: an insulated metal substrate (IMS)

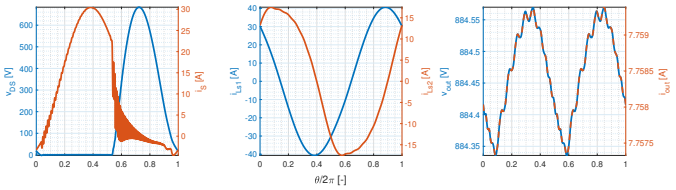


Fig. 9: Waveforms of the transistor drain voltage and current (left), currents through the coils (middle), and output load power (right). The Rx coil has distortion from the third harmonic, which is an artifact of the Class DE rectification.

TABLE I: Component values of the high power IPT system

Parameter	Value	Unit
$V_{in}^{\max}$	180	V
L_{rfc}	100	µH
f_S	3.39	MHz
D	48.5	%
R_g	0	Ω
G	UCC27512	–
V_{dd}	6	V
Q	GS66516B	–
C_p	678	pF
C_{s_1}	611	pF
L_{s_1}	4.17	µH
k	24.5	%
L_{s_2}	3.14	µH
C_{s_2}	1.916	nF
D	C4D20120H	–
C_r	236	pF
C_o	2.24	µF
R_L	114	Ω

daughter PCB with the Ventec VT-4B7 SP material containing the switching network for improved thermal performance, and a FR4 motherboard with the rest of the components. The transistors are the GS66516B from GaN Systems and the gate drivers are the UCC27512 from TI. Some indicative waveforms from the simulation of the full IPT system at nominal power are given in Fig. 9.

V. Experimental Results

Both the inverter and the rectifier use 7.2 kV 3838 NP0 ceramic capacitor from Kyocera AVX for resonance with the coils, and the shunt capacitors are 2 kV 2225 NPO from TDK. The input chokes are the AGP4233-333ME from Coilcraft, and the output stabilising capacitors of the rectifier are 1.5 kV X7R ceramics. The input stabilising capacitors comprise of a combination of electrolytic and ceramic, both X7R and NP0. The signal generating circuit is the same as the one used in the experimental examples in [22]. The exact measured component values are given in Table I and a photo of the complete IPT system is shown in Fig. 10.

The waveforms of the experimental setup in Fig. 10 are given in Fig. 11. The gate signals are measured with 50 Ω coaxial cables, the secondary coil current is measured with the Pearson 6585 current monitor, the primary coil current is measured with the N7041A Rogowski probe from Keysight,

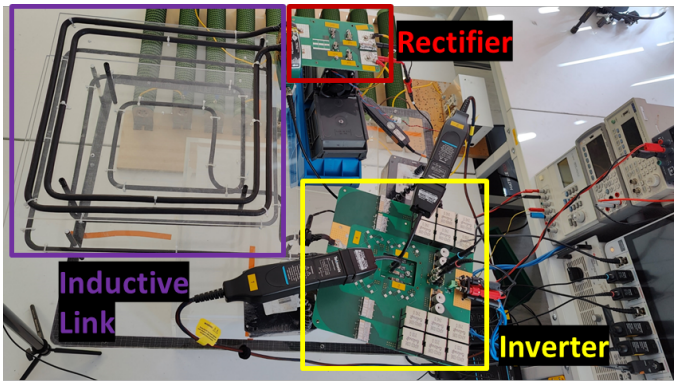


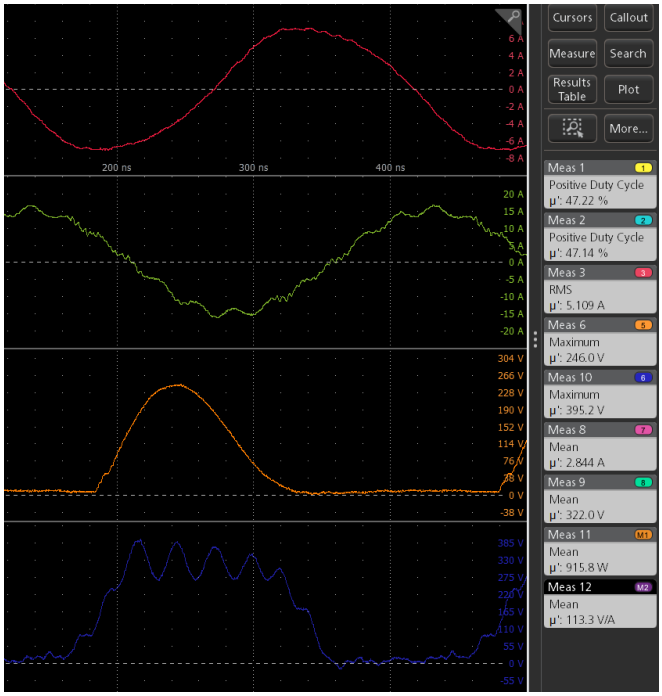
Fig. 10: Photo of the complete high power IPT experimental setup.

the drain voltage is measured with the TVIH08 isolated probe and WSQPIN1000X tip from Tektronix, the voltage across the diode is measured with the N2891A differential probe from Keysight, the output voltage is measured with a high voltage passive PMK probe, and the output current is measured with the N2893A current clamp from Keysight.

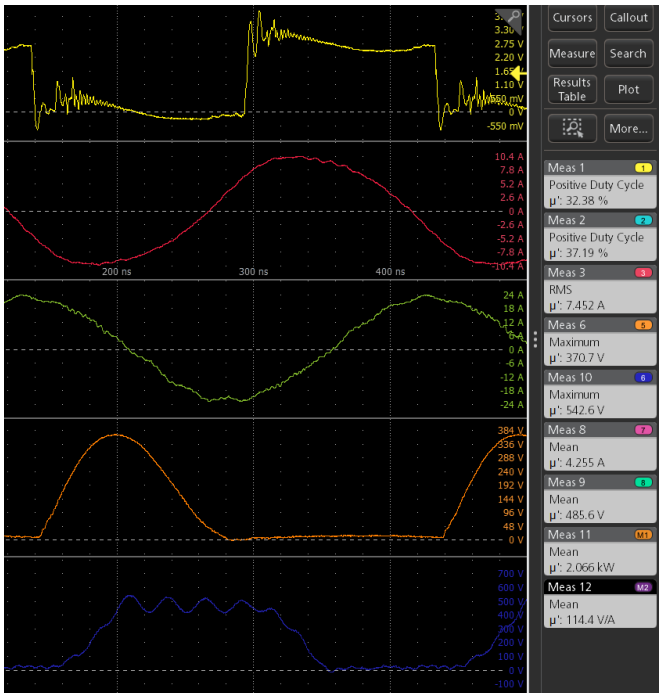
The rectifier measurements match the simulations, but the inverter is reverse conducting more than expected, due to the large, non-predictable parasitic capacitance of the IMS board. At 69 V input voltage the inverter is soft switching with both zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS), and the output power is 916 W. At 102 V input voltage the inverter is reverse conducting and the load is consuming over 2 kW power at over 91 % DC/DC efficiency. The highest output power achieved was around 3 kW at 95 % efficiency. Throughout the testing of the system the devices remained below 40 °C and the coils were around 30 °C at maximum power.

Several issues that limited the performance of the system had to be addressed. First, the 1.5 kV X7R capacitors at the output are not suitable for such application, since their temperature was increasing unexpectedly high. The reason lies in the voltage dependent behaviour of their capacitance as well as well as the lower SRF compared to NP0. This problem was easily resolved by adding extra NP0 ceramic capacitors to the output. Next, the metal substrate of the IMS board should not be left floated, but instead should be connected to ground. This intervention would make the parasitic capacitance of the IMS board more controllable and provide a return path through an uninterrupted plane to the signals. The cross-talk noise on the gate signal, which is caused by caused by the supply of the gate and the drain node current, was significantly decreased by grounding the metal substrate.

In addition, the mother board has unnecessarily large traces, which introduce parasitic inductances. Also, the transistors should be connected in a star configuration with a common solid ground plane, to minimise interference from the return path of the drain node. Finally, the gate signal traces should be shielded and kept as short as possible, to minimise coupling with the strong fields present on the power board.



(a) $V_{in} = 69\,\mathrm{V}$



(b) $V_{in} = 102\,\mathrm{V}$

Fig. 11: Measured waveforms of the IPT system in Figure 10 at two supply voltage values. The gate signal to one of the two pairs of gate drivers is yellow, the Rx coil current is red, the Tx coil current is green, the drain voltage is orange, the voltage across one of the diodes is blue. The first two measurements are the duty cycles of the gate signals, the third measurement is the RMS value of the Rx coil, "Meas 6", is the peak of the drain voltage, "Meas 10" is the peak of the voltage across the diode, "Meas 8" and "Meas 9" are the DC output current and voltage, respectively, "Meas 11" is the output power, and "Meas 12" is the DC load. The ripple of the L_{s_1} current is noise from the Rogowski probe.

VI. Summary

HF operation in IPT systems reduces the weight and size of the magnetic link, which in turn reduces cost, and increases the potential transfer distance. This paper showcases the advantages of using a HF IPT system where improved tolerance to misalignment, lightweight potential and lower cost can encourage its uptake in high power applications. The hierarchy of the design process is provided in detail, starting from defining and measuring the IPT link, then tuning a suitable rectifier and finally choosing a corresponding inverter. A novel inverter configuration is proposed to increase the power output of traditional Class E type topologies within the drain voltage limitations of GaN transistors. The experimental demo using a parallel PP Class E inverter achieved $95\,\%$ peak efficiency at $3\,\mathrm{kW}$ output, operating at $3.39\,\mathrm{MHz}$. Several practical issues that require attention have been mentioned regarding the optimal operation of the experimental setup.

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