A New Hybrid Multi-Level Voltage-Source Converter with DC Fault Blocking Capability

M.M.C. Merlin*, T.C. Green*, P.D. Mitcheson*, D.R. Trainer†, D.R. Critchley†, R.W. Crookes†

*Imperial College London, UK, {michael.merlin07, t.green, paul.mitcheson}@ic.ac.uk
†Alstom Grid, UK, david.trainer@areva-td.com

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Abstract

Voltage-Source Converters have brought numerous advantages to HVDC transmission. However, they suffer from high losses and are usually weak against faults on the DC-side. In this paper, a new topology which brings together some concepts from traditional Current Source Converters and multi-level converters, is presented. Two stacks of H-bridge cells alternate to construct the converter voltage using director switches made of IGBTs in series. The resulting converter generates AC current with low harmonic content and with low loss. Furthermore, the converter is still very responsive in case of a fault. This paper first explains the composition and the working of this converter, then detailed simulations at 20 MW illustrate the performances and low losses of this converter under normal conditions. The ability of this topology to deal with abnormal conditions is also demonstrated, especially its ability to keep control of the current despite the collapse of the DC bus voltage, e.g. a DC-side fault.

1 Introduction

HVDC plays an important role in schemes which involve undersea cables or unsynchronised networks. Renewable sources are good application cases for this technology, for example wind farms, due to their off-shore location and unsynchronised operation. The more recent class of converter, Voltage Source converter (VSC) [3,5], has several advantages over the Current Source Converter (CSC), such as relying on constant DC voltage and independent active and reactive power conversion. However, the first VSC topologies had a limited number of levels for the converter voltage waveform construction, partly due to capacitor balancing difficulties and the large number of devices required. The drawbacks were thus large harmonic content in the generated AC current and high losses due to the requirement to use an IGBT rather than a thyristor (as would be used in a CSC) together with the use of PWM techniques.

A new generation of converter [2,4] using H-bridge cells has started to emerge as an interesting evolution for VSCs. Known as the Modular Multi-level Converter (M2C), this topology can contain a large number of cells, e.g. 200 cells, and can thus generate low distortion AC current and may not need AC filters. Furthermore, in case of a DC fault, the cells can still produce enough voltage to control the inductor current. However, this configuration results in even higher losses because of the large number of conducting devices. Losses can be reduced using half-bridge cells instead of full H-bridge cells, thus halving the number of conducting IGBTs. However, this also removes the ability of the converter to block a DC fault which was an advantage over the first generation of VSC.

2 Schematic and Principles

2.1 Presentation

Given the summary of the existing converters presented above, this paper proposes a new topology which aims to lower the losses and maintain the ability to deal with DC-side faults. This topology, briefly presented in [8], is based on multi-level converters, since it uses stacks of H-bridge cells to construct the converter voltage from the DC-bus voltage, and is similar to a CSC because a string of IGBTs, called a director switch, is inserted in each arm to direct the current either to the upper or lower arm. A general representation of this topology is presented in Figure 1. Because of its alternate use of the two arms of each phase, this topology could be called Alternate-Arm Multi-level Converter (A2MC).

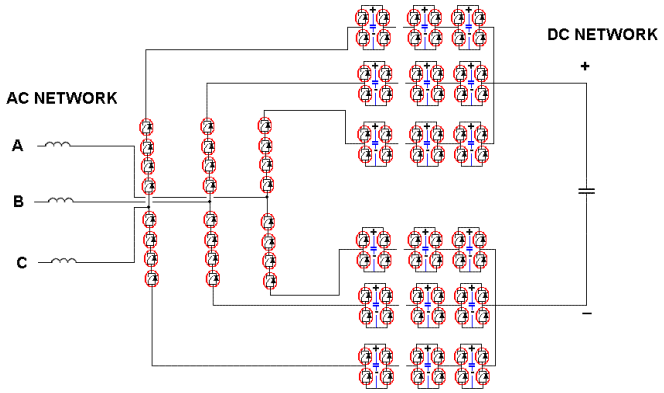

Figure 1: Schematic of the proposed Alternate-Arm Multi-level Converter

Each phase consists of two arms which conduct alternatively, as illustrated in Figure 2. Each arm is composed of a stack of H-bridge cells (4 IGBTs and 1 charged capacitor) and a director switch made of series IGBTs. When conducting, i.e.,

when the director switch is closed, an arm uses its cells to construct the converter voltage by adding or subtracting several small voltage contributions to the DC-bus voltage. The AC phase current passes to either the positive or negative DC terminal and, together with the two other phase currents, create a DC current with a 6-pulse ripple.

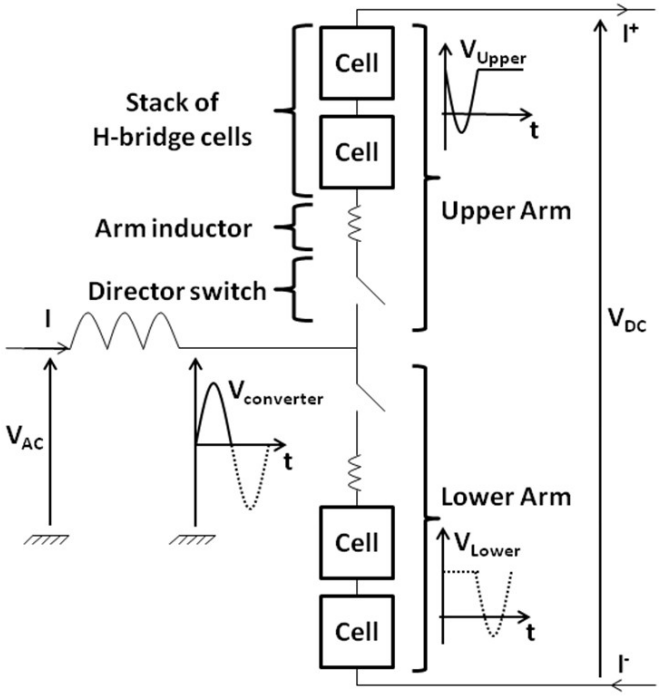

Figure 2: Representation of a single phase converter

Because an objective of this topology is to minimize the losses, the working cycle of the arms is synchronised with the converter voltage. This means that the positive half-cycle of the converter sine wave is constructed by the upper arm while the lower arm constructs the negative half-cycle, as represented in Figure 2. Therefore, the minimum number of H-bridge cells is only half the number of the M2C requirement. Furthermore, the non-conducting arm can be used to minimize the voltage of its open director switch but still keep it positive to avoid conduction of the anti-parallel diodes. This reduces the number of series IGBTs to block the maximum required voltage. Interestingly, the cells can be actively used during the cross-over between the two arms to drive the current of the previously working arm to zero. This reduces the stress on the director switches since soft-switching (zero current and zero voltage switching) is achieved. All these features contribute to the reduction of the losses in this topology.

2.2 Energy Balance

In this topology, the AC current is directed alternatively through the different stacks of cells and thus through the cell capacitors. As a consequence, the converter should be operated such that the amount of energy converted from the AC side equals the amount of energy going to the DC side over half the fundamental period. This condition ensures that the voltage of the capacitors in the cells will come back periodically to their nominal value; otherwise their voltage will diverge and threaten the operation of the converter. By matching the equations, shown below, of the transferred energies from the AC side (1) and from the DC side (2), a condition to achieve the equilibrium, as described above, can be drawn on the AC and DC voltage magnitudes (3).

$$E_{AC} = \frac{3}{2}\frac{\hat{V}_{AC} \times \hat{I}_{AC}}{\omega_0} \times \pi \times \cos(\Phi_I) \quad (1)$$

$$E_{DC} = 3 \times \frac{V_{DC} \times \hat{I}_{AC}}{\omega_0} \times \cos(\Phi_I) \quad (2)$$

$$V_{DC_{opt}} = \frac{\pi}{2}\hat{V}_{AC} = \frac{\pi}{\sqrt{6}} V_{Line-to-Line} \quad (3)$$

This relationship between the AC and DC voltages has some consequences in the design of the converter. One of them is the fact that the peak AC voltage is higher than half the DC bus voltage (27%). This implies that the converter has to use the cells in the reversed direction which is possible since the cells are full H-bridge cells and enough cells are present to produce this additional voltage. Moreover, it has also an impact on the voltage rating of the director switches since they have to support higher voltages.

Since it is unlikely the converter always operates in this condition, energy balancing techniques must be used. So far, two techniques have been identified to achieve energy balance: overlap current and third harmonic current. The former takes advantage of the moment when the current is directed from one arm to the other. By extending this period, a current path through both arms connects to the DC side. Using the small arm inductors, a controlled DC current can be used to charge (or discharge) the cell capacitors by exchanging power with the DC bus. The latter consists of generating a third harmonic in the AC current which by its nature does not go through the grid transformer but still exchange power between the stack of cells and the DC bus. This technique has not been fully investigated but should have the advantage of balancing the energy slowly over time instead of in bulk every half cycle. Furthermore, in addition to its balancing effect, the third harmonic may smooth the 6-pulse ripple of the DC current.

Finally, one of the biggest advantages of this topology lies in its capacity to deal with DC side fault. Indeed, in the case of a large DC bus voltage drop, the stacks of cells are still operational and, because the cells are full H-bridges , they can produce negative as well as positive voltages. Therefore, if enough cells are present in the stack, the converter is still able to oppose the grid voltage, thus driving the current of the inductor down to zero before it reaches dangerous levels. This topology can be used as a STATCOM system when the DC grid is not available (DC fault or service requirement) since it contains a stack of H-bridges similar to the STATCOM system from GEC Alsthom [1]. In this mode, either one arm or both arms of each phase converter can be used to produce reactive power, depending on the strategy chosen.

3 Simulation

3.1 Simulation Model and Control Structure

A simulation model has been constructed to verify the operation of this new topology under normal and fault conditions. This model has the following characteristics:

- 20 MW converter with ±6.6 MVAr capability
- 11 kV line-to-line grid voltage
- 20 kV DC bus voltage
- Transformer with a 11:16 voltage ratio
- 4 mF capacitor charged at 1.5 kV in each cell
- 9 cells per arm
- 8 IGBTs in series per director switch

The ratio of the transformer was chosen such that the magnitude of the resulting AC voltage connected to the converter corresponds to the optimal voltage, as established in Equation (3). Then, the number of cells was chosen in order to give to the converter the ability to cope with DC side faults. The number of series IGBT in the director switches is chosen in accordance to a steady state average voltage stress of 1.5kV to accommodate the use of a 3.3kV IGBT.

Next, a control system was designed to manage this model and is composed of three different layers, as illustrated in Figure 3. The top level control sets the AC current in the converter inductor. This task is achieved using a P+R compensator [7] which compares the difference between the measured current and the desired reference current in the time domain. The magnitude and phase angle of this reference current is preset at the beginning of the simulation using active and reactive power demands. Given this information, the P+R compensator computes the required converter voltage to control the inductor current. The choice of the P+R technique over more conventional techniques [6] has been motivated by its single-phase control structure which proves to be useful in case of imbalanced 3-phase AC networks, e.g., a 1-phase fault.

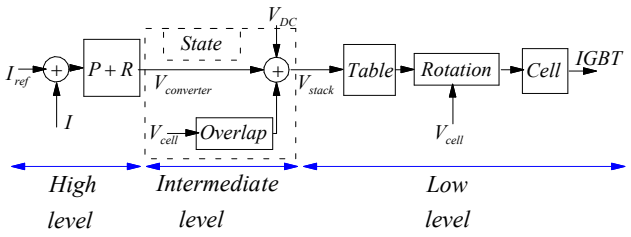

Figure 3: Structure of the control system

The intermediate level controller deals with the management of the stack of cells and the director switches. Using the converter voltage command, this controller activates the correct arm, computes the voltage command of each stack of cells and controls their level of charge via the modification of the overlap current magnitude. The low level controller is responsible for the cells and the associated IGBTs. This controller converts the stack voltage command into cell activation commands, i.e. positive, negative or zero contribution. Second, in order to keep the cells charged homogeneously, a rotation algorithm swaps the cell duties, thus sharing the load across the different cells. The main effect this algorithm has on the capacitors is that the voltage deviation is minimized and cell voltages are kept close to their nominal value. Finally, the cell commands are translated into IGBT firing commands which are sent to the devices.

3.2 Normal Operation

The test in normal operation aims to verify the ability of the converter to export / import power to / from the AC system with low harmonic content. As illustrated in Figure 4, the generated AC current is good quality and FFT analysis of this current in Figure 5 shows despite the fact this current still contains several harmonics, their magnitudes are kept small (THD < 1.6%).

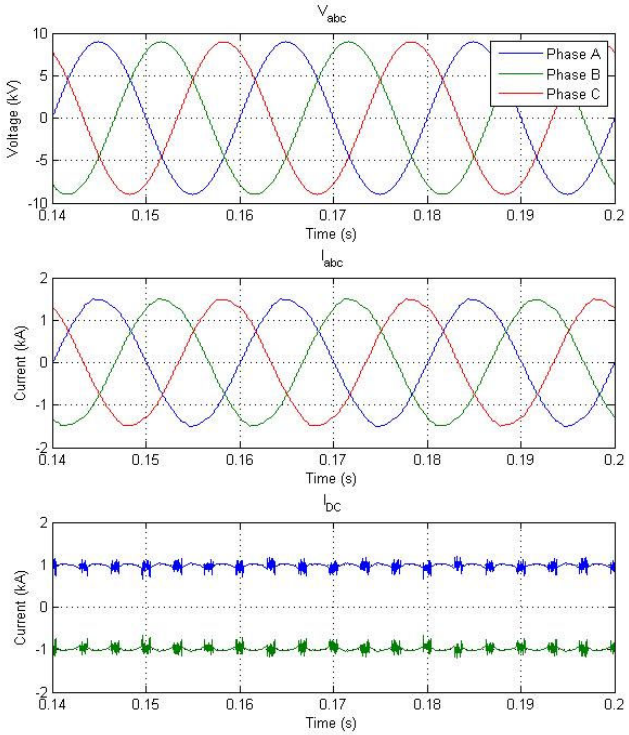

Figure 4: Voltage and current waveforms under normal operation at 20 MW (rectification mode) with a P.F. = 1. Phase voltages (top), phase current (middle) and unfiltered DC link current (bottom).

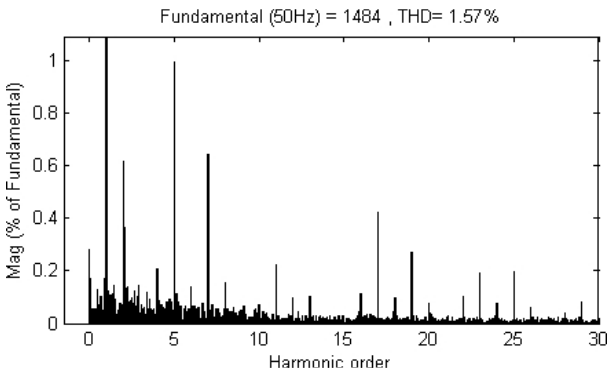

Figure 5: FFT analysis of the generated AC current

The DC current flowing from the converter without any filtering consists of 3 components, as shown in Figure 4 (bottom). They are the non-zero average current (about 1 kA), the 6-pulse ripple (about 200 A) and the additional balancing current (a few hundred Amps). The overlap current aims to re-balance the cell capacitors every half cycle, thus in a 3-phase converter it flows every 6.67 ms. The visible shuttering of the overall current is due to the small size of the arm inductor and its control by switching cells on top of the converter voltage command.

The voltage of the different cell capacitors is kept close to nominal, as illustrated in Figure 6. The voltage pattern shows that an arm is only working every half cycle and the energy stored in a stack goes back to its nominal value thanks to both the voltage equilibrium and the additional balancing DC current. The rate of change of capacitor voltages is determined by the value of the capacitors. Therefore, lowering their values will increase the overall voltage deviation accordingly which could lead to more distortion to the generated AC current.

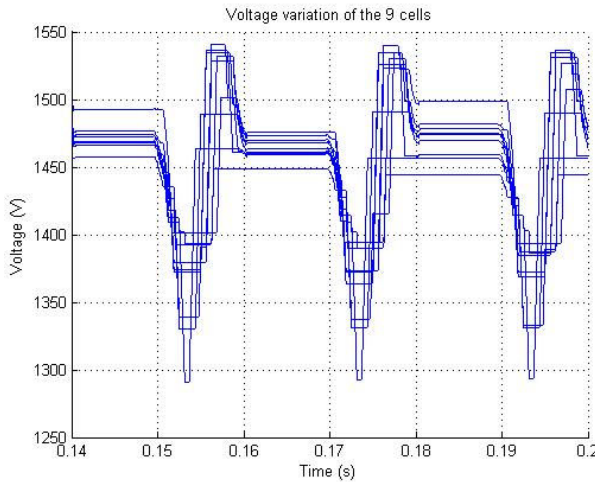

Figure 6: Voltages of the 9 capacitors in one arm

Finally, the losses in the system have been determined by post-processing the time domain simulations to assess the overall efficiency, based on the MG1200FXF1US53 module from Toshiba. A summary of this study is presented in Table 1. This topology is able to achieve almost 99% overall efficiency using a multi-level approach without involving PWM techniques and thus shows great potential for future DC VSC schemes.

Category	*Power [kW]*
Cell Losses	**168.58**
Conduction Loss	98.21
Switching Loss	49.80
Reverse Recovery Loss	20.57
Director switches Losses	**34.64**
Total Losses	**203.22**
Efficiency (%)	**98.98**

Table 1: Semiconductor losses and efficiency of the converter in the 20 MW simulation case.

3.3 Abnormal Operation

Having verified normal operation of the converter, the model was tested under abnormal operation. In the previous simulations, cell energy balancing was achieved almost entirely thanks to the relationship between the AC and DC voltage magnitudes. However, as the operation condition moves away from these equilibrium values, the balancing current will increase, until it reaches the maximum current rating of the devices. This model has been tested successfully down to 0.8 p.u. retained AC voltage, but then specific corrective actions have to be taken, for example a reduction in the AC current reference.

Three different faults are presented in this paper: a 3-phase fault, a 1-phase fault and a DC fault. The fault scenario was set up such that the AC voltage drops from 1.0 p.u. to 0.3 p.u. between 20 ms and 200 ms and then goes back to its nominal voltage. During the fault period, the reference AC current which is provided to the P+R controller is replaced after a detection delay of 10 ms. With this change, the converter moves from full active power conversion (20 MW rectification and 6.6 MVAr leading during normal operation) to only reactive power mode (0 MW and 6.6 MVAr leading during abnormal operation). This scenario has been chosen in order to show the ability of the converter to continue operation and support for the grid by providing reactive power. After the fault is cleared, the converter goes through a power ramp over 100 ms to avoid further sudden changes.

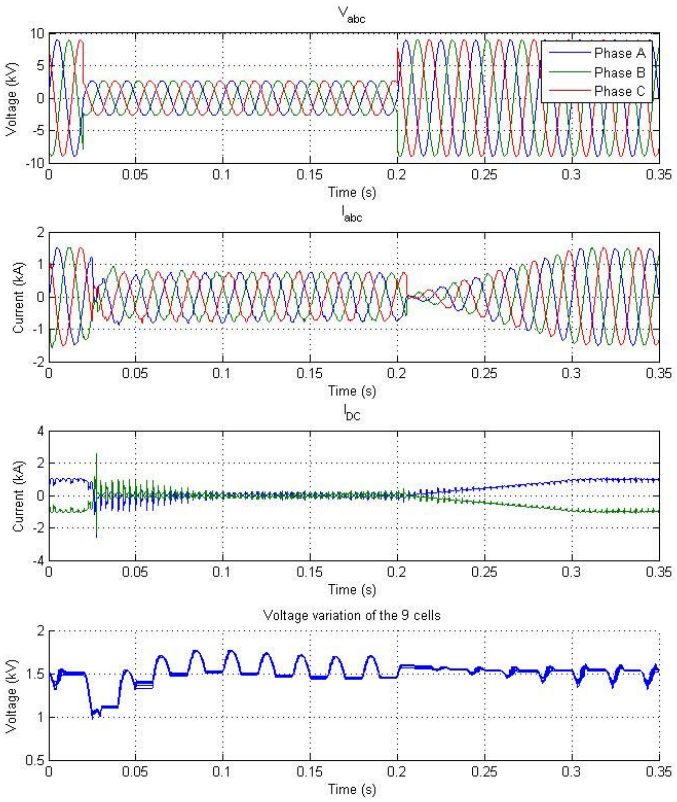

Figure 7: Simulation of a 3-phase fault (0.3 p.u. retained voltage and 5 ms detection delay)

Figures 7 and 8 show respectively the results for a 3-phase fault and a 1-phase fault (phase A) simulations. It can be seen that the converter responds quickly (few ms) to a change in its current reference and is still able to continue operating despite the severe disruption.

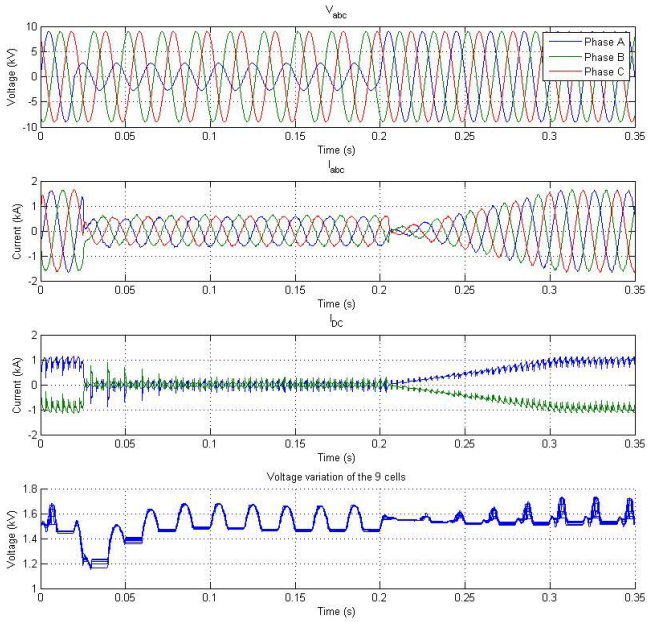

Figure 8: Simulation of a single phase fault (0.3 p.u. retained voltage and 5 ms detection delay).

In the DC fault simulations (Figure 9), the parameters are the same as the AC fault simulations apart from the fact that only the DC bus voltage is affected. Between 20 ms and 200 ms, this voltage drops to 0 p.u. and then comes back to nominal value. During the fault, the converter does not lose the control of the current and behaves successfully as a STATCOM

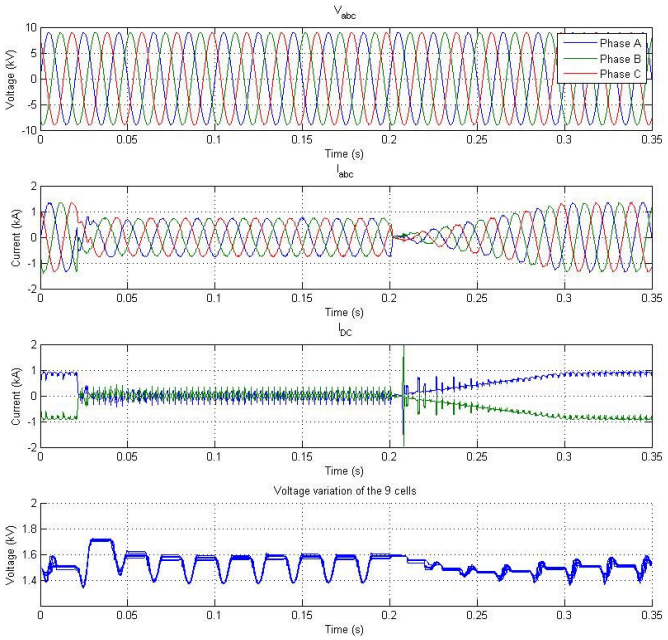

Figure 9: Simulation of a DC Fault showing STATCOM operation during the fault (between 20 ms and 200 ms).

4 Conclusion

The Alternate-Arm Multilevel Converter (A2MC) appears to be a promising topology for VSC applications. Its composition and operation have been explained. Simulations have demonstrated good performance of this converter which combines the advantage of half-bridge multi-level converters (low distortion and low losses) and of full H-bridge converter (DC-side fault blocking).
Furthermore, the simulations have also demonstrated the capability of this converter to provide reactive power during severe abnormal operation, even during a DC-side fault. This last feature may bring additional advantage to VSC topologies since they can offer support to the AC grid during a fault.

Acknowledgements

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References

[1] J. D. Ainsworth, M. Davies, P. J. Fitz, K. E. Owen, and D. R. Trainer, "Static VAR compensator (STATCOM) based on single-phase chain circuit converters" *Proceeding Institute Electrical Engineer - Generation Transmission Distribution*, **145(4)**, pp. 381-386, (1998).

[2] S. Allebrod, R. Hamerski, R. Marquardt. "New transformerless, scalable modular multilevel converters for hvdc-transmission", *Power Electronics Specialists Conference*, pp. 174-179, (2008).

[3] B.R. Andersen, L. Xu, P.J. Horton, P. Cartwright. "Topologies for VSC transmission", *Power Engineering Journal*, **16(3)**, pp. 142-150, (2002).

[4] J Dorn, H Huang, and D Retzmann. "Novel voltage-sourced converters for hvdc and facts applications", *Conference proceeding CIGRE - Osaka*, **314**, (2007).

[5] R Jose, L Jih-Sheng, and P Fangzheng. "Multilevel inverters: A survey of topologies, controls, and applications", **49(4)**, *IEEE Transactions on Industrial Electronics*, pp. 724-738, (2002).

[6] B. Singh and J. Solanki. "A comparison of control algorithms for DSTATCOM", *Industrial electronics, IEEE transactions on*, **56(7)**, pp. 2738-2735, (2009).

[7] R. Teodorescu, F. Blaabjerg, M. Liserre, and P.C. Loh. "Proportional-resonant controllers and filters for grid-connected voltage-source converters", *Electric Power Applications, IEE Proceedings*, **153(5)**, pp. 750-762, (2006).

[8] D.R. Trainer, C.C. Davidson, C.D.M. Oates, N.M. Macleod, D.R. Critchley, R.W. Crookes "A new Hybrid Voltage-Sourced Converter for HVDC Power Transmission", *CIGRE Session 2010*, (2010).