Symbolic Framework for Linear Active Circuits Based on Port Equivalence Using Limit Variables

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Abstract—This paper proposes a new framework for linear active circuits that can encompass both circuit analysis and synthesis. The framework is based on a definition of port equivalence for admittance matrices. This is extended to cover circuits with ideal active elements through the introduction of a special type of limit-variable called the infinity-variable (∞-variable). A theorem is developed for matrices containing ∞-variables that may be utilized in both circuit analysis and synthesis. The notation developed in this framework can describe nonideal elements as well as ideal elements and therefore the framework encompasses systematic circuit modeling.

Index Terms—Active circuit analysis, active circuit synthesis, active circuits, circuit modeling, admittance matrix, nullor.

I. INTRODUCTION

ONE of the difficulties in the field of linear active circuits has been the lack of general mathematical techniques to underpin the analysis and synthesis of practical designs. The critical factor that prevents this possibility is the nonexistence of a simple basis for which the descriptions of active circuit elements and the corresponding circuit functions exist. The purpose of this paper is to show how an admittance description can fulfill this requirement, providing that certain limiting cases are allowed. This is made possible through the concept of port-equivalence and a novel notation based on limit-variables.

Co-ordinate-free descriptions for nondegenerate linear active circuits already exist, since it is recognized [1] that the behaviour of such a circuit corresponds to an n dimensional subspace of the $2n$ dimensional vector space spanned by the n voltage and n current unit vectors. Linear active circuits may thus be characterized as points in a Grassmannian [2]. Intrinsically nonsingular co-ordinate systems exist in formalisms due to Belevitch [1], $[\mathbf{A} \,|\, \mathbf{B}][\mathbf{V} \,|\, \mathbf{I}]' = [0]$, and Youla [3], $[\mathbf{V} \,|\, \mathbf{I}]' = [\mathbf{Q}][\mathbf{x}]$. These elegant approaches have been used to prove important results in circuit theory. However, they do suffer from a lack of economy in that the number of coordinates is greater than the dimensionality of the space and the nonuniqueness of the equations means that they have to be normalized to yield canonical forms. Hence, these descriptions for circuits have not been widely accepted for use in design and synthesis of active circuits.

The admittance basis for describing circuits, where the node voltages are independent variables and the node currents are

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dependent variables, is potentially an attractive candidate for a general framework [4]. In order that a framework can accommodate circuit synthesis, it must be able to describe ideal circuit elements, because synthesis using nonideal elements is usually intractable. However, the admittance matrix representation suffers from the problem that key ideal circuit elements, including the nullor, which can represent the ideal transistor and op-amp, most dependent sources, and the impedance converter, require infinite matrix elements. This problem has been overcome by the modified nodal approach (MNA) in which additional columns and rows are incorporated into the standard admittance matrix [4], [5]. As a consequence, the MNA has become the industry standard for both numerical and symbolic circuit analysis. Another approach is to associate a series combination of a positive resistor R and a negative resistor $-R$ with each problem element and then convert the combination of the problem element and one of the resistors into an acceptable form using source transformations [6]. For the MNA and $\pm R$ approaches, the dimensions of the matrix and the basis for the representation are dependent on the type of elements contained in the circuit. This does not greatly obstruct circuit analysis where the circuit elements are known in advance and the matrix dimensions and basis can be set up accordingly. However, this is a problem for circuit synthesis where the types of elements needed in the circuit are not known *a priori*. For a coordinate framework encompassing both circuit analysis and synthesis it is necessary for the dimensionality, and the chosen basis, to be independent of the type of element. This condition is satisfied by the admittance basis, as the dimensions of the matrix are determined by the number of nodes in the circuit, but the problem of infinite matrix elements remains.

The use of a variable that is initially treated as a finite variable (such as the gain of an op-amp, μ) and then at some point allowed to tend to infinity in order to define a limit is well known [7]. Talbot in 1965 used an *infinite parameter* $Y(Y \rightarrow \infty)$ in order to describe a number of elements in admittance matrix form, including the op-amp and the transformer [8]. Piercey (working with Talbot) and then Sewell extended the work of Talbot to the realm of circuit synthesis [9]–[11]. Using an infinite parameter $K(K \rightarrow \infty)$ and by deploying node introduction matrices and sometimes transformation matrices, Sewell synthesized the negative impedance converter and the circulator [10] and various single amplifier Sallen and Key-type circuits from their admittance matrices [11]. In the field of calculus, the hyper-real numbers (H or K) have been identified, which are greater than any real number but less than infinity and may be used like finite variables [12].

This paper extends previous work on the use of matrices with infinite elements. We will study their properties systematically

and show that they imply the existence of matrix equivalences. We will use those equivalences to derive a theorem and use that to provide a framework for analysis and synthesis of active circuits. The paper is based on preliminary work in [13] and [14]. We begin by considering a mathematical equivalence for admittance matrices of passive circuits.

II. PORT EQUIVALENCE FOR PASSIVE NETWORKS

A. Case Where All Circuit Nodes Are Accessible

Consider a circuit with n nodes, apart from the reference node. At this stage, let the circuit consist entirely of 2-terminal, linear, passive elements. Such an element has the admittance matrix stamp

$$
\begin{array}{c}
\quad\; g \quad\;\; h \\
\begin{array}{c} g \\ h \end{array}
\begin{bmatrix} y_i & -y_i \\ -y_i & y_i \end{bmatrix}
\end{array}
\tag{1}
$$

where y_i is the element admittance which is connected between nodes g and h; node names in (1) act as labels for the rows and columns the matrix elements occupy. The nodal admittance equations for the circuit may be expressed in the (homogeneous) form

$$
\mathbf{I} = \mathbf{Y}\mathbf{V}
\tag{2}
$$

where $\mathbf{I}$ is a column vector of node currents, $[I_1, I_2, \ldots, I_n]'$, $\mathbf{V}$ is a column vector of node voltages, $[V_1, V_2, \ldots V_n]$, and $\mathbf{Y}$ is the $n \times n$ nodal admittance matrix (NAM), which consists of a superposition of stamps of the form of (1). The matrix (2) defines a set of linear equations between components of $\mathbf{V}$ and $\mathbf{I}$. For a given circuit, $\mathbf{Y}$ is unique, and therefore there is a one-to-one correspondence between the circuit and $\mathbf{Y}$. We now consider the case where only some of the nodes are port nodes and the remainder are inaccessible, or internal, nodes for which the node current is zero.

B. Case Where Internal Nodes Exist

Consider a circuit with n nodes and p ports ($p < n$). At this stage, we still assume that the circuit consists entirely of 2-terminal, linear, passive elements. The nodal equations may be expressed in the form

$$
\begin{bmatrix} \mathbf{I_P} \\ \mathbf{0_{(n)}} \end{bmatrix} = \begin{bmatrix} \mathbf{Y_{11(n)}} & \mathbf{Y_{12(n)}} \\ \mathbf{Y_{21(n)}} & \mathbf{Y_{22(n)}} \end{bmatrix} \begin{bmatrix} \mathbf{V_P} \\ \mathbf{V_{i(n)}} \end{bmatrix}.
\tag{3}
$$

The partitioning separates rows and columns corresponding to the port nodes, $1, 2, \ldots p$, from those corresponding to the internal nodes, $p+1, p+2, \ldots n$. The second subscript (n) associated with some of the sub-matrices denotes that the dimensions of the complete admittance matrix are $n \times n$. Kirchhoff's current law (KCL) implies that the dependent current elements $I_{p+1}, I_{p+2}, \ldots I_n$, in rows corresponding to the internal nodes, are zero.

We can apply row operations iteratively in (3) in order to perform Gaussian elimination, subtracting the bottom row from each of the other rows after scaling it by a factor which reduces
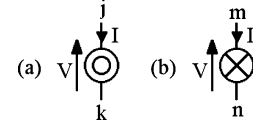

Fig. 1.   The nullor. (a) Nullator. (b) Norator.

the element in the last column to zero. The bottom row and last column may then be discarded to yield

$$
\begin{bmatrix} \mathbf{I_P} \\ \mathbf{0_{(n-1)}} \end{bmatrix} = \begin{bmatrix} \mathbf{Y_{11(n-1)}} & \mathbf{Y_{12(n-1)}} \\ \mathbf{Y_{21(n-1)}} & \mathbf{Y_{22(n-1)}} \end{bmatrix} \begin{bmatrix} \mathbf{V_P} \\ \mathbf{V_{i(n-1)}} \end{bmatrix}.
\tag{4}
$$

Application of $p - n$ such reductions will lead to the port matrix

$$
[\mathbf{I_P}] = [\mathbf{Y_{11(p)}}] [\mathbf{V_P}].
\tag{5}
$$

The reduced matrices could equally well have been obtained by performing column operations with scaling to make the elements in the last row zero. In order to ensure that when the matrices are reduced the port variables $(\mathbf{V}_{bfp}, \mathbf{I}_{bfp})$ are preserved, the source row or column for each operation must always correspond to an internal node.

Since each matrix in the series that starts with the NAM in (3) and ends with the port matrix in (5) reduces to the same port matrix, we may state that the matrices are equivalent in the sense that they describe the same port behaviour

$$
\begin{aligned}
\begin{bmatrix} \mathbf{Y_{11(n)}} & \mathbf{Y_{12(n)}} \\ \mathbf{Y_{21(n)}} & \mathbf{Y_{22(n)}} \end{bmatrix} &\equiv \begin{bmatrix} \mathbf{Y_{11(n-1)}} & \mathbf{Y_{12(n-1)}} \\ \mathbf{Y_{21(n-1)}} & \mathbf{Y_{22(n-1)}} \end{bmatrix} \\
&\equiv \begin{bmatrix} \mathbf{Y_{11(n-2)}} & \mathbf{Y_{12(n-2)}} \\ \mathbf{Y_{21(n-2)}} & \mathbf{Y_{22(n-2)}} \end{bmatrix} \\
&\equiv \cdots \\
&\equiv [\mathbf{Y_{11(p)}}].
\end{aligned}
\tag{6}
$$

The Gaussian elimination process, moving from left to right in (6) is one of circuit analysis. A reversal of this process, pivotal expansion, would correspond to circuit synthesis. For passive circuits in general, the synthesis problem posed this way may be intractable [15]. However, we have shown that the removal or introduction of internal nodes in a circuit permits the derivation of equivalent matrices that preserve the port behaviour. We refer to such equivalence between admittance matrices as *port equivalence*.

III. PORT EQUIVALENCE FOR ACTIVE NETWORKS

A. Limit Description for the Nullor

It has been shown that a sufficient set of elements to construct any active network consists of a number of passive element types and a single type of active element, the universal active element [16]. The universal active element is also known as the nullor and consists of a pair of 2-terminal elements called the nullator and norator, the symbols for which are shown in Fig. 1. The nullator imposes two constraints on its voltage and current, $V = 0$ and $I = 0$; the norator imposes no constraint on its voltage and current. The nullor may represent a small-signal
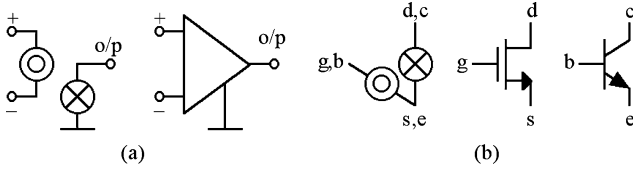
Fig. 2. Nullor equivalents. (a) Ideal op-amp. (b) Ideal FET and bipolar junction transistor.

model for the ideal op-amp and transistor as shown in Fig. 2, [17], [18]. The nullor may also be used, by itself or in conjunction with passive elements, to realise higher level active elements such as dependent sources [17], [19] or the complete family of current, voltage and hybrid types of op-amp [16], [20].

It is known that the nullor can be derived as a limit of any of the four types of dependent source when its gain tends to infinity. Since we are working with admittance matrices and the voltage-controlled current source (VCCS) is the only dependent source that possesses an admittance matrix, here we shall consider the nullor as a VCCS for which the transconductance gain tends to infinity. The admittance matrix stamp for the representation of a nullor with nullator connected between nodes j and k and norator connected between nodes m and n, as in Fig. 1, can be considered as that for a VCCS with transconductance G_{mi}

$$
\begin{array}{c}
\quad\quad j \quad\quad k \\
\begin{array}{c} m \\ n \end{array}
\left[
\begin{array}{cc}
G_{mi} & -G_{mi} \\
-G_{mi} & G_{mi}
\end{array}
\right]
\end{array}
\tag{7}
$$

where G_{mi} is taken to a limit of infinity. One way to preserve finiteness in an equation containing a parameter that tends to infinity is to divide the relationship by that parameter. Let us apply this approach in a set of NAM equations containing passive and active element stamps as in (1) and (7). At this stage, we assume that different nullor representations never co-exist in the same row or column of the NAM; this restriction will be removed later. For a nullor whose norator is connected to nodes m and n, rows m and n of the NAM equation set have the form

$$
\left[
\begin{array}{c}
I_m \\
I_n
\end{array}
\right]
=
\left[
\begin{array}{cc}
G_{mi} & -G_{mi} \\
-G_{mi} & G_{mi}
\end{array}
\right]
\left[
\begin{array}{c}
V_j \\
V_k
\end{array}
\right]
+
\left[
\begin{array}{c}
\text{finite terms} \\
\text{finite terms}
\end{array}
\right]
\tag{8}
$$

where $G_{mi} \to \infty$ (If m or n are internal nodes, then $I_m = 0$ or $I_n = 0$, respectively). Now consider dividing rows m and n of the matrix equation by G_{mi}

$$
\left[
\begin{array}{c}
I_m/G_{mi} \\
I_n/G_{mi}
\end{array}
\right]
=
\left[
\begin{array}{cc}
1 & -1 \\
-1 & 1
\end{array}
\right]
\left[
\begin{array}{c}
V_j \\
V_k
\end{array}
\right]
+
\left[
\begin{array}{c}
\text{finite terms}/G_{mi} \\
\text{finite terms}/G_{mi}
\end{array}
\right]
\tag{9}
$$

where $G_{mi} \to \infty$. Dependent current variable terms on the LHS and finite terms on the RHS vanish when the limit is taken

$$
\left[
\begin{array}{c}
0 \\
0
\end{array}
\right]
=
\left[
\begin{array}{cc}
1 & -1 \\
-1 & 1
\end{array}
\right]
\left[
\begin{array}{c}
V_j \\
V_k
\end{array}
\right]
+
\left[
\begin{array}{c}
0 \\
0
\end{array}
\right].
\tag{10}
$$

We are left with a relationship involving independent variables only. Both rows corresponding to the norator nodes in the NAM

set of equations yield the same relationship between the independent variables, namely

$$
V_j - V_k = 0.
\tag{11}
$$

Since the nullor description in (7) has no entries in row j or row k, we also have

$$
I_j = I_k = 0.
\tag{12}
$$

Hence the nullor description in (7) with $G_{mi} \to \infty$ imposes finite relationships between the nodal voltages and currents which correctly describe the nullator. The symmetry of the coefficients in (7) imposes the constraint that the current entering the norator is equal to that leaving it and (8) imposes KCL at nodes m and n; however, the norator voltage and current are otherwise unconstrained.

Thus, infinite limits of elements in the NAM (2) may be used providing we understand that the limit applies to the NAM equation rather than the NAM elements in isolation. Formally, the NAM port equivalence class, which defines circuit behaviour, has a well-defined limit in this case even though the NAM itself does not. One advantage of this formulation is that a single expression may be used to represent both a real circuit, for which the element has a finite value, and an idealized circuit. Taking the limit may thus be viewed as an abstraction, or approximation, operation that converts real circuits into the related ideal circuits. We shall see that this duality allows the framework we are developing to handle not only circuit analysis and synthesis, but also circuit modeling.

In order to make working with limits more practical, we now introduce a special notation.

B. Limit Variables

In the case where a matrix contains a variable x_i that approaches a limit k, we replace each instance of the variable x_i in the matrix by the *limit-variable* k_{xi}. In the limit variable notation k_{xi}, the subscript x_i denotes the variable that is involved in the limit and k denotes its limit value. The limit variable for $x_i \to k$ may be abbreviated to k_i, providing i refers unambiguously to the circuit variable x_i.

Where the limit is a limit to infinity, the limit variable is called an infinity-variable, or ∞-variable, and written ∞_i, where i refers to the circuit element whose parameter is being taken to infinity. Using ∞-variables, the nullor description in (7) takes the form

$$
\begin{array}{c}
\quad\quad j \quad\quad k \\
\begin{array}{c} m \\ n \end{array}
\left[
\begin{array}{cc}
\infty_i & -\infty_i \\
-\infty_i & \infty_i
\end{array}
\right].
\end{array}
\tag{13}
$$

The ideal short circuit is equivalent to the parallel connection of a nullator and norator; thus it has an admittance matrix description similar to that for the nullor in (13) except that the elements are arranged symmetrically

$$
\begin{array}{c}
\quad\quad j \quad\quad k \\
\begin{array}{c} j \\ k \end{array}
\left[
\begin{array}{cc}
\infty_i & -\infty_i \\
-\infty_i & \infty_i
\end{array}
\right].
\end{array}
\tag{14}
$$

Replacement of regular variables in an NAM by limit-variables implies that these variables can no longer be given numerical values and have to be treated as symbolic variables that may be manipulated by hand or by using symbolic computation. Since ∞-variables are shorthand for finite variables with infinite limits, and algebraic transformations may be applied before taking the limit, it follows that ∞-variables must conform to the rules of algebra for regular variables, including Gaussian elimination and pivotal expansion of admittance matrices.[1] The concept of port-equivalence, developed in Section II-B for passive networks, is therefore equally applicable to matrices containing ∞-variables. Using the ∞-variable as a placeholder for a variable that can tend to infinity at some point is just a notational convenience. The real advantage comes from special operations that are possible only for matrices containing ∞-variables.

C. Operations for Matrices Containing ∞-Variables

We begin by considering the general form that admittance matrix elements may take during a process of Gaussian elimination. A circuit consisting of passive elements and nullors can be described by an NAM consisting of a superposition of stamps as in (1) and (13). Each element of the NAM must consist, in general, of a signed sum of passive element admittances $(\pm y_i)$ and ∞-variables $(\pm \infty_i)$. It may be shown that, provided the admittance of each circuit element is represented by a unique variable, reduction of the NAM to the port matrix leads to matrix elements at every stage which are bilinear functions of each circuit variable [17], [21]. Thus, in terms of an ∞-variable for a particular nullor (nullor i), each matrix element at every stage of the reduction has the form

$$y_{rc(s)} = \frac{A_{rc(s)}\infty_i + B_{rc(s)}}{C_{rc(s)}\infty_i + D_{rc(s)}} \qquad (15)$$

where r and c denote the row and column the element is in and s denotes the stage of the reduction process $p \leq s \leq n$. We now consider taking limits in respect of such a typical matrix element.

Provided the coefficients in (15) are finite, then taking the limit in respect of ∞_i can yield only three possible limiting values, which are $0, k_1$ or $k_2\infty_i$, where k_1 and k_2 are finite.[2] Hence, in the case where the ∞_i element survives the limit, it may be multiplied by a finite quantity.

In the case where the coefficients in (15) contain other ∞-variables, a number of cases arise: 1) a finite limit is obtainable; 2) a function of two or more ∞-variables may be set equal to a composite ∞-variable (this case applies if a differential pair of field-effect transistors (FETs) are represented and the node the sources are connected to is eliminated [22]); and 3) known relationships between ∞-variables may be introduced in order to reduce the number of ∞-variables, to one (as when the geometries and bias conditions of FETs have known interdependencies [23]). It is clear that an ∞-variable that emerges from these scenarios may have a finite scaling factor.

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[1]This is true under the assumption that the circuit described is nondegenerate, as will be the case for all physically realizable circuits.

[2]We exclude discussion here of the case where both denominator coefficients are zero; this will be discussed in Section IX.

When we allow for a finite scaling factor associated with an ∞-variable, it is necessary to ensure that the constraints imposed by the complete set of ∞-variables are consistent. This requirement can be met by introducing, into the set of ∞-variables describing the nullor in (13), a row scaling factor α and a column scaling factor β

$$\begin{array}{c} \\ m \\ n \end{array} \begin{array}{cc} j & k \\ \left[\begin{array}{cc} \infty_i & -\beta\infty_i \\ -\alpha\infty_i & \alpha\beta\infty_i \end{array} \right]. \end{array} \qquad (16)$$

For this matrix, the constraint imposed by each row is identical and given by $V_j = \beta V_k$ and the constraint imposed by each column is identical and given by $I_n = -\alpha I_{m_,}$. The set of elements in (16) is a very general one that can represent the class of 2-port circuits which do not, in the conventional sense, possess an admittance matrix; this class includes the nullor and short-circuit, and all the elements whose stamps we will derive in Sections V–VII.

Following the procedure adopted in Section III-A for interpreting the nullor description in (7), let us divide row m and column j of the matrix equation set corresponding to (16) by ∞_i to create row m' and column j' for use in performing row and column operations

$$\begin{array}{c} \\ m \\ n \\ m' \end{array} \begin{array}{cccc} j & k & & j' \\ \left[\begin{array}{cc} \infty_i & -\beta\infty_i \\ -\alpha\infty_i & \alpha\beta\infty_i \end{array} \right] & \begin{array}{c} 1 \\ -\alpha \end{array} \\ \begin{array}{cc} 1 & \end{array} & -\beta \end{array}. \qquad (17)$$

All other elements in the row m' and column j' become zero, including dependent currents on the LHS of the matrix equation in the case where the source row corresponds to a port node. If we had derived (17) starting from the second row or second column of (16) instead of the first row and column, we would have obtained an identical result.

Thus, the presence of ∞-variables in an admittance matrix permits the carrying out of special row and column operations that preserve port equivalence; these are in addition to the general ones for finite NAMs described in Section II-B that are equally applicable to matrices containing ∞-variables. The special operations differ from the ordinary ones in that the source row and column are not restricted to correspond to internal nodes and in that it is only coefficients of ∞-variables that are scaled and added to other rows and columns of the matrix. Thus, the admittance matrix of a circuit containing nullors where all of its nodes are accessible is not unique, as it is in the case of a network of passive elements. Before developing theorems from the special row and column operations, we consider the case where two or more sets of ∞-variables share a row or column of an admittance matrix.

D. Case Where Different ∞-Variables Co-Exist in a Single Row or Column of [Y]

We amend the first row of the admittance matrix shown in (16) by introducing a second set of ∞-variables $\pm\infty_j$ with column scaling factor β_j

$$\begin{array}{c} \\ m \end{array} \begin{array}{cccc} j & k & r & s \\ \left[\begin{array}{cccc} \infty_i & -\beta_i\infty_i & \infty_j & -\beta_j\infty_j \end{array} \right]. \end{array} \qquad (18)$$

The nodal equation for this row may be written as

$$I_m = \infty_i(V_j - \beta_i V_k) + \infty_j(V_r - \beta_j V_s) + \text{finite terms} \quad (19)$$

where I_m is the nodal current ($I_m = 0$ if m is an internal node) and the finite terms may exist in any columns. Let us divide (19) by ∞_i

$$\frac{I_m}{\infty_i} = V_j - \beta_i V_k + \frac{\infty_j}{\infty_i}(V_r - \beta_j V_s) + \frac{\text{finite terms}}{\infty_i}. \quad (20)$$

Since ∞_i and ∞_j are independent variables approaching the limit of infinity, this equation must be true for all finite values of ∞_j/∞_i. Hence, in the limit, the solution to (20) yields two separate equations

$$\begin{aligned} V_j - \beta_i V_k &= 0 \\ V_r - \beta_j V_s &= 0. \end{aligned} \quad (21)$$

Thus, each set of ∞-variables yields a separate row, corresponding to one of the expressions in (21), that may be used as a source row for row operations

$$\begin{array}{c} \begin{array}{cccc} j & k & r & s \end{array} \\ \begin{array}{c} m \\ m' \\ m'' \end{array} \left[\begin{array}{cccc} \infty_i & -\beta_i\infty_i & \infty_j & -\beta_j\infty_j \\ 1 & -\beta_i & & \\ & & 1 & -\beta_j \end{array} \right]. \end{array} \quad (22)$$

The same outcome arises where two sets of ∞-variables share a column of the matrix and applies irrespective of the number of sets of ∞-variables that share a row or column. Thus, each set of ∞-variables that shares a row or column with other sets of ∞-variables generates its own row and column that may be used for row and column operations.

IV. THEOREM FOR MATRICES WITH ∞-VARIABLES

A. Arbitrary Element Theorem

From the general set of ∞-variables in (16), we may derive an extra row m' and column j' as in (17), scale the extra row and column by arbitrary factors and then add them to any row or column, respectively

$$\begin{array}{c} \begin{array}{cc} j & k \end{array} \\ \begin{array}{c} m \\ n \end{array} \left[\begin{array}{cc} \infty_i & -\beta\infty_i \\ -\alpha\infty_i & \alpha\beta\infty_i \end{array} \right] \end{array} \rightarrow \begin{array}{c} \begin{array}{ccc} j & kk & p \end{array} \\ \begin{array}{c} m \\ n \\ q \end{array} \left[\begin{array}{ccc} \infty_i & -\beta\infty_i & a_p \\ -\alpha\infty_i & \alpha\beta\infty_i & -\alpha a_p \\ b_q & -\beta b_q & \ddots \end{array} \right]. \quad (23)$$

Variables a_p and b_q are arbitrary expressions and q and p represent any row or column including the source rows and columns, m, n and j, k. We call this equivalence the *arbitrary element theorem*. If a_p and b_q were to contain ∞-variables, there would be an inconsistency in the derivation; hence the arbitrary elements a_p and b_q in (23) are restricted to be finite. We now consider a particularly useful corollary of the arbitrary element theorem.

B. Element Shift Theorem

We apply the arbitrary element theorem in (23) in the special case where there already exist matrix elements y_{mp} and y_{qj} and we let $a_p = -y_{mp}$ and $b_q = -y_{qj}$

$$\begin{array}{c} \begin{array}{ccc} j & k & p \end{array} \\ \begin{array}{c} m \\ n \\ q \end{array} \left[\begin{array}{ccc} \infty_i & -\beta\infty_i & y_{mp} \\ -\alpha\infty_i & \alpha\beta\infty_i & 0 \\ y_{qj} & 0 & \ddots \end{array} \right] \equiv \begin{array}{c} \begin{array}{ccc} j & k & p \end{array} \\ \begin{array}{c} m \\ n \\ q \end{array} \left[\begin{array}{ccc} \infty_i & -\beta\infty_i & 0 \\ -\alpha\infty_i & \alpha\beta\infty_i & \alpha y_{mp} \\ 0 & \beta y_{qj} & \ddots \end{array} \right]. \quad (24)$$

The effect is to eliminate y_{mp} and y_{qj} from their original positions and shift them as shown while scaling them by the appropriate row or column scaling factor α or β, respectively. Where y_{mp} and y_{qj} consist of a sum of admittance terms, then the shift theorem may be applied to any sub-set of these terms. If y_{mp} or y_{qj} are ∞-variables, then (24)-LH already implies some constraints on V_p and I_q;[3] since these constraints are unchanged in (24)-RH, it follows that, in this corollary of the theorem, y_{mp} and y_{qj} are permitted to be ∞-variables.

C. Arbitrary Element and Element Shift Theorems for the Nullor

The description for the nullor corresponds to setting $\alpha = \beta = 1$ in (16), in which case the arbitrary element theorem in (23) takes the form

$$\begin{array}{c} \begin{array}{cc} j & k \end{array} \\ \begin{array}{c} m \\ n \end{array} \left[\begin{array}{cc} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{array} \right] \end{array} \rightarrow \begin{array}{c} \begin{array}{ccc} j & k & p \end{array} \\ \begin{array}{c} m \\ n \\ q \end{array} \left[\begin{array}{ccc} \infty_i & -\infty_i & a_p \\ -\infty_i & \infty_i & -a_p \\ b_q & -b_q & \ddots \end{array} \right]. \quad (25)$$

Under the same conditions, the element shift theorem of (24) takes the following forms for finite and for ∞-variable elements:

$$\begin{array}{c} \begin{array}{ccc} j & k & p \end{array} \\ \begin{array}{c} m \\ n \\ q \end{array} \left[\begin{array}{ccc} \infty_i & -\infty_i & y_{mp} \\ -\infty_i & \infty_i & 0 \\ y_{qj} & 0 & \ddots \end{array} \right] \end{array} \rightarrow \begin{array}{c} \begin{array}{ccc} j & k & p \end{array} \\ \begin{array}{c} m \\ n \\ q \end{array} \left[\begin{array}{ccc} \infty_i & -\infty_i & 0 \\ -\infty_i & \infty_i & y_{mp} \\ 0 & y_{qj} & \ddots \end{array} \right] \quad (26)$$

$$\begin{array}{c} \begin{array}{ccc} j & k & p \end{array} \\ \begin{array}{c} m \\ n \\ q \end{array} \left[\begin{array}{ccc} \infty_i & -\infty_i & \infty_r \\ -\infty_i & \infty_i & 0 \\ \infty_s & 0 & \ddots \end{array} \right] \end{array} \rightarrow \begin{array}{c} \begin{array}{ccc} j & k & p \end{array} \\ \begin{array}{c} m \\ n \\ q \end{array} \left[\begin{array}{ccc} \infty_i & -\infty_i & 0 \\ -\infty_i & \infty_i & \infty_r \\ 0 & \infty_s & \ddots \end{array} \right]. \quad (27)$$

Davies and others [24]–[26] have suggested a method of analysis for circuits containing nullors in which the rows of the matrix corresponding to the nodes of each norator are combined into a single row and the columns corresponding to the nodes of each nullator are combined into a single column. The theorems in (25), (26), and (27) are consistent with this method of analysis, because introduction of elements or movement of

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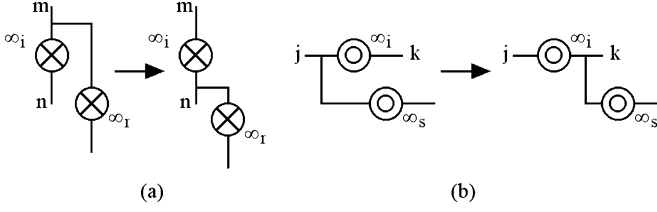[3]LH and RH denote left-hand and right-hand matrices, respectively.

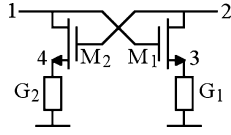Fig. 3. Nullor tree transformations. (a) For norators. (b) For nullators.

Fig. 4. Transistor circuit example.

elements, the effect of which is eliminated when the circuit is analysed, can clearly not affect the result of the analysis.

The shift of the ∞_r element in (27) is illustrated in Fig. 3(a) and corresponds to one node of the norator r shifting from node m to node n of norator i. Similarly, the movement of the ∞_s element in (27) corresponds to one node of the nullator s shifting from node j to node k of nullator i, as illustrated in Fig. 3(b). Hence, (27) is a description of the well-known nullator and norator tree transformations [18].

D. Arbitrary Scale Factor Theorem

The constraints imposed on node voltages and currents by the ∞_i terms in (16) are trivially unchanged if the parameter ∞_i in (16) is scaled by a finite scaling factor C. Hence, there exists the equivalence

$$
\begin{array}{c} \\ m \\ n \end{array}
\begin{array}{cc} j & k \\ \begin{bmatrix} \infty_i & -\beta\infty_i \\ -\alpha\infty_i & \alpha\beta\infty_i \end{bmatrix} \end{array}
\rightarrow
\begin{array}{c} \\ m \\ n \end{array}
\begin{array}{cc} j & k \\ \begin{bmatrix} C\infty_i & -\beta C\infty_i \\ -\alpha C\infty_i & \alpha\beta C\infty_i \end{bmatrix} \end{array}. \quad (28)
$$

where scaling factor C is arbitrary and omitted elements not including ∞_i are unaffected.

We now present an example of the use of the equivalence theorems for analysis and synthesis of a simple active circuit.

E. Simple Example to Illustrate Application of Theorems

1) Circuit Analysis: Consider the 2-port circuit in Fig. 4 consisting of two transistors and two resistors. Treating the transistors M_i as ideal and modeling each as a VCCS with transconductance represented by a limit-variable ∞_{mi}, the NAM of this circuit is shown in the first matrix of (29) (unlabelled rows and columns are assumed to be in numerical order and correspond to the node numbers in the circuit). By virtue of the $\pm\infty_{m1}$ elements, we use the element shift theorem to move element G_1 to column 1 and then to row 2 and, by virtue of the $\pm\infty_{m2}$ elements, we move element G_2 to column 2 and then to row 1, which leads to the second

matrix in (29), where the arrow denotes a procedure based on port-equivalence

$$
\begin{bmatrix}
0 & \infty_{m2} & 0 & -\infty_{m2} \\
\infty_{m1} & 0 & -\infty_{m1} & 0 \\
-\infty_{m1} & 0 & G_1+\infty_{m1} & 0 \\
0 & -\infty_{m2} & 0 & G_2+\infty_{m2}
\end{bmatrix}
$$

$$\downarrow$$

$$
\begin{bmatrix}
0 & G_2+\infty_{m2} & 0 & -\infty_{m2} \\
G_1+\infty_{m1} & 0 & -\infty_{m1} & 0 \\
-\infty_{m1} & 0 & \infty_{m1} & 0 \\
0 & -\infty_{m2} & 0 & \infty_{m2}
\end{bmatrix} \quad (29)
$$

$$\downarrow$$

$$
\begin{bmatrix}
0 & G_2 & 0 & 0 \\
G_1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0
\end{bmatrix}
\rightarrow
\begin{bmatrix}
0 & G_2 \\
G_1 & 0
\end{bmatrix}.
$$

In going from the second matrix to the third matrix, the ∞-variables have been removed. This step may be made in a number of ways, including: 1) Gaussian elimination to eliminate the $\pm\infty_{m1}$ and $\pm\infty_{m2}$ elements in row and column 3 and 4; 2) recognition that each set of ∞-variables describes a nullator and norator connected in series which is equivalent to an open-circuit and may be removed; and 3) using the ∞-variables in rows 3 and 4 to apply the element shift theorem in order to cancel the ∞-variables in rows 1 and 2 followed by removal of remaining elements in rows 3 and 4. The zeros in row and column 3 and 4 in the 3$^{\text{rd}}$ matrix of (29) represent two isolated nodes that may be removed to obtain the 2×2 port matrix, which shows that the circuit is a negative impedance inverter.

2) Circuit Synthesis: We start from the port admittance matrix for a negative impedance inverter given in the first matrix of (30). We will realise this matrix using ideal transistors, i.e., nullors, and 2-terminal passive elements, resistors in this case. In order that the G_1 and G_2 elements are realized by resistors, they must be moved on to the main diagonal. In order to make room for them, we introduce two rows and columns of zeros, as shown in the second matrix in (30)

$$
\begin{bmatrix}
0 & G_2 \\
G_1 & 0
\end{bmatrix}
\rightarrow
\begin{bmatrix}
0 & G_2 & 0 & 0 \\
G_1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0
\end{bmatrix}
$$

$$\downarrow$$

$$
\begin{bmatrix}
0 & G_2+\infty_{m2} & 0 & -\infty_{m2} \\
G_1+\infty_{m1} & 0 & -\infty_{m1} & 0 \\
-\infty_{m1} & 0 & \infty_{m1} & 0 \\
0 & -\infty_{m2} & 0 & \infty_{m2}
\end{bmatrix} \quad (30)
$$

$$\downarrow$$

$$
\begin{bmatrix}
0 & \infty_{m2} & 0 & -\infty_{m2} \\
\infty_{m1} & 0 & -\infty_{m1} & 0 \\
-\infty_{m1} & 0 & G_1+\infty_{m1} & 0 \\
0 & -\infty_{m2} & 0 & G_2+\infty_{m2}
\end{bmatrix}.
$$

The third matrix in (30) differs from the second one in that $\pm\infty_{m1}$ and $\pm\infty_{m2}$ elements have been introduced. A procedure for performing this step can be generalized as follows:

$$
[y_e] \rightarrow
\begin{bmatrix} y_e & 0 \\ 0 & 0 \end{bmatrix}
\rightarrow
\begin{bmatrix} y_e+\infty_i-\frac{(-\infty_i)^2}{\infty_i} & 0 \\ 0 & 0 \end{bmatrix}
$$

$$
\rightarrow
\begin{bmatrix} y_e+\infty_i & -\infty_i \\ -\infty_i & \infty_i \end{bmatrix}. \quad (31)
$$

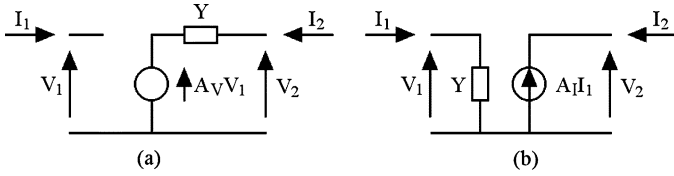Fig. 5. Equivalent circuits. (a) For nonideal VCVS. (b) For nonideal CCCS.

Fig. 6. Alternative equivalent circuits for the nonideal CCVS.

Element y_e represents an existing matrix element that we wish to shift. After introducing a blank row and column, element y_e is then augmented by a function that evaluates to zero but can be expanded pivotally as in the last matrix in (31). Once the $\pm\infty_{m1}$ and $\pm\infty_{m2}$ elements are in place in the third matrix in (30), the element shift theorem may be applied to shift elements G_1 and G_2 to their diagonal positions, as in the final matrix in (30), that is the NAM of the circuit in Fig. 4.

An alternative way of introducing the $\pm\infty_{mi}$ elements in the third matrix of (30) is to recognise that introduction of a blank row and column, as in the second matrix, is equivalent to introducing an isolated node into the circuit [27]. The voltage at an isolated node is unobservable and its current is zero. Since the voltage is unobservable, we may define its voltage by linking it to any other node by a nullator. Since the current at the isolated node with the introduced nullator is zero, we may also link the isolated node to any other node by a norator. The movements of elements that we wish to make govern the nodes to which the nullator and norator are connected. Thus, by linking the nullator and norator at node 3 to nodes 1 and 2, respectively, and the nullator and norator at node 4 to nodes 2 and 1, respectively, we obtain the third matrix in (30).

Having presented the theorem for matrices with ∞-variable elements and illustrated its use, we now use ∞-variables to write admittance matrix descriptions for the dependent sources and for the impedance converter.

V. ADMITTANCE MATRIX DESCRIPTIONS FOR VCVS AND CCCS

We approach the problem of the nonexistence of admittance matrices for the ideal voltage-controlled voltage source (VCVS) and current-controlled current source (CCCS) by considering the circuits in Fig. 5(a) and (b), respectively, which do have admittance matrices and which can approach the ideal VCVS and CCCS as limiting cases. (Note that we have defined the current gain of the CCCS as $A_I = -I_2/I_1$.) The admittance matrices for the circuits in Fig. 5 are as follows:

$$\mathbf{Y}_{\text{VCVS}} = \begin{bmatrix} 0 & 0 \\ -A_v Y & Y \end{bmatrix} \quad \mathbf{Y}_{\text{CCCS}} = \begin{bmatrix} Y & 0 \\ -A_I Y & 0 \end{bmatrix}. \quad (32)$$

The nonideal VCVS and CCCS circuits approach their ideal counterparts if we let $Y \to \infty$. Using ∞-variables to imply limits in (32), we obtain the following admittance matrices for the ideal VCVS and CCCS:

$$\mathbf{Y}_{\text{VCVS}} = \begin{bmatrix} 0 & 0 \\ -A_v\infty_y & \infty_y \end{bmatrix}$$

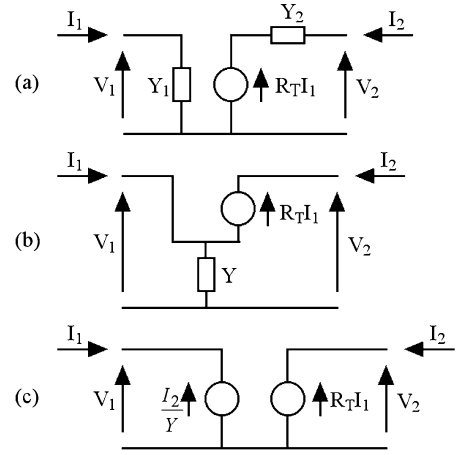$$\mathbf{Y}_{\text{CCCS}} = \begin{bmatrix} \infty_y & 0 \\ -A_I\infty_y & 0 \end{bmatrix}. \quad (33)$$

The VCVS and CCCS circuits in Fig. 5 have their input and output ports grounded. Descriptions for nongrounded dependent sources are presented in the Appendix.

VI. ADMITTANCE MATRIX DESCRIPTIONS FOR CCVS

An equivalent circuit for a nonideal current-controlled voltage source (CCVS) that possesses an admittance matrix is shown in Fig. 6(a). The circuit becomes ideal when $Y_1 \to \infty$ and $Y_2 \to \infty$. Analysis of the circuit and setting $Y_1 \to \infty_1$ and $Y_2 \to \infty_2$ yields the admittance matrices

$$\mathbf{Y}_{\text{CCVS}(1)} = \begin{bmatrix} Y_1 & 0 \\ -Y_1 Y_2 R_T & Y_2 \end{bmatrix} \to \begin{bmatrix} \infty_1 & 0 \\ -\infty_1\infty_2 R_T & \infty_2 \end{bmatrix}. \quad (34)$$

The equivalent circuit for the CCVS in Fig. 6(a) can be considered to be a natural one in the sense that the elements Y_1 and Y_2 that tend to infinity can be interpreted as input and output admittances of a circuit or device that implements the CCVS. However, the matrix description in (34) appears uneconomical compared with those for the VCVS and CCCS in (33) that require only a single ∞-variable. We now derive a more economical description.

The infinite input and output admittances of the ideal CCVS can be handled by introducing into the ideal CCVS just a single admittance provided that it is located in the connection to the reference node, as shown in Fig. 6(b). Analysis of this circuit and setting Y to ∞_y leads to the admittance matrices

$$\mathbf{Y}_{\text{CCVS}(2)} = \begin{bmatrix} -G_T & G_T \\ Y + G_T & -G_T \end{bmatrix} \to \begin{bmatrix} -G_T & G_T \\ \infty_y + G_T & -G_T \end{bmatrix} \quad (35)$$

where $G_T = R_T^{-1}$. We have reduced the number of ∞-variables to one, but the number of nonzero elements in the matrix has increased and we now seek a means to reduce their number.

The derivation of equivalent admittance matrix descriptions by picking circuit models, as was done using those in Fig. 6(a) and (b), is ad hoc in the since that it provides no mathematical link between the two circuits. A more systematic approach would be to develop alternative models using the theorem of Section IV, which offers the potential of mathematical proof

since it is derived via row and column operations. We now illustrate the use of the theorem.

The element ∞_y in (35)-RH can be considered as a special case of the general set of ∞-variables in (25)-LH with nodes n and k coincident with the reference node. It follows from (25) that we can add arbitrary finite elements in the row and column that the element ∞_y occupies, i.e., in row 2 and column 1 of (35)-RH. Let us add $\pm G_T$ elements in the following positions:

$$\mathbf{Y}_{\text{CCVS(3)}} = \begin{bmatrix} -G_T + G_T & G_T \\ \infty_y + G_T - G_T & -G_T + G_T \end{bmatrix}$$
$$= \begin{bmatrix} 0 & G_T \\ \infty_y & 0 \end{bmatrix}. \tag{36}$$

We now have an admittance matrix description for the CCVS that has two zero elements and is as simple as the descriptions for the VCVS and CCCS. By setting ∞_y in (36)-RH to a finite parameter Y and deriving the port equations, we can determine the corresponding equivalent circuit, and this is shown in Fig. 6(c). It can be seen that the parameter Y that tends to infinity is associated with a CCVS at the input port. Although this equivalent circuit corresponds to a simple admittance matrix, it is not a natural equivalent circuit from a modeling point of view. Thus, whereas for the VCVS and CCCS the natural equivalent circuits in Fig. 5 yield the canonical admittance matrices (33), for the CCVS there is a trade-off between having a natural equivalent circuit model and a simple matrix description.

The three alternative admittance matrices that we have derived for the CCVS in (34), (35) and (36) are equivalent at the limit. In spite of the fact that they have different forms, they must yield identical solutions when the same port constraint is applied. As an example, let us use these matrices to calculate the open-circuit trans-impedance

$$z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2=0} = \left[y_{12} - \frac{y_{11} y_{22}}{y_{21}} \right]^{-1}. \tag{37}$$

Using the descriptions in (34), (35), and (36), we obtain

$$z_{21(1)} = \frac{1}{0 - \frac{\infty_1 \infty_2}{-\infty_1 \infty_2 R_T}}$$
$$= R_T$$
$$z_{21(2)} = \frac{1}{G_T - \frac{(-G_T)(-G_T)}{\infty_y + G_T}}$$
$$= \frac{\infty_y + G_T}{\infty_y G_T} \rightarrow R_T$$
$$z_{21(3)} = \frac{1}{G_T - \frac{0 \times 0}{\infty_y}}$$
$$= R_T. \tag{38}$$

The results are identical and correct. The analysis shows that, for the specified network function and port constraint, $z_{21(1)}$ and $z_{21(3)}$ behave in an ideal way even for finite parameters ($\infty_1 \rightarrow G_{m1}, \infty_2 \rightarrow G_{m2}, \infty_y \rightarrow Y$). On the other hand for $z_{21(2)}$ it is necessary that the limit is taken. Note that the application to port-equivalent matrices of constraints that are incompatible with the circuit function may lead to different (but meaningless) solutions. E.g., for the CCVS descriptions in (34), (35) and (36), the incompatible constraint $V_2 = 0$, yields very different input admittances I_1/V_1 of $\infty_1, -G_T$ and 0, respectively.
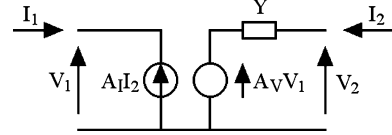

Fig. 7.   Equivalent circuit for the nonideal impedance converter.

VII. Admittance Matrix Description for Impedance Converter

A natural equivalent circuit for a nonideal impedance converter is shown in Fig. 7. The circuit becomes ideal when $Y \rightarrow \infty$. Note that the impedance converter is defined by two parameters, namely the forward voltage gain $A_V = V_2/V_1$ and the reverse current gain $A_I = -I_1/I_2$. Analysis of the circuit in Fig. 7 and letting $Y \rightarrow \infty_y$ yields the admittance matrices

$$\mathbf{Y}_{\text{conv}} = \begin{bmatrix} A_V A_I Y & -A_I Y \\ -A_V Y & Y \end{bmatrix} \rightarrow \begin{bmatrix} A_V A_I \infty_y & -A_I \infty_y \\ -A_V \infty_y & \infty_y \end{bmatrix}. \tag{39}$$

With $A_V = A_I = n$, (39)-RH describes a transformer with turns-ratio n [8]

$$\mathbf{Y}_{\text{transformer}} = \begin{bmatrix} n^2 \infty_y & -n \infty_y \\ -n \infty_y & \infty_y \end{bmatrix}. \tag{40}$$

The impedance transforming property of the transformer (load admittance Y_L at port 2 multiplied by n^2 when shifted to port 1) follows directly from (40) using the element shift theorem of (24)

$$\begin{bmatrix} n^2 \infty_y & -n \infty_y \\ -n \infty_y & \infty_y + Y_L \end{bmatrix} \rightarrow \begin{bmatrix} n^2 \infty_y & -n \infty_y \\ -n \infty_y + n Y_L & \infty_y \end{bmatrix}$$
$$\rightarrow \begin{bmatrix} n^2 \infty_y + n^2 Y_L & -n \infty_y \\ -n \infty_y & \infty_y \end{bmatrix}. \tag{41}$$

With $A_V = A_I = 1$, the impedance converter reverts to a unity turns-ratio transformer which is equivalent to a short-circuit between the ports and its admittance matrix in (39)-RH reduces to that already given for the short-circuit in (14).

A complete set of canonical admittance matrix descriptions, or stamps, for the dependent sources, nongrounded as well as grounded, and the impedance converter, is presented in the Appendix.

VIII. Discussion

A. Framework for Circuit Analysis and Identification

We have shown that for a circuit containing ideal active elements represented by nullors, each nullor may be represented in the NAM by a stamp containing ∞-variables. We then showed that not only nullors but also all dependent sources and the impedance converter have admittance matrix descriptions containing ∞-variables. It follows that when a circuit possesses such higher-level active elements, the NAM may be constructed using their ∞-variable representations directly without the need to make use of nullor equivalents.

Many circuits have specified voltage or current transfer functions, V_2/V_1 or I_2/I_1, which are independent of load. The 2-port admittance matrix of such a circuit may be viewed as that for a
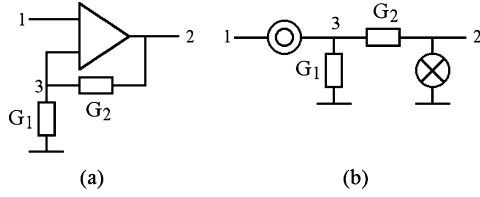
Fig. 8. (a) Circuit for example. (b) Nullor equivalent.

VCVS or CCCS where the gain of the dependent source is the voltage or current transfer function of the circuit. Hence, matrices containing ∞-variables may be used not only as stamps for the active elements contained in a circuit in the NAM but also as stamps which enable identification of the functional type of a circuit from the port matrix obtained by reducing the NAM.

Thus, the concepts of port equivalence and ∞-variables provide a framework where a circuit containing any type of linear element may be represented in an NAM and, after reduction of the NAM to the port matrix, the circuit functional type may be reliably identified. To facilitate such identification, a catalogue of alternative forms of admittance matrices for key circuit functions is given in the appendix.

B. Comparison With Modified Nodal Analysis

An example circuit containing an op-amp is shown in Fig. 8, together with the nullor equivalent valid for the case where the op-amp is considered ideal. The nodal admittance matrices of the circuit in Fig. 8 using ∞-variables and the MNA may be written by inspection

$$\mathbf{Y}_{\infty-\text{var}} = \begin{bmatrix} 0 & 0 & 0 \\ -\infty_1 & G_2 & -G_2 +\infty_1 \\ 0 & -G_2 & G_2 + G_1 \end{bmatrix}$$

$$\mathbf{Y}_{\text{MNA}} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_2 & -G_2 & 1 \\ 0 & -G_2 & G_2 + G_1 & 0 \\ 1 & 0 & -1 & 0 \end{bmatrix}. \tag{42}$$

We carry out Gaussian elimination on the modified matrix $\mathbf{Y}_{\text{MNA}}$ first using the y_{33} element as a pivot and then discard row 3 and column 3

$$\mathbf{Y}_{\text{MNA}} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_2 & -G_2 & 1 \\ 0 & -G_2 & \boxed{G_2 + G_1} & 0 \\ 1 & 0 & -1 & 0 \end{bmatrix}$$

$$= \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & \frac{G_1 G_2}{G_1+G_2} & 0 & 1 \\ 0 & 0 & 0 & 0 \\ 1 & -\frac{G_2}{G_1+G_2} & 0 & 0 \end{bmatrix}$$

$$= \begin{bmatrix} 0 & 0 & 0 \\ 0 & \frac{G_1 G_2}{G_1+G_2} & 1 \\ 1 & -\frac{G_2}{G_1+G_2} & 0 \end{bmatrix}. \tag{43}$$

The result is a stamp in modified nodal form for a VCVS of gain $A_V = (G_1 + G_2)/G_2$ [4]. The y_{22} element is redundant.
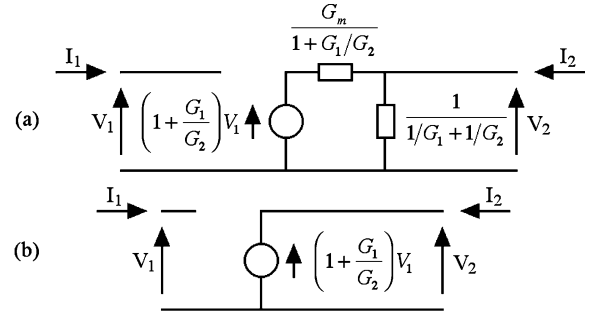

Fig. 9. (a) Exact model for circuit in Fig. 8. (b) Ideal model.

Consider now the reduction of the admittance matrix $\mathbf{Y}_{\infty-\text{var}}$ in (42). Using Gaussian elimination with y_{33} as the pivot, we obtain the 2×2 port matrix[4]

$$\mathbf{Y}_{\infty-\text{var}} = \begin{bmatrix} 0 & 0 & 0 \\ -\infty_1 & G_2 & -G_2 +\infty_1 \\ 0 & -G_2 & \boxed{G_2 + G_1} \end{bmatrix}$$

$$\equiv \begin{bmatrix} 0 & 0 \\ -\infty_1 & \frac{G_2(G_1+\infty_1)}{G_2+G_1} \end{bmatrix}. \tag{44}$$

This description is valid for finite values of ∞_1 and can be represented by a nonideal model containing a VCVS as shown in Fig. 9(a), where G_m has replaced ∞_1 and denotes the finite transconductance of the op-amp.

We can now take the limit in (44)

$$\mathbf{Y}_{\infty-\text{var}} \equiv \begin{bmatrix} 0 & 0 \\ -\infty_1 & \frac{G_2(G_1+\infty_1)}{G_2+G_1} \end{bmatrix} \rightarrow \begin{bmatrix} 0 & 0 \\ -\infty_1 & \frac{G_2}{G_2+G_1}\infty_1 \end{bmatrix}. \tag{45}$$

From Table III (in the Appendix), we can see that the matrix obtained describes an ideal VCVS with voltage transfer function $A_V = (G_1 + G_2)/G_2$. It yields the ideal model in Fig. 9(b) for the circuit of Fig. 8.

This example illustrates the advantages for symbolic analysis of the ∞-variable approach over the MNA. These are that the matrix dimensions are smaller, it is possible to derive a port matrix, the method encompasses both ideal analysis and nonideal analysis and modeling, and there are no redundant or arbitrary parameters.

C. Circuit Synthesis

The existence of a framework for ideal active circuits provides a potential capability for systematic circuit synthesis. As a means to develop the framework, the synthesis of known circuits has been considered so far. These circuits fall into three categories that are shown in Table I, together with circuit details and references. The restriction that the synthesis process is symbolic means that the initial specification must be in symbolic form and this does restrict the scope of this method to circuits where the complexity and order are limited. In spite of this, it is anticipated that the framework is capable of yielding useful

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[4]There is an apparent indeterminacy in determining the modified y_{21} element. The full expression is $y'_{21} = -\infty_1 - (\varepsilon_{31} \times (-G_2 +\infty_1))/(G_2+G_1) = -\infty_1(1+\varepsilon_{31}/(G_2+G_1)+0 \rightarrow -\infty_1$. Hence, there is in fact no indeterminacy.

TABLE I
WORK TO DATE ON SYSTEMATIC CIRCUIT SYNTHESIS

Circuit type	Circuit details	References
Active circuit building blocks	Transconductor, impedance inverter (gyrator), simulated inductance, negative resistance, CCVS, voltage amplifier, current amplifier, positive and negative impedance converter	[27]
Active-RC sections	Sallen and Key (unity and non-unity gain), Deliyannis/Friend, Kundert/Bach, 3-integrator loop, GIC-based section	[28]
All-transistor circuits	Transconductance, current mirror	[29]
	Differential FET pair, single stage op-amp, 2-stage op-amp	[22]

new circuit solutions as needs arise. Admittance matrix stamps that are suitable starting points for circuit synthesis are given in the Appendix.

D. Circuit Modeling

Circuit modeling can have two meanings. In the first, a circuit at device level, which can be represented by its NAM, is represented instead by a simpler description, such as a port description, at the cost of some loss of accuracy. In the second, a simple ideal description of a circuit function, such as an ideal port description, is implemented by a real circuit, the NAM of which, when reduced, approximates the ideal port matrix. These operations correspond to analysis and synthesis operations, respectively, combined with some degree of approximation.

The ability of the framework we are presenting to handle analysis and synthesis and to accommodate nonideal and ideal circuit descriptions provides a potentially powerful tool for circuit modeling. We have already seen in Section VI, that we can obtain the equivalent circuit for the CCVS of Fig. 6.1(c) by application of the theorem of Section IV to the description of the CCVS equivalent circuit in Fig. 6.1(b), which although equivalent at the limit will clearly behave differently in the approach to the limit. Use of the limit variable method means that the model in Fig. 6(c) may be mathematically derived from that in Fig. 6(b). This is unlike the equivalence of Fig. 6(b) and (a), which was based on picking circuit models. Similarly, in Section VIII-B, the circuit of Fig. 8(a) was modelled exactly in Fig. 9(a) and then approximately by an ideal VCVS in Fig. 9(b). In the authors' view, a rigorous theory of modeling and model-assessment for active circuits could be developed using ∞-variables and some preliminary work on alternative ways of modeling the nullor is presented in [23].

E. Second and Third Theorems

It is convenient to refer to the arbitrary element theorem of Section IV and its corollary, the element shift theorem, collectively as a *first theorem* for matrices containing ∞-variables. Two further theorems have been presented in [30] that involve

more than one group of ∞-variables. The *second theorem* is a generalized description of the nullator-norator re-pairing principle [18] and the *third theorem* is a generalized description of the nullator-norator cloning principle [22]. The second and third theorems can play a key role in the systematic synthesis of all-transistor circuits.

IX. ZERO PIVOTS AND ZERO-VARIABLES

In this section, we consider the circumstances in which representation of a circuit can lead to a zero pivot in the NAM. The next most useful limit variable after the ∞-variable is the zero-variable (0-variable, 0_i) and we show here how it can be used to resolve the zero pivot problem.

Consider a general circuit consisting of passive elements and active elements represented in the NAM using ∞-variables. The special case where a particular node p is connected only to the norator of one nullor (∞_1) and to the nullator of another nullor (∞_2) is illustrated in Fig. 10. Row and column p of the NAM will have the form shown in (46)-LH

$$
\begin{array}{cccc}
 & & p & \\
\cdot & \cdot & \infty_2 \\
\cdot & \cdot & -\infty_2 \\
p \quad \infty_1 & -\infty_1 & 0
\end{array}
\quad \rightarrow \quad
\begin{array}{cccc}
 & & p & \\
\cdot & \cdot & \infty_2 \\
\cdot & \cdot & -\infty_2 \\
p \quad \infty_1 & -\infty_1 & 0_{pp}
\end{array}
$$

$$
\rightarrow \quad
\begin{array}{ccc}
 & p & \\
\infty_{\text{eff}} & -\infty_{\text{eff}} & \cdot \\
-\infty_{\text{eff}} & \infty_{\text{eff}} & \cdot \\
p \quad \cdot & \cdot & \cdot
\end{array}
\quad \infty_{\text{eff}} = \frac{\infty_1 \infty_2}{0_{pp}}. \tag{46}
$$

The problem of the zero pivot can be solved by replacing it by the variable 0_{pp}, as in (46)-centre, where 0_{pp} is a type of limit variable (as defined in Section III-B) called a zero-variable (0-variable) which represents the parasitic admittance y_{pp} at node p and which has a limit value of zero. Gaussian elimination leads to the last matrix in (46) which contains a set of ∞-variables that may be handled using the methods we have discussed. As well as being able to solve this problem of a zero pivot, the 0-variable can also be used to solve the problem of matrix singularity which arises due to incompatibility between a circuit and a basis that is due to the topology of the circuit rather than the values of its parameters [14].

X. CONCLUSION

We have used the concepts of port equivalence and limit variables in order to develop a framework for working with linear active circuits. The ∞-variable notation allows the nullor, all dependent sources, and the impedance converter to be symbolically represented in a nodal admittance matrix alongside representations for passive and other active elements. We have shown that, for admittance matrices with elements containing ∞-variables, special row and column operations apply that maintain port equivalence and lead to theorems for matrices containing such elements. These theorems provide the means for analysis and synthesis of circuits containing ideal active elements. Analysis of any active circuit allows its functional type be identified. The ∞-variable notation encompasses nonideal as well as ideal element and circuit behaviour and thus can play a key role in circuit modeling, optimization and design.
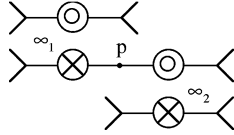
Fig. 10. Sub-circuit that leads to zero pivot in [Y].

TABLE II
STAMPS FOR NONGROUNDED DEPENDENT SOURCES

Element	Admittance matrix	Equivalent Circuit
VCVS	$\begin{array}{c} \\ k \\ l \end{array}\begin{array}{cccc} i & j & k & l \end{array}$ $\begin{bmatrix} -A_v\infty_1 & A_v\infty_1 & \infty_1 & -\infty_1 \\ A_v\infty_1 & -A_v\infty_1 & -\infty_1 & \infty_1 \end{bmatrix}$	
CCCS	$\begin{array}{c} i \\ j \\ k \\ l \end{array}\begin{array}{cc} i & j \end{array}$ $\begin{bmatrix} \infty_1 & -\infty_1 \\ -\infty_1 & \infty_1 \\ -A_i\infty_1 & A_i\infty_1 \\ A_i\infty_1 & -A_i\infty_1 \end{bmatrix}$	
CCVS	$\begin{array}{c} i \\ j \\ k \\ l \end{array}\begin{array}{cccc} i & j & k & l \end{array}$ $\begin{bmatrix} 0 & 0 & G_T & -G_T \\ 0 & 0 & -G_T & G_T \\ \infty_1 & -\infty_1 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 \end{bmatrix}$	

APPENDIX
ADMITTANCE MATRIX STAMPS FOR DEPENDENT SOURCES AND THE IMPEDANCE CONVERTER

A. General

In this Appendix, we present stamps that may be used to represent elements in an NAM (Table II), stamps that may be used to identify circuit functions when an NAM is reduced to a port matrix (Tables III to VI) and stamps that may be used as starting points for circuit synthesis (Tables VII to IX).

B. Stamps for Non-Grounded Dependent Sources

The stamps for VCVS, CCCS, and CCVS presented in Sections V and VI assumed that each input and output port included the reference node. Stamps for the general nongrounded case can easily be derived and are as shown in Table II.[5] Note that for the VCVS, the $\pm\infty_1$ elements occupy the rows and columns corresponding to the output nodes and the $\pm A_v\infty_1$ elements are in the same rows but in the columns corresponding to the input nodes. A similar rule applies for the CCCS, but the $\pm\infty_1$ elements occupy rows and columns corresponding to the input nodes.

C. Stamps Obtained by ∞-Variable Scaling

Admittance matrix descriptions for the VCVS and CCCS, which we obtained in Section V, are re-stated in Table III, where they are referred to as Type i). If in Table III we use the arbitrary scale factor theorem of Section IV-D to scale ∞_1 for the VCVS by $-A_V^{-1}$ and ∞_1 for the CCCS by $-A_I^{-1}$ then we obtain the Type ii) matrices in Table III; since these matrices have, just

---

[5]In this Appendix, all ∞-variables are denoted as ∞_1 for conformity.

TABLE III
STAMPS FOR THE VCVS AND CCCS OBTAINED BY ∞-VARIABLE SCALING

Function	Type i	Type ii
VCVS	$\begin{bmatrix} 0 & 0 \\ -A_V\infty_1 & \infty_1 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ \infty_1 & -A_V^{-1}\infty_1 \end{bmatrix}$
CCCS	$\begin{bmatrix} \infty_1 & 0 \\ -A_I\infty_1 & 0 \end{bmatrix}$	$\begin{bmatrix} -A_I^{-1}\infty_1 & 0 \\ \infty_1 & 0 \end{bmatrix}$

TABLE IV
STAMPS FOR THE IMPEDANCE CONVERTER OBTAINED BY ∞-VARIABLE SCALING

Type i	Type ii
$\begin{bmatrix} A_V A_I\infty_1 & -A_I\infty_1 \\ -A_V\infty_1 & \infty_1 \end{bmatrix}$	$\begin{bmatrix} A_I\infty_1 & -A_V^{-1}A_I\infty_1 \\ -\infty_1 & A_V^{-1}\infty_1 \end{bmatrix}$

Type iii	Type iv
$\begin{bmatrix} A_V\infty_1 & -\infty_1 \\ -A_V A_I^{-1}\infty_1 & A_I^{-1}\infty_1 \end{bmatrix}$	$\begin{bmatrix} \infty_1 & -A_V^{-1}\infty_1 \\ -A_I^{-1}\infty_1 & A_V^{-1}A_I^{-1}\infty_1 \end{bmatrix}$

like the Type i) matrices, just two elements and two parameters, they form a canonic pair of matrices for the VCVS and CCCS. The admittance matrix description for the impedance converter, which we obtained in Section VII, is re-stated as Type i) in Table IV. As for the dependent sources, equivalent matrices may be obtained by scaling of ∞_1, and use of scaling factors A_V^{-1}, A_I^{-1} and $A_V^{-1}A_I^{-1}$ leads to the three alternative matrices shown in Table IV as Types ii), iii), and iv), which have, like the Type i) matrix, just three parameters and which may therefore be regarded as forming the canonic set.

The Type i) matrices in Tables III and IV have natural equivalent circuits already given in Figs. 5 and 7. The Type iv) impedance converter matrix also has a simple equivalent circuit which is the same as the Type i) circuit in Fig. 7 but with terminals 1 and 2 interchanged and A_V and A_I replaced by A_V^{-1} and A_I^{-1}.

D. Stamps in Transfer Function Form

In the admittance matrices for VCVS and CCCS in Table III, we can replace the gains, A_V and A_I, by rational functions, N/D, where N and D are transfer function numerator and denominator, respectively. This leads to the Type i) and ii) admittance matrices in Table V. Scaling the parameter ∞_1 in the Type i) functions in Table V for both VCVS and CCCS by $\pm D/Q$ or in the Type ii) functions by $\pm N/Q$, where Q is an arbitrary function, yields the same matrix and this is shown as Type iii) in Table V. The Type iii) matrices like the Type i) and Type ii) matrices have only two nonzero 2-port admittance parameters. Since the transfer function A_V for the VCVS case is given by $-y_{21}/y_{22}$, then the three matrices in Table A.4 represent the three logical cases where, N and D are in y_{21}, N and D are in y_{22} and N and D are divided between y_{21} and y_{22}. A similar statement applies to the CCCS matrices, but for y_{11} and y_{21}. Hence, it is appropriate to regard each set of three matrices in

TABLE V
STAMPS FOR CIRCUITS WITH VCVS AND CCCS TRANSFER FUNCTIONS

Function	Type i	Type ii	Type iii
VCVS	$\begin{bmatrix} 0 & 0 \\ -\dfrac{N}{D}\infty_1 & \infty_1 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ \infty_1 & -\dfrac{D\infty_1}{N} \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ -\dfrac{N\infty_1}{Q} & -\dfrac{D\infty_1}{Q} \end{bmatrix}$
A_V	N/D	N/D	$-N/D$
CCCS	$\begin{bmatrix} \infty_1 & 0 \\ -\dfrac{N}{D}\infty_1 & 0 \end{bmatrix}$	$\begin{bmatrix} -\dfrac{D\infty_1}{N} & 0 \\ \infty_1 & 0 \end{bmatrix}$	$\begin{bmatrix} -\dfrac{D\infty_1}{Q} & 0 \\ -\dfrac{N\infty_1}{Q} & 0 \end{bmatrix}$
A_I	N/D	N/D	$-N/D$

TABLE VI
STAMPS FOR THE IMPEDANCE CONVERTER IN TRANSFER FUNCTION FORM

Type i	Type ii
$\begin{bmatrix} \dfrac{N_V N_I \infty_1}{D_V D_I} & -\dfrac{N_I \infty_1}{D_I} \\ -\dfrac{N_V \infty_1}{D_V} & \infty_1 \end{bmatrix}$	$\begin{bmatrix} \dfrac{N_I \infty_1}{D_I} & -\dfrac{D_V N_I \infty_1}{N_V D_I} \\ -\infty_1 & \dfrac{D_V}{N_V}\infty_1 \end{bmatrix}$

Type iii	Type iv
$\begin{bmatrix} \dfrac{N_V \infty_1}{D_V} & -\infty_1 \\ -\dfrac{N_V D_I \infty_1}{D_V N_I} & \dfrac{D_I \infty_1}{N_I} \end{bmatrix}$	$\begin{bmatrix} \infty_1 & -\dfrac{D_V \infty_1}{N_V} \\ -\dfrac{D_I \infty_1}{N_I} & \dfrac{D_V D_I}{N_V N_I}\infty_1 \end{bmatrix}$

Type v
$\begin{bmatrix} \dfrac{N_V N_I \infty_1}{Q_1 Q_2} & -\dfrac{D_V N_I \infty_1}{Q_1 Q_2} \\ -\dfrac{N_V D_I \infty_1}{Q_1 Q_2} & \dfrac{D_V D_I \infty_1}{Q_1 Q_2} \end{bmatrix}$

TABLE VII
EXPANDED STAMPS FOR THE VCVS AND CCCS

Type	VCVS $A_V = A$	CCCS $A_I = A$	A
i	$\begin{bmatrix} 0 & 0 & 0 \\ 0 & \infty_1 & -\infty_1 \\ -N & 0 & D \end{bmatrix}$	$\begin{bmatrix} \infty_1 & 0 & 0 \\ 0 & 0 & -N \\ -\infty_1 & 0 & D \end{bmatrix}$	$\dfrac{N}{D}$
ii	$\begin{bmatrix} 0 & 0 & 0 \\ \infty_1 & 0 & -\infty_1 \\ 0 & -D & N \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & -D \\ \infty_1 & 0 & 0 \\ -\infty_1 & 0 & N \end{bmatrix}$	$\dfrac{N}{D}$
iii	$\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \infty_1 \\ -N & -D & Q \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & -D \\ 0 & 0 & -N \\ \infty_1 & 0 & Q \end{bmatrix}$	$-\dfrac{N}{D}$
iv	$\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \infty_1 & -\infty_1 \\ -N_1 & -D_1 & P_1 & 0 \\ -N_2 & -D_2 & 0 & P_2 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & -D_1 & -D_2 \\ 0 & 0 & -N_1 & -N_2 \\ \infty_1 & 0 & P_1 & 0 \\ -\infty_1 & 0 & 0 & P_2 \end{bmatrix}$	$\dfrac{N_1 P_2 - N_2 P_1}{D_2 P_1 - D_1 P_2}$

Table V as a canonic set of admittance matrices for circuits with given voltage and current transfer function numerator and denominator functions. Note that in the Type iii) expansions we have changed the sign of the numerator function N in the matrix and in the transfer function expression.

For the impedance converter with voltage and current gain expressed as the rational functions, $A_V = N_V/D_V$ and $A_I = N_I/D_I$ the four canonic admittance matrices in Table IV lead to the Type i)–iv) matrices in Table VI. By carrying out several different forms of scaling of the ∞-variable ∞_1, such as scaling by $D_V D_I/(Q_1 Q_2)$ in the Type i) matrix, we obtain the Type v) matrix in Table VI. So for the impedance converter, the set of canonic admittance matrices at the transfer function numerator and denominator level consists of five matrices.

E. Expansion of Transfer Function Forms of Stamps for VCVS, CCCS and Impedance Converter

Pivotal expansion may be used to expand the 2×2 admittance matrix representations for the VCVS and CCCS in Table V and it leads to the Type i), ii), and iii) 3×3 matrices shown in Table VII. These expansions effectively eliminate products and

quotients of terms. All elements in Table VII must have the dimensions of admittance; so all elements other than the ∞-variables, $\pm\infty_1$, are in fact divided by a common admittance function, which is arbitrary as far as the transfer function is concerned and which is not shown for clarity. The expansions in Table VII may be checked by applying Gaussian elimination to the expanded matrices.[6]

In the Type iii) VCVS expansion in Table VII, the elements ∞_1 and Q have been involved in expansion of both the N and the D terms in the Type iii) matrix in Table V. These N and D terms can alternatively be expanded into separate rows and columns (3 and 4) as follows:[7]

$$\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \infty_1 & -\infty_1 \\ -N & 0 & Q & 0 \\ 0 & -D & 0 & Q \end{bmatrix}. \qquad (47)$$

If y_{32} and y_{41} elements were present in this matrix, Gaussian elimination shows that they would contribute to the transfer functions, in which case the Q elements are no longer arbitrary and the transfer functions assume the form shown as the Type iv) expansions in Table VII. Due to the $\pm\infty_1$ terms, P_1 may be expressed as a sum of two terms, one term of which may be moved to the 3, 4 position for the VCVS function or to the 4,3 position for the CCCS function; therefore there is no loss of generality if we set y_{34} and y_{43} to zero in both Type iv) expansions, as shown. Degrees of freedom in the choice of signs in the elements in Table VII have been used to associate positive signs with diagonal elements and negative signs with off-diagonal elements without loss of generality.

In the case of the Type i) and ii) expansions in Table VII, it is possible to interchange a $-\infty_1$ element in column 3 with a $-N$ or

---

[6]It might be thought that Gaussian elimination leads to some indeterminate elements. That this is not the case may be seen by writing out the element expressions and taking ∞_1 out as a common factor.

[7]We have negated N in the matrix and in the transfer function expression.

$-D$ element in row 3 or vice versa, but this leads to two ∞_1 elements which are neither on the same row nor in the same column; since such alternatives have no correspondence to a physical element, they can be ignored. It may be shown that the Type i) and Type ii) expansions for the VCVS and CCCS are related by terminal interchange transformations;[8] nevertheless, it seems sensible to regard them as separate expansions at this stage.

Note that all of the expansions for the VCVS in Table VII imply the presence of a grounded norator at node 2 (by virtue of the ∞_1 elements in row 2) and all of the expansions for CCCS imply the presence of a grounded nullator at node 1 (∞_1 elements in column 1). For the VCVS case, the intrinsic nullator connection is from node 3 to the following nodes: Type i)—to the output node 2; Type ii)—to the input node 1; Type iii)—to the reference node; Type iv)—to a fourth node (i.e., no constraint). Since the intrinsic nullator may not be connected between nodes 1 and 0, 1 and 2, 2 and 0, because these connections restrict the transfer function that can be realized, this suggests that the four expansions in Table VII form a logically complete set. Constraints on norator connections for the CCCS expansions in Table VII are similar to those on the nullator in the VCVS expansions.

The Type iv) expansions in Table VII are more general than the others; however, they do imply that the circuit realising the transfer function has at least 4 nodes rather than 3, which could be a restriction. It is possible to derive the other expansions from the Type iv) expansion as special cases. For instance, by setting $N_2 = D_2 = 0$, we obtain the Type iii) expansions. To derive the Type i) expansions, we set $D_1 = N_2 = 0$ and $D_2 = P_2$; we then denote N_1 by N and P_1 by D. To derive the Type ii) expansions, we set $N_1 = D_2 = 0$ and $N_2 = P_2$; we then denote D_1 by D and P_1 by N. Nevertheless, it is recommended to regard all four as the set of expansions. Note that, in the Type i) and ii) VCVS and CCCS expansions in Table VII, the element shift theorem provides degrees of freedom in that the 3,3 diagonal element may be expressed as the sum of two parts and one part may be moved to another row or column by virtue of the intrinsic $\pm\infty_1$ elements.

Pivotal expansion of the 2×2 admittance matrix representations in Table VI for the impedance converter leads to the expansions in Table VIII. In the case of expansion v), both its nullator and its norator are connected to the reference node. In expansions i)–iv) the nullor is fully floating.

F. Element Stamps Without ∞-Variables

We consider first the dependent sources, starting with the CCVS. The 2×2 admittance matrix of (36)-RH may be expanded using pivotal expansion to obtain a 3×3 matrix, after first replacing the element ∞_1 by 0_1^{-1}, where 0_1 is a 0-variable with dimensions of impedance

$$
\begin{bmatrix} 0 & R_T^{-1} \\ \infty_1 & 0 \end{bmatrix} = \begin{bmatrix} 0 & R_T^{-1} \\ 1/0_1 & 0 \end{bmatrix}
$$
$$
= \begin{bmatrix} 0 & R_T^{-1} & 0 \\ 0 & 0 & Q_2 \\ Q_1 & 0 & -Q_1Q_20_1 \end{bmatrix}. \quad (48)
$$

---

[8]For the VCVS, descriptions Type i) and ii) are related by interchange of column 1 and 2 and interchange of N and D, i.e., inversion of the transfer function; the circuits they lead to are related by a terminal interchange transformation [31]. For the CCCS, descriptions Type i) and ii) are related by interchange of row 1 and 2 and interchange of N and D; the circuits they lead to are also related by a terminal interchange transformation.

TABLE VIII
EXPANDED STAMPS FOR THE IMPEDANCE CONVERTER

Type i	Type ii
$\begin{bmatrix} 0 & 0 & -N_I & 0 \\ 0 & \infty_1 & 0 & -\infty_1 \\ 0 & -\infty_1 & D_I & \infty_1 \\ -N_V & 0 & 0 & D_V \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & -N_I & 0 \\ -\infty_1 & 0 & 0 & \infty_1 \\ \infty_1 & 0 & D_I & -\infty_1 \\ 0 & -D_V & 0 & N_V \end{bmatrix}$

Type iii	Type iv
$\begin{bmatrix} 0 & -\infty_1 & 0 & \infty_1 \\ 0 & 0 & -D_I & 0 \\ 0 & \infty_1 & N_I & -\infty_1 \\ -N_V & 0 & 0 & D_V \end{bmatrix}$	$\begin{bmatrix} \infty_1 & 0 & 0 & -\infty_1 \\ 0 & 0 & -D_I & 0 \\ -\infty_1 & 0 & N_I & \infty_1 \\ 0 & -D_V & 0 & N_V \end{bmatrix}$

Type v
$\begin{bmatrix} 0 & 0 & -N_I & 0 \\ 0 & 0 & D_I & 0 \\ 0 & 0 & Q_1 & \infty_1 \\ -N_V & D_V & 0 & Q_2 \end{bmatrix}$

TABLE IX
STAMPS WITHOUT ∞-VARIABLES FOR DEPENDENT SOURCES AND THE IMPEDANCE CONVERTER

CCVS	VCVS (type v)	CCCS (type v)	Impedance converter (type vi)
$\begin{bmatrix} 0 & R_T^{-1} & 0 \\ 0 & 0 & Q_2 \\ Q_1 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & Q \\ -N & -D & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & -D \\ 0 & 0 & -N \\ Q & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & N_I \\ 0 & 0 & -D_I \\ -N_V & D_V & 0 \end{bmatrix}$
	$A_V = -\dfrac{N}{D}$	$A_I = -\dfrac{N}{D}$	$A_V = \dfrac{N_V}{D_V}, \; A_I = \dfrac{N_I}{D_I}$

In the 3×3 expanded matrix, Q_1 and Q_2 are arbitrary admittance functions. The $-Q_1Q_20_1$ element in (48)-RH may be set to zero to yield the matrix in the first column of Table IX. In a similar way, element expansions for the VCVS and the CCCS may be derived by pivotal expansion of the Type iii) 2×2 matrices in Table V and they are also shown in Table IX, where they are designated Type v). The Type v) 2×2 admittance matrix for the impedance converter in Table VI may be expanded avoiding ∞-variables

$$
\begin{bmatrix} \frac{N_V N_I}{Q_1 Q_2 0_1} & -\frac{D_V N_I}{Q_1 Q_2 0_1} \\ -\frac{N_V D_I}{Q_1 Q_2 0_1} & \frac{D_V D_I}{Q_1 Q_2 0_1} \end{bmatrix} = \begin{bmatrix} 0 & 0 & N_I \\ 0 & 0 & -D_I \\ -N_V & D_V & Q_1 Q_2 0_1 \end{bmatrix} \quad (49)
$$

where $0_1 = 1/\infty_1$. The term $Q_1 Q_2 0_1$ may be set to zero to give the matrix in the last column in Table IX.

Matrices with zero pivots, such as those in Table IX may appear similar to MNA matrices. However, in Table IX, the third row and column relate strictly to node 3 of the circuit and define relationships between dependent current (I_3), independent voltage (V_3) and other variables in the way that is usual for admittance matrices. In our formulation, the N, D and Q matrix elements in Table IX are viewed as functions that can be expanded into new rows and columns in order to synthesise a circuit.

The existence of the finite matrices in Table IX proves that circuits that are said to not possess admittance matrices (in the conventional sense) can still be members of the class of circuits that are realizable as interconnections of transconductors with finite transconductances.

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