3-D Printed Rectangular Waveguide 123–129 GHz Packaging for Commercial CMOS RFICs

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***Abstract*— This work demonstrates the hybrid integration of a complementary metal–oxide–semiconductor (CMOS) radio frequency integrated circuit (RFIC) into a host 3-D printed metal-pipe rectangular waveguide (MPRWG). On-chip Vivaldi antennas are used for TE_{10}-to-thin-film microstrip (TFMS) mode conversion. Our packaging solution has a combined measured insertion loss of only 1 dB/transition at 126 GHz. This unique packaging and interconnect solution opens up new opportunities for implementing low-cost subterahertz (THz) multichip modules.**

***Index Terms*— 3-D printing, additive manufacturing, complementary metal–oxide–semiconductor (CMOS), interconnects, millimeter wave, mode conversion, packaging, radio frequency integrated circuit (RFIC), rectangular waveguide, Vivaldi antenna, WR-6.**

I. Introduction

ADDITIVE manufacturing using polymer-based 3-D printing has demonstrated its potential for microwave-to-terahertz (THz) applications as an emerging technology. For example, in 2015, we reported the first 3-D printed metal-pipe rectangular waveguide (MPRWG) thru line and filter components at X-band (8–12 GHz) and W-band (75–110 GHz) [1]. Since then, many other low-cost, high-performance passive components have been demonstrated with polymer-based 3-D printed MPRWGs. However, to date, there are very few examples of hybrid integration of active devices or integrated circuits (ICs) with 3-D printed host waveguides.

MPRWGs are commonly used in very high-performance, front-end microwave and millimeter-wave subsystems. While discrete semiconductor devices (e.g., Gunn diode sources, Schottky junction detectors, and p-i-n diode switches) are routinely embedded within host MPRWGs, the packaging of ICs is more problematic. For example, at microwave frequencies, the cross-sectional dimensions of the MPRWG can be much greater than the size of the IC, thus requiring additional off-chip transition design solutions. At (sub-)millimeter-wave frequencies, the converse can be true, resulting in no obvious packaging solutions. More importantly, wire-based chip interconnects work best up to *ca.* 30 GHz with bond wires and *ca.* 100 GHz with flip-chip bonding, due to the unwanted effects of the associated parasitics.

Existing wireless-based solutions at upper millimeter-wave frequencies (i.e., above *ca.* 100 GHz) employ electromagnetic (EM) coupling via on-chip resonators or impedance-matched field probes, which inherently have a relatively narrow bandwidth and are not compatible with commercial foundry silicon-based radio frequency ICs (RFICs) and GaAs-based monolithic microwave ICs (MMICs).

The concept of RF EM-field coupling between a host MPRWG and its packaged IC was first introduced in 1998 for implementing THz multichip modules (T-MCMs) [2]. Otter and Lucyszyn [3] demonstrated the first T-MCM, incorporating 3-D printed MPRWGs with integrated high-resistivity silicon (HRS) implants and optoelectronic modulating laser diodes at 500 GHz.

Lozar et al. [4] demonstrated electric (E)-field probe coupling between a machined MPRWG and GaAs-based MMIC thru line (grounded-coplanar waveguide) at D-band (110–170 GHz). Skaik et al. [5] also demonstrated E-field probe coupling into a GaAs MMIC at both V-band (50–75 GHz) and D-band with 3-D printed MPRWGs; unfortunately, no waveguide-to-chip interface characterization was undertaken. With all these approaches, split-block designs were adopted [3], [4], [5].

In this letter, we demonstrate novel EM-field coupling, using two on-chip Vivaldi antennas, between a 3-D printed host MPRWG and its packaged D-band RFIC thru line [on-chip thin-film microstrip (TFMS)] fabricated using the GlobalFoundries[1] 45-nm RF HRS-on-insulator (GF 45RFSOI with Option 18) complementary metal–oxide–semiconductor (CMOS) technology platform. As in our previous work [3], an H-plane split-block design is adopted, and a masked stereolithography apparatus (MSLA) 3-D printer is used [6] to

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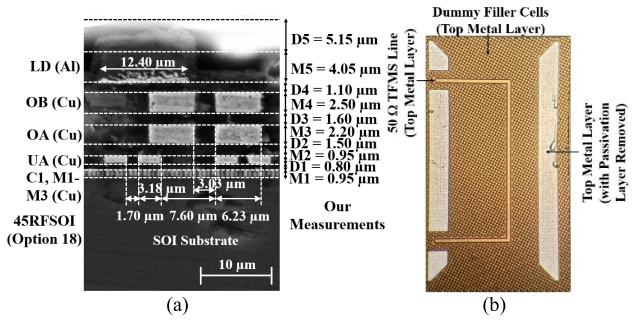

Fig. 1. GlobalFoundries 45-nm CMOS RFIC. (a) SEM and (b) optical microphotograph showing 20-µm-wide 50-Ω TFMS line.

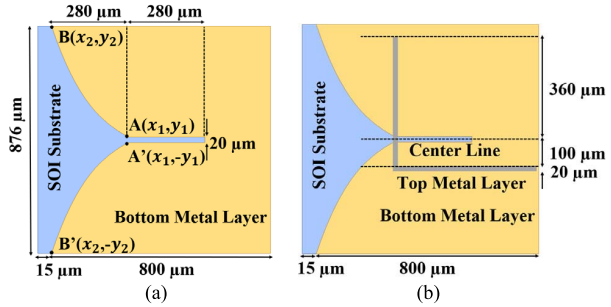

Fig. 2. On-chip Vivaldi antenna design. (a) Ground (bottom metal layer, our M1) and (b) with TFMS line (top metal layer, our M5).

manufacture a standard WR-6 waveguide before being copper electroplated.

II. Waveguide-to-Chip Interface Design

We recently introduced an active D-band 65-nm CMOS RFIC single-stage amplifier that exhibits a measured gain of 5.1 dB using standard on-wafer probing techniques (i.e., with unpackaged chips) [7]. For chip packaging employing a 3-D printed host MPRWG, a proof of principle for TE_{10}-to-TFMS mode conversion is demonstrated, using on-chip TFMS and two back-to-back Vivaldi antennas [8]. A scanning electron microscopy (SEM) image showing the cross-sectional view of the front-side passive layer structure is shown in Fig. 1(a). The optical microphotograph of the plane view for the 322 × 876 × 1630 µm test chip is shown in Fig. 1(b).

Each on-chip Vivaldi antenna employs a fin-line transition, as envisaged for the T-MCM [2], not demonstrated until now. The design for this on-chip solution is shown in Fig. 2.

With our Vivaldi antenna, A(x_1, y_1) and B(x_2, y_2) are the two endpoints associated with the generic exponential taper curve expressed by

$$y = C_1 e^{\alpha x} + C_2 \tag{1}$$

where the exponential factor $\alpha = 6$ [obtained after parameter tuning in High-Frequency Structure Simulator (HFSS), for optimal impedance matching within the available limitations of chip real estate], while C_1 and C_2 are obtained from

$$C_1 = \frac{y_2 - y_1}{e^{\alpha x_2} - e^{\alpha x_1}} \quad \text{and} \quad C_2 = \frac{y_1 \cdot e^{\alpha x_2} - y_2 \cdot e^{\alpha x_1}}{e^{\alpha x_2} - e^{\alpha x_1}}. \tag{2}$$

For our D-band demonstrator, the host MPRWG is based on the WR-6 standard, as illustrated in Fig. 3, having internal cross-sectional dimensions $a \times b$ of 1651 × 826 µm. The H-plane split-block waveguide design [6] is chosen for chip

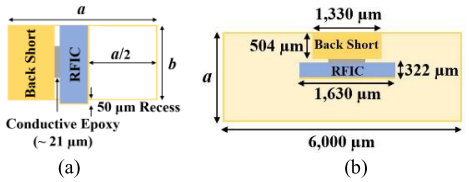

Fig. 3. Internal illustrations of packaged RFIC for 126-GHz operation showing chip side views with HRS dielectric substrate (blue) and top metallization layers (yellow). (a) End and (b) plan.

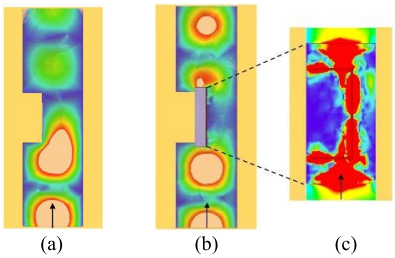

Fig. 4. Simulated E-field distributions within the waveguide at 126 GHz. (a) Plan view without RFIC, (b) plan view with RFIC, and (c) side view showing TE_{10}-to-TFMS-to-TE_{10} mode conversions.

packaging. The RFIC is internally mounted in the E-plane of the waveguide with its Vivaldi taper located at the center. A back short provides mechanical support and blocks backside leakage of radiation.

All simulations are undertaken with commercial 3-D full-wave EM simulation software, using Ansys HFSS. The simulated E-field distributions at 126 GHz are shown in Fig. 4. Fig. 4(a) and (b) shows the E-field distributions without and with RFIC mounted within the waveguide, respectively. Fig. 4(c) shows the E-field distribution on top of the RFIC. From Fig. 4(a), it can be seen that most of the incident energy is reflected at the back short. Conversely, from Fig. 4(b) and (c), the waveguide's incident TE_{10} mode is coupled into the on-chip TFMS line by the Vivaldi antenna, with most of the incident energy being transmitted thru the waveguide.

Two-dimensional periodic arrays of dummy filler cells are found with CMOS RFICs [9]; these can be seen in Fig. 1 on all upper metal layers (our M2–M5). With regard to the metal-plated waveguide walls, it has been determined that the average radius of hemispherical protrusions is 3.7 µm, having an average separation distance of 17 µm, giving an RMS profile roughness of $R_q = 1.41$ µm. To avoid EM computation overloading, equivalent dummy-free layer substitution is adopted (using foundry design rules) and with zero surface roughness.

III. Fabrication

The MSLA 3-D printer used in this work is the Phrozen Sonic Mini 4K, with a quoted 35-µm pixel resolution in the x–y build plane and employing a 20-µm layer thickness. In theory, an E-plane split will have less loss attributed to radiation leakage with a machined waveguide. However, with 3-D printing for D-band applications, we have previously demonstrated low leakage that works with the H-plane solution, due to the easier removal of resin residue within the wider trough and easing of alignment tolerances in assembly [6]. All pixel-based 3-D printers, which include MSLA, suffer from quantization problems due to the introduction of registration errors. As a result, for this work, we employed our multistep

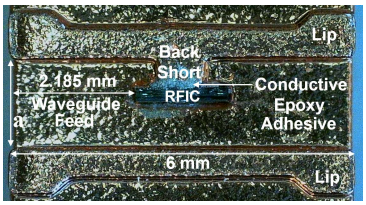

Fig. 5. Microphotograph of the integrated RFIC assembled into the lower part of the rectangular waveguide packaging (plan view).

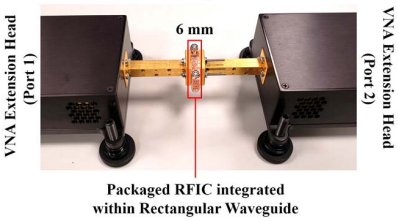

Fig. 6. D-band test setup for the packaged RFIC.

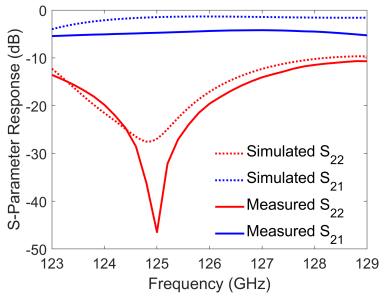

Fig. 7. Measured *S*-parameter responses with RFIC.

quantization predistortion methodology to correct for registration errors [6].

The 3-D printed parts are first electroless plated with a thin layer of nickel. This is followed by electroplating a 50-μm layer of copper, ensuring that the corners are sufficiently plated [6].

For assembly, MG Chemical 8331 slow cure silver conductive epoxy adhesive is applied between the RFIC and back short, as shown in Fig. 5.

IV. Measurements and Results

Measurements were made at the U.K.'s National Physical Laboratory, using the Keysight Technologies PNA-X N5247B vector network analyzer and VDI WR-6.5 frequency extension heads. The packaged RFIC test setup is shown in Fig. 6.

Our equivalent simulation model is based on a single value for the effective dielectric constant of 5.2 that represents all the layers (including the equivalent dummy-free layer) for the CMOS RFIC. The simulated and measured results are shown in Fig. 7. With the packaged RFIC, the minimum measured insertion loss is ∼4 dB at 126 GHz. The measured return loss is better than 10 dB at all frequencies across our 5% fractional bandwidth from 123 to 129 GHz.

Seo et al. [9] investigated "dummy modeling" for 65-nm CMOS RFICs having different area fill ratios; the most significant effect is to increase the distributed capacitance associated with dummy-prefilled on-chip TFMS lines.

In addition, Seo et al. [9] measured an on-chip TFMS line loss of 2 dB/mm at 140 GHz for their 65-nm CMOS RFICs. As a result, for our 1.04-mm on-chip TFMS lines, it is reasonable to expect an associated loss of 2 dB. Therefore, the combined losses associated with two waveguide feeds (mainly attributed to their surface roughness) and two MPRWG-to-chip interfaces are approximately 2 dB (i.e., ∼1 dB/transition) at 126 GHz.

TABLE I
Comparison With Other Works

Band	Frequency Range (GHz)	Pick-up Solution	WG-to-Tx Line Transition	Transition Loss (dB)	Year	Ref.
W	67-110	CMOS RFIC Patch	MPRWG to MS	0.35	2015	[10]
W	72-95	PCB Transformer	MPRWG to MS	0.8	2017	[11]
W	88.5-103	PCB Patch	MPRWG to MS	0.5	2012	[12]
D	110-170	MMIC E-probe	MPRWG to stripline	N.A.	2017	[13]
D	120-130	GaAs MMIC E-probe	MPRWG to MS	N.A.	2022	[5]
D	123-129	CMOS RFIC Vivaldi	MPRWG to TFMS	1	2022	**This work**
D	124-161	GaAs MMIC Patch	MPRWG to MS	0.8	2021	[14]
G	140-220	Silicon RFIC E-probe	N.A.	1	2020	[15]
Y	340-380	InP MMIC Dipole	MPRWG to CPW	1	2009	[16]

PCB: printed circuit board; WG: waveguide; Tx: transmission; MS: microstrip; CPW: coplanar waveguide; N.A.: not available.

An exhaustive literature review has been undertaken of W-, D-, G-, and Y-band waveguide-to-chip interconnects, and the results are now shown in Table I. As seen in Table I, there are very few examples of actual waveguide-to-chip interfaces (Aljarosha et al. [11] and Tong and Stelzer [12] use PCBs at W-band, instead of a chip, but these are included for completeness).

V. Conclusion

In this letter, a new upper millimeter-wave packaging solution for commercial CMOS RFICs has been demonstrated experimentally. Here, EM coupling into and out of a chip replaces conventional wire-based solutions. Our first prototype demonstrator exhibits a combined insertion loss of only 1 dB/transition at 126 GHz. This opens up sub-THz applications for an individually packaged silicon-based RFIC or GaAs-based MMIC, as well as being able to implement complete multichip modules.

We have demonstrated that on-chip Vivaldi antennas work well at D-band with HRS used in the commercial GF 45RFSOI process. In contrast, EM simulations confirm that these antennas are inefficient with standard commercial low-resistivity silicon processes, which are generally limited to microwave frequencies of operation.

Our unique hybrid integration approach combines low-cost commercial CMOS RFIC technology with a novel ultralow-cost 3-D printed packaging and interconnect solution for next-generation high-performance, broadband applications operating at millimeter-wave frequencies, including 6G mobile communications base stations, standoff detection imaging systems, and phased-array radars.

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