Design and Control Optimisation of a Novel Bypass-embedded Multilevel Multicell Inverter for Hybrid Electric Vehicle Drives

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Abstract—A novel bypass-embedded multilevel multicell inverter is proposed with manipulation of bidirectional flow of currents targeting electric motor drives and regenerative braking (battery recharging) for hybrid electric vehicles. To balance switching losses, maximise DC supply utilisations, balance the state of charge, and minimise total harmonic distortions, the inverter control method is optimised by incorporating phase disposition PWM with variable carrier frequency, third harmonic injection, as well as carrier reordering and reduction schemes. The proposed control scheme is investigated on an 11-level inverter for motor drives of a parallel hybrid electric vehicle with regenerative braking capability. The total harmonic distortion is 1.23% for line voltage, and 1.04% for stator current without filtering networks, i.e. a comparable performance to the states of the arts.

Keywords—bypass circuit, cascaded H-bridge, motor drives, multilevel converter, power inverter, total harmonic distortion

I. INTRODUCTION

Motor drives of hybrid electric vehicles (HEV) advance continuously with the development of cascaded H-bridge (CHB) multilevel multicell inverters (MMI) [1], due to the advantages over the conventional two-level inverters, e.g. reduced switching losses, a lower rate of change in voltage, and less susceptible to electro-magnetic interference [2]. However, the MMI does exhibit three main drawbacks [3], i.e. the costs of a large number of switching devices, the complexity in the driving circuit, and the vulnerability of system failures due to this complexity.

To be more specific for the HEV drives, the more and more stringent requirements in the fuel economy and fault tolerance challenge the current status of MMC in terms of the control modules design. States-of-the-arts fault-tolerance bypass techniques reported so far [4][5] are mainly for remedial purpose, while few study to the best of our knowledge has concerned with the manipulation of the bidirectional current flow for battery recharging during the regenerative braking. This paper bridges the gap by tailoring the conventional Phase Disposition Pulse Width Modulation (PD-PWM) with a novel bypass design (reported in section II) for achieving both the fault tolerance and the battery recharging functionalities, with multi-objective optimisations carried out in section III and the results analysed in section IV.

II. PD-PWM WITH BYPASS DESIGN

A. CHB MMI and Control Modules Design

As illustrated in Fig. 1, an 11-level MMI with 5 symmetric CHB modules (each with a 48 V battery supply) per phase is modelled using MATLAB/Simulink, with one of the bridge

modules shown in Fig. 2. To synthesise a 240 V phase-to-neutral voltage output in a staircase waveform, an output of 0 V for each bridge module is required for a certain time in each clock cycle. To realise this, conventional methods (bypass-free) are based on signals 1 and 2 simultaneously be low (i.e. 0 in Fig. 2), hence shutting off all the MOSFETs and blocking the current through the module, which however contradicts with the same current implication of all CHB modules connected in series. To address this, we propose a novel solution by adding a “bypass enable” signal (see the blue block in Fig. 2) for the upper MOSFETs of each module, i.e. the control signals for each phase are constituted by PD-PWM signals together with the bypass enable signals as implemented in Fig. 3 using NOT gates. Level of the enable signal is dictated by the modulation signal, i.e. given either signal 1 or 2 is in high level, the current circulates without problems, thus the enable signal is off. The enable signal kicks in and goes high when signals 1 and 2 are both in low levels (see the case in Fig. 3), MOSFET 1 is turned on allowing the positive current flow in short circuit through the body diode of MOSFET 2 (see Fig. 2).

Fig. 1. Schematic of an 11-level MMI with 5 CHB.

Fig. 2. The proposed bypass control in each H-bridge.

Fig. 3. PD-PWM with bypass control (implemented with NOT gates to generate enable signals).

B. Simulation Results

As verified in Fig. 4 the simulated output voltage of each CHB module versus time for phase A, as well as in Fig. 5 the output phase-to-neutral voltages for each phase, the proposed bypass-embedded design functions properly for the voltage synthesis in a sinusoidal waveform. It is worth noting that during the regenerative braking (negative current recharging batteries), the inverter control operation is analogous, i.e. MOSFET 2 and the body diode of MOSFET 1 develop a path along which the negative current flows. In a summary, the proposed bypass arrangement enables the CHB MMI to manipulate the bidirectional current circulation, hence highly suitable for the motor drives and regenerative braking in the HEV applications.

Fig. 4. Simulated output voltages of bridges 1-5 for phase A.

Fig. 5. Simulated phase-to-neutral voltages.

III. MULTI-OBJECTIVE OPTIMISATION

Note that only the upper MOSFETs are in use for the bypass mode (Fig. 2), resulting in higher switching losses and compromised lifespan as compared with the lower switches. A programmed selector for the loss equalisation is proposed in Fig. 6, with the upper switches in use only for the first half cycle, while the lower switches put into operation for the second half cycle. Given all the H-bridges share a same carrier frequency, the switching losses will be unequal among the bridges. As sinusoidal reference intersects with the top and the bottom carriers more frequently than the intermediate carriers, the switching losses increase accordingly from the centre carrier to both sides, i.e. bridge 1 (or 5) > bridge 2 (or 4) > bridge 3 as observed in Fig. 4 above.

To balance the switching losses for a longer service life and reduced maintenance costs, a hybrid carrier frequency scheme is proposed in Fig. 7, with top and bottom carriers' frequency (300 Hz) smaller than that of the middle one (600 Hz). As also shown in Fig. 4b, the PD-PWM is further optimised by incorporating the carrier reduction (to only 5 carriers per phase) and reordering methods (for balancing the state of charge between batteries), and the third harmonic injection (for maximising the DC supply utilisation rate).

Fig. 6. Optimised bypass control design using a programmed selector.

Fig. 7. Optimised hybrid PD-PWM with variable carrier frequencies.

IV. OPTIMISATION RESULTS AND ANALYSIS

With the proposed hybrid control schemes optimised, the output line voltages of the inverter are presented in Fig. 8 below, with multilevel waveforms approaching sinusoidal without filtering. The Fast Fourier Transform (FFT) analysis is performed for the line voltage (Fig. 9) and the stator current (Fig. 10), with the total harmonic distortions (THD) of 1.23% and 1.04% respectively, and the DC voltage utilisation rate of 81.6%, all demonstrating a decent performance improvement at a reduced cost as compared with the up-to-date documentations [5–7].

The novel bypass-embedded concept proposed in this work is not restricted for the PD-PWM, but could easily branch out into other PWM techniques and inform future research directions and optimisation opportunities both numerically and experimentally [8]–[33], notably the state-of-the-art windowed PWM [33] for traction drives.

Fig. 8. Results of output line voltages.

Fig. 9. FFT analysis of line voltage.

Fig. 10. FFT analysis of stator current.

V. CONCLUSION

A novel and cost-effective bypass-embedded control scenario is proposed and optimised for a cascaded H-bridge multilevel multicell inverter targeting the motor drives of hybrid electric vehicles. Incorporating the proposed bypass circuits with the phase-disposition PWM, third-harmonic injection, carrier reordering and reduction strategies, the 11-level inverter is demonstrated with a negligible THD in the output voltages (1.23%) and currents (1.04%), meanwhile a high utilisation rate of DC supply (81.6%), a balanced switching loss between switches, a minimum quantity of carriers, and a balanced state of charge between battery modules. The proposed solution is important for answering the UK's energy challenges [34][35] in the electrification of transportation towards the strategic importance [36] in electric mobility [30] and a greener future [37].

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