Laser-Assisted Bumping for Flip Chip Assembly

Changhai Wang and Andrew S. Holmes

Abstract—A novel laser-assisted chip bumping technique is presented in which bumps are fabricated on a carrier and subsequently transferred onto silicon chips by a laser-driven release process. Copper bumps with gold bonding layers and intermediate nickel barriers are fabricated on quartz wafers with pre-deposited polyimide layers, using UV lithography and electroplating. The bumps are thermosonically bonded to their respective chips and then released from the carrier by laser machining of the polyimide layer, using light incident through the carrier. Bumps of 60 to 85 μm diameter and 50 μm height at a pitch of 127 μm have been fabricated in peripheral arrays. Parallel bonding and subsequent transfer of arrays of 28 bumps onto test chips have been successfully demonstrated. Individual bump shear tests have been performed on a sample of 13 test chips, showing an average bond strength of 26 gf per bump.

Index Terms—Flip chip assembly, flip chip bumping, laser ablation, thermosonic bonding.

I. INTRODUCTION

FLIP chip assembly of electronic and optoelectronic chips is one of the key technologies in system packaging and integration with a wide range of applications in microelectronics, optoelectronics, communications and microsystems technology. The technology allows attachment of a bare chip directly to a substrate in a face-down configuration, with electrical connection between chip and substrate being achieved via conducting “bumps” which also define stand-off height. Flip chip interconnection offers a number of advantages over the more widely used technique of wire bonding, including high input/output (I/O) density and short interconnect distance between chip and substrate/board, leading to high performance and miniature products [1]. The technology, originally developed at IBM in the 1960s [1], [2], has evolved considerably in choice of bumping materials, under-bump metallurgy (UBM) and bumping method [1]. Solders, conducting polymers, pure metals and alloys have all been explored as bumping materials, while both thin film deposition and nickel plating have been used to create UBM.

In most flip chip processes, the bumps are produced directly on the chip or substrate before assembly. An alternative is to fabricate the bumps on a carrier and then transfer them onto the chip or

Fig. 1. Schematic of laser-assisted chip bumping process: (i) Fabrication of bumps on a carrier; (ii) thermosonic bonding of a chip to the bumps on the carrier, and (iii) bump release from the carrier by laser machining of the polyimide layer.

substrate—this is the so-called *decal* or transfer approach [3], [4]. Solder and indium bumps have been used previously to demonstrate decal bumping of chips. These low melting temperature materials facilitate thermal transfer of the bumps from carrier to chip, simply by heating the bump material above its melting point and utilising the higher wettability of the bump material to the UBM than to the carrier surface [5]. However this technique is not applicable to bump materials with high melting temperatures such as copper and gold. Non-melting bumps have the advantage that the stand-off height can be made larger than the interconnect pitch, improving the thermal compliance of the assembly.

In this paper, we report a new laser-assisted chip bumping technique based on transfer of electroplated metal bumps. The bumps are produced on a carrier and then transferred onto the chip in parallel. The technique does not require under bump metallurgy because the bumps are bonded directly to the aluminum pads of the chip; this minimizes chip processing prior to flip chip assembly. Fig. 1 shows the schematic of the laser assisted chip bumping process. It consists of three separate steps:

- 1) bump fabrication on a carrier;
- 2) thermosonic bonding of the bumps to a chip;
- 3) release of the bumps from the carrier by laser machining of a polyimide layer, using light incident through the carrier.

In the following sections, we describe the details of the new bumping process and demonstrate the successful bumping of test chips with 28 peripheral I/Os. Shear test data for the transferred bumps are also presented.

Manuscript received December 2, 2000; revised April 6, 2001. This work was presented at the EMAP'00 Conference, Hong Kong, November 30–December 2, 2000. This work was supported by the U.K. Engineering and Physical Sciences Research Council under Grant GR/M12223 “A novel bumping method for flip chip assembly,” Celestica, Ltd., Exitech, Ltd., Morton International (U.K.), Ltd., and Shipley (U.K.), Ltd.

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Publisher Item Identifier S 1521-334X(01)05755-X.

Fig. 2. (a) Schematic of bump fabrication process and (b) details of bump layer structures.

II. BUMP FABRICATION

Bumps were fabricated using the so-called UV-LIGA technique which combines UV lithography with electroplating [6]. This approach has been widely used for fabricating high aspect ratio metallic structures, for example gears for microsystems applications [7] and metal bumps for high pitch electronic interconnections [8]. Fig. 2(a) shows a flow diagram of the fabrication process. Firstly a layer of polyimide was deposited on a quartz (fused silica) wafer by spin coating, and cured in an oven for 2 h at $\sim 170^\circ\text{C}$. The layer thickness was of order $2\ \mu\text{m}$ after curing. Quartz was chosen as the carrier material because it is transparent at 248 nm, the wavelength of krypton fluoride excimer laser used in this work to release the bumps from the carrier. Secondly, depending on the required bump structure, either a copper layer of $\sim 300\ \text{nm}$ thickness or a gold layer of $\sim 200\ \text{nm}$ thickness was produced on the polyimide layer by sputter deposition. This thin metallic layer served as a seed layer for electroplating during bump formation. Thirdly a layer of dry film photoresist of $50\ \mu\text{m}$ thickness (Morton International, type Laminar 5050) was laminated onto the seed layer at a temperature of $\sim 117^\circ\text{C}$. Dry film resist offers advantages of easy processing and compatibility with standard PCB (printed circuit board) manufacturing processes. To produce resist moulds for bump formation, the resist film was exposed on a mask aligner (Quintel UltraLine 7001) through a mask with patterns for bump definition. The resist was then spray-developed using a commercial alkaline developer (Morton International, type KB1A). The wafer was then rinsed in deionised water prior to electroplating.

Gold, nickel and copper plating were carried out to produce bumps with gold metallization either at one end or at both ends, as shown in Fig. 2(b). The latter structure requires a more elaborate plating process, but the resulting bumps exhibit better solderability and also allow thermosonic or thermocompression

(a)

(b)

Fig. 3. (a) SEM image of Au/Ni-Cu-Ni/Au bumps on a carrier and (b) detail of a single bump.

bonding at the substrate attachment stage. The main body of the bump is copper with nickel barrier layers between the gold and copper to prevent interdiffusion which would otherwise degrade the joint. Copper was used as the bump material because of low cost. All three metals were plated using commercial baths based respectively on gold potassium cyanide (Engelhard CLAL, type E59), nickel sulphamate (Schloetter, type Sulphamate MS), and copper sulphate/sulphuric acid (Shipley, type Electroposit 1200T).

After the electroplating process the resist mould was removed using a commercial stripper (Morton International, type Alkatrip SQI, 5% aqueous solution), and the seed layer was cleared from around the bumps by wet etching (using either an ammonium persulphate copper etch, or ISOFORM gold etch). The exposed polyimide was also removed by reactive ion etching (RIE) to minimize the debris produced by the subsequent release process. A pure oxygen plasma was used under the following conditions: 160 W RF power, $\sim 50\ \text{mT}$ chamber pressure and 50 sccm oxygen flow. Under these conditions the exposed polyimide was removed completely in 10 min. Fig. 3 shows SEM

Fig. 4. Experimental setup for thermosonic bonding of chips to carriers.

images of bumps on a carrier before removal of the seed layer. The bumps shown are $60\text{ }\mu\text{m}$ in diameter and $\sim 50\text{ }\mu\text{m}$ in height, with gold bonding layers on both ends and nickel barrier layers between the gold and the copper. The Ni barrier layers are each $\sim 3\text{ }\mu\text{m}$ thick, while the top and bottom Au layer thicknesses are $\sim 5\text{ }\mu\text{m}$ and $\sim 3\text{ }\mu\text{m}$, respectively.

III. BUMP-TO-CHIP BONDING

As mentioned previously, a key feature of the new bumping technique is the minimal processing of the chip prior to flip chip assembly; the bumps are fabricated on a separate carrier, and no preprocessing of the aluminum contact pads is required before transfer of the bumps to the chip. Fig. 4 shows a schematic of the purpose-built bonding setup, which consists of a mechanical stage system for aligning the chip to the carrier, an optical vision system for monitoring alignment, and an ultrasonic bonding head. The carrier is mounted over a quartz window on a heated platform, while the chip is held by the ultrasonic bonding tool. The quartz window allows a CCD camera, mounted underneath the platform, to view the bump array and the chip simultaneously for alignment purposes. The platform, and hence the carrier, can be translated in the horizontal plane, and rotated about the vertical axis; it can also be tilted to achieve good parallelism between chip and carrier, an essential requirement for array bonding [9]–[11].

The ultrasonic system consists of a 40 W generator, a transducer/horn and a bonding tool. The ultrasonic generator and the transducer were provided by UTHE inc, and the bonding tool was provided by Pine Valley inc. The bonding tool was mounted on the arm of the transducer (see Fig. 4). The tool was designed to have a cavity at the bonding end for location of the chip and a capillary for vacuum pick-up. The transducer and the tool were set up in the transverse configuration i.e., with the tool end and the chip vibrating parallel to the plane of the carrier under ultrasonic excitation.

For thermosonic bonding, application of a controlled bonding force is essential to ensure good contact between the bond pads

Fig. 5. Bonding force versus displacement of spring-loaded stage.

on the chip and the bumps on the carrier. This is achieved in our setup by having the transducer mounted on a vertical, spring-loaded linear stage. The displacement of the stage is monitored with a digital micrometer as the entire assembly is lowered and the chip is pushed against the carrier. Fig. 5 shows how the applied force varies as a function of the stage displacement; the relationship is linear up to a force exceeding 2 kgf, with a coefficient of 0.39 kgf/mm.

A number of test chips have been bumped using the thermosonic bonding setup described above. The test chips were designed to have 28 I/Os in a peripheral layout with seven aluminum pads on each side, as shown in Fig. 6(a). The square pads are $90\text{ }\mu\text{m}$ in size and the pitch is $127\text{ }\mu\text{m}$ on all sides. The chip outer dimensions are $1.3\text{ mm} \times 1.3\text{ mm}$. The bump layout was designed to match that of the contact pads exactly, and the bumps were circular with diameters of 60, 70, 80, or $85\text{ }\mu\text{m}$. Each 3" diameter carrier could provide bumps for up to 512 test chips. No special cleaning of the aluminum pads was carried out before bonding and no trace of pad contamination was observed under an optical microscope. The details of the bumps and the bonding conditions are given in Table I. Fig. 6(b) shows an optical image of a bonded chip, viewed through the carrier.

IV. LASER-DRIVEN RELEASE

The final step in the bumping process is to release the bumped chips by laser machining the polyimide layer between the bumps and the carrier. Any polyimide residues remaining on the ends of the bumps must also be cleaned away following the release operation; this can be achieved by normal laser ablation. The bumped chips can then be assembled onto a circuit board or MCM (multichip module) substrate. At Imperial College, we are developing a process based on thermosonic substrate attachment. Reflow soldering of fine-pitch copper columns is also possible, and has been demonstrated previously [8].

In this work the release process was carried out using an industrial excimer laser workstation (Exitech Ltd), incorporating a krypton fluoride excimer laser operated at 248 nm wavelength. The system includes a conventional fly's eye homogeniser to

Fig. 6. (a) Optical micrograph of a test chip with 28 peripheral aluminum contact pads; the square pads are $90\ \mu\text{m}$ in dimension and on a $127\ \mu\text{m}$ pitch. (b) Optical micrograph of the chip after bonding to the bumps on a carrier showing good alignment between the pads and bumps; image taken through the quartz carrier.

produce uniform illumination at the sample plane, as shown in Fig. 7; this ensures that the mechanical impulse generated by the polyimide ablation is uniformly distributed over the bump array. Chip release was typically achieved by a single laser pulse at a fluence of around $100\ \text{mJ}/\text{cm}^2$. At this fluence level the laser radiation is expected to vaporise only a very thin layer of polyimide ($\sim 0.1\ \mu\text{m}$), but this is sufficient for separation of the bumps from the carrier.

The residual polyimide on the bumps was removed by normal laser ablation at a slightly higher fluence of $\sim 150\ \text{mJ}/\text{cm}^2$. This fluence level is below the laser damage threshold of the chip passivation and underlying electronics, and so flood exposure could be used without risk of damage to the chip. Fig. 8 shows SEM images of a chip with Au/Ni-Cu bumps after laser cleaning. LIMA (laser-ionization mass analysis) was performed on cleaned bumps to assess the effectiveness of the cleaning process. No trace of the characteristic polyimide

TABLE I
BUMP DETAILS AND BONDING
PARAMETERS FOR THERMOSONIC BONDING OF CHIPS TO BUMPS ON CARRIERS

Bump diameter	60 to $85\ \mu\text{m}$
Bump height	$\sim 50\ \mu\text{m}$
Number of bumps/bonding pads	28
Bonding force	1.6 to 2 kg (57 to 71 gf per bump)
Ultrasonic energy	16 W
Bonding time	500 ms
Bonding temperature	$235\ ^\circ\text{C}$

Fig. 7. Optical setup for laser-driven release, showing fly's eye homogeniser.

signature was observed, indicating complete removal of the polyimide layer.

V. SHEAR TESTS

Shear tests were conducted to determine the strengths of the bump-to-chip bonds. These tests were carried out using a Dage 4000 series machine. Each chip was attached to a $5\ \text{mm} \times 5\ \text{mm}$ silicon substrate with epoxy glue for ease of mounting on the tester, and the bumps were sheared off individually. The chip was positioned under the needle of the shear tester by moving the chuck in the X and Y directions. The needle was then lowered such that its tip was just above the chip surface, and the chip position was adjusted such that the bump to be sheared was aligned to the needle, as shown schematically in Fig. 9 (inset). The needle was then brought toward the bump to shear it off the chip. The height of the needle tip above the chip was automatically set to a pre-determined value; for the shear tests reported in this paper, this height was set to $10\ \mu\text{m}$. A cartridge with a force range of 0–100 gf was used. Each test result was acquired by a computer.

The graph in Fig. 9 shows the distribution of shear strengths among the individual bumps on a particular chip. The bump diameter was $60\ \mu\text{m}$ in this case. The results show an average shear strength of 39 gf, while the maximum and minimum bonding strengths are 93 gf and 10 gf respectively. These values are well above the 5 gf per bump specified in the U.S. military standard test method for microcircuits (MIL-STD-883E under the Method 2011.7 for flip chip devices [9]), and the average bond strength is comparable to the value of ~ 50 gf typically obtained for gold wire bonding to aluminum pads (100 point average) [10]. A larger sample of 13 test chips bumped under similar process conditions yielded a global average bond strength of 26 gf.

(a)

(b)

Fig. 8. (a) SEM image of transferred Au/Ni-Cu bumps on a chip after laser cleaning of polyimide residues and (b) detail of a single bumped contact pad.

The variation in bond strength with position in Fig. 9 appears to contain both systematic and random components. The systematic component—an increase in bond strength from left to right—is believed to be associated with the presence of slight nonparallelism between the chip and the carrier during the bonding process [11], [12]. Unfortunately, at the time of measurement there was no diagnostic tool for monitoring the parallelism between chip and carrier prior to bonding. The random component is probably caused by slight variations in bump height and/or surface profile. To investigate this aspect height maps of several bumps arrays were obtained using a Zygo interferometer. The carrier studied had been slightly over-plated, and consequently the bumps were domed in shape. The difference in height between the centre and edge of each bump was recorded, and found to lie in the range 2.5 to 3.5 μm . The centre heights showed a random variation within each array having a standard deviation of 0.4 μm or less, and a maximum deviation from mean of $\pm 0.8 \mu\text{m}$. These nonuniformities in profile and centre height, although small enough to

Fig. 9. Typical distribution of bump shear strength across a chip and (inset) shear test configuration.

Fig. 10. Optical micrographs of contact pads after shear testing showing: (a) desirable failure mode with high shear strength and (b) silicon cratering resulting in chip damage.

be taken up by compression of the gold bonding layer, appear to be the most likely cause of the observed variations in bond strength. Further experiments are planned to test the correlation between bump height and subsequent bond strength. Surface contamination of the bumps by organic residues from the bump fabrication process is another possible explanation of bond strength variability. However, this appears less likely in view of the relatively high average bond strength.

The failure modes of the shear test were examined under an optical microscope and are shown in Fig. 10. The preferred failure mode, associated with higher shear strength, is shown in Fig. 10(a); here the pad metallization has pulled away leaving the underlying silicon intact. The silicon cratering in Fig. 10(b) corresponds to a lower shear strength. These failure modes have been widely reported previously in thermosonic bonding of gold wires to aluminum pads [13]. Silicon cratering is known to be

related to excessive local stress at a bonding site generated by the bonding force and the applied ultrasonic energy.

VI. DISCUSSION

A new laser-assisted transfer bumping technique for flip chip assembly and packaging has been investigated. The bumping process, which could be implemented on a single bump transfer machine combining thermosonic bonding with laser ablation, offers two potential advantages over existing chip bumping methods: bumps are applied to the entire chip in a single bonding step, and no under bump metallurgy is required resulting in minimal chip processing before bumping. Copper bumps (low cost, high conductivity) with gold bonding layers and nickel barrier layers, have been fabricated using UV lithography and electroforming, a micro-engineering technique suitable for fine pitch ($< 100 \mu\text{m}$) flip chip interconnections [1]. Parallel bonding of 28 bumps has been realized and successful transfer of the bumps from a carrier to a chip has been demonstrated using the laser-driven release technique. Shear tests on individual bumps show adequate bond strength in the vast majority of cases. Reliability data for chips assembled onto substrates will be reported in a later paper.

A key issue with the current process is the wide variation in bond strength across the chip. An optical system for monitoring chip-to-carrier parallelism is currently being introduced with a view to eliminating nonparallelism as a possible cause of this variation. Other factors, such as bump height nonuniformity and gold surface roughness, are also being investigated as possible causes of random variations in bond strength. Reduction of bond-strength variability should allow optimization of the bonding process and elimination of the observed cratering phenomena. Finally, to achieve high reliability under temperature cycling, bumps with substantially higher aspect ratios will be required, and we are currently developing modified fabrication processes to produce such bumps.

ACKNOWLEDGMENT

The authors wish to thank M. Hendriksen, Celestica, and J. Greuters, Exitech, for their assistance with the shear tests and laser-driven release experiments, respectively.

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