Laser-Assisted Bump Transfer for Flip Chip Assembly

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Abstract

This paper describes a novel laser-assisted bumping technique for flip chip assembly. Copper bumps, with gold bonding layers and intermediate nickel barriers, are fabricated by UV lithography and electroplating on quartz wafers with pre-deposited polyimide layers. The bumps are thermosonically bonded to their respective chips and then released from the carrier by laser machining of the polyimide layer, using laser light incident through the carrier. Bump fabrication, parallel bonding, and chip release have been successfully demonstrated for test chips having 28 peripheral I/Os on 127 μm pitch. Visual inspection of bump cross-sections and individual bump shear test measurements have been carried out for chips bumped by the new method.

Introduction

Flip chip assembly allows bare integrated circuit dies or chips to be attached to an electronic substrate in a face-down configuration. Electrical connection between chip and substrate is achieved via bumps that also provide mechanical stability and define the chip-to-substrate separation or stand-off height. The bumps have to be introduced onto the chip or the substrate prior to the assembly process. Chip bumping can be achieved either by direct fabrication of bumps on the chip, or by a transfer method in which the bumps are fabricated on a separate carrier and then transferred to the chip. In both cases, wafer-scale processes have been developed that allow parallel bumping of many chips prior to wafer dicing. For example, screen and stencil printing have been used for direct wafer-scale fabrication of solder and adhesive bumps [1-3], while wafer-scale bump transfer methods have been demonstrated for solder and indium bumps [4,5]. Transfer bumping has the advantage that the bumps can be inspected before they are transferred onto the chip or wafer, potentially improving yield.

In this paper, we report a transfer bumping method in which laser ablation is used to realise bump transfer from carrier to chip. An outline of the process is shown in Figure 1. Bumps are fabricated on a quartz carrier with an intermediate polyimide layer (Fig. 1(a)), and then bonded directly onto the aluminium pads of a silicon chip (Fig. 1(b)). The bumped chip is separated from the carrier by

laser machining of the polyimide (Fig. 1(c)), completing the transfer process. The laser beam is incident on the polyimide layer through the transparent quartz carrier. After the release process, any polyimide residues on the bumps are removed to ensure that the bump ends can form conducting joints with the contact pads on a substrate. Cleaning can be achieved either by laser ablation or plasma etching.

Figure 1: Schematic of laser-assisted chip bumping process: (a) fabrication of bumps on carrier, (b) bonding of bumps to chip, and (c) release of bumped chip from carrier.

The new bumping method offers several potential advantages over existing chip bumping techniques. Firstly, unlike solder bumping [2,3], it does not require under-bump metallurgy (UBM) so there is no chip processing prior to bumping. Secondly, it allows the use of low-cost, lead-free bump materials such as copper.

Thirdly, bump transfer is parallel, but can also be applied selectively if necessary by masked exposure of the carrier. In addition, by using microfabrication techniques to realise the bumps, the method can produce fine pitch bumps suitable for high-density flip chip interconnection.

Bump fabrication

A combination of UV lithography and electro-plating was used to fabricate cylindrical bumps with a layer structure as shown in Figure 2. The upper gold layer in this structure facilitates thermosonic bonding of the bump to the IC (integrated circuit) contact pad, while the lower gold layer renders the bump suitable for substrate attachment by a range of techniques, including thermosonic bonding. The nickel layers provide barriers between the copper and gold to prevent interdiffusion which would otherwise degrade the joints and compromise the reliability of the assembly. Quartz wafers of 3-inch diameter were used as the carriers for bump fabrication. The layout of the bumps was designed to match the pad layout of our test chips - a square peripheral array consisting of seven bumps on each side (28 bumps in total), with a 127 μm pitch on all sides of the array. The patterns were arranged in 32 groups of 4x4 arrays, producing 512 bump arrays on a single quartz wafer. Bumps of diameters of 60, 70, 80, and 85 μm were fabricated on each wafer.

For bump fabrication, firstly a thin layer of polyimide was spin-coated on the quartz wafer and cured in an oven for 2 hours at $\sim 170^\circ\text{C}$. The layer thickness was of order 2 μm after curing. This layer formed the sacrificial material to be laser machined during release of the bumped chips from the carrier. Secondly, a gold layer of ~ 200 nm thickness was produced on the polyimide layer by sputter deposition. Alternatively, a copper film was used if the lower gold and nickel layers were not required. This thin metallic layer served as a seed layer for electro-plating during bump formation. A dry photoresist film of 50 μm thickness was laminated onto the metal layer, and patterned by UV contact exposure and spray development to form the electro-plating mold.

The bumps were formed by electro-plating gold, copper and nickel into the openings in the resist. All three metals were plated using commercial baths based respectively on gold potassium cyanide (Engelhard CLAL, type E59), nickel sulphamate (Schloetter, type Sulphamate MS) and copper sulphate/sulphuric acid (Shipley, type Electroposit 1200T).

After the electroplating process the resist mold was removed using a commercial stripper (Morton International, type Alkastrip SQI, 5 % aqueous solution), and the seed layer was cleared from around the bumps by wet etching (using either an ammonium persulphate copper etch, or ISOFORM gold etch). Also the exposed polyimide was also removed by reactive ion etching (RIE) to minimise the debris produced by the subsequent release process. A pure oxygen plasma was used under the following conditions: 160 W RF power, ~ 50 mT chamber pressure and 50 sccm oxygen flow. Under these conditions the exposed polyimide was removed

completely in 10 minutes. Figure 3 shows SEM images of bumps on a carrier prior to removal of the gold seed layer. The bumps shown are 60 μm in diameter and 50 μm in height, with about 3 μm Ni and 4 μm Au on each end.

Figure 2: Schematic of bump structure.

(a)

(b)

Figure 3: SEM micrographs of (a) Au/Ni-Cu-Ni/Au bumps on a carrier and (b) details of a single bump.

Bump-to-chip bonding

Attachment of the electroplated bumps to their respective chips was performed using a purpose-built

thermosonic bonder. This machine, which is shown schematically in Figure 4, consists of a mechanical stage system for aligning the chip to the carrier, an optical microscope for monitoring alignment, and an ultrasonic bonding head. The carrier is mounted over a quartz window on a heated platform, while the chip is held by the ultrasonic bonding tool. The quartz window allows a CCD camera, mounted underneath the platform, to view the bump array and the chip simultaneously during alignment. The platform, and hence the carrier, can be translated in the horizontal plane, and rotated about the vertical axis; it can also be tilted to achieve good parallelism between chip and carrier, an essential requirement for array bonding [6,7].

The ultrasonic system consists of a 40 W generator, a transducer/horn and a bonding tool. The ultrasonic generator and the transducer were provided by UTHE inc, and the bonding tool was provided by Pine Valley inc. The bonding tool was mounted on the arm of the transducer (see Figure 4). The tool was designed to have a cavity at the bonding end for location of the chip and a capillary for vacuum pick-up. The transducer and the tool were set up in the transverse configuration i.e. with the tool end and the chip vibrating parallel to the plane of the carrier under ultrasonic excitation.

Figure 4: Experimental setup for thermosonic bonding of chips to bumps on a carrier.

Application of a controlled bonding force is essential during thermosonic bonding to ensure good contact between the two surfaces. This is achieved in our setup by having the transducer mounted on a vertical, spring-loaded linear stage. The displacement of the stage is monitored with a digital micrometer as the entire assembly is lowered and the chip is pushed against the carrier. The bonding force provided by the stage has a linear relationship with the displacement of the springs.

More than fifty test chips have been bumped using the thermosonic bonding setup described above. As mentioned previously, the test chips were designed to have 28 I/Os in a peripheral layout with seven aluminium pads on each side. The contact pads were 90 μm square and the

chip outer dimensions were 1.3 mm x 1.3 mm. No special cleaning of the aluminium pads was carried out before bonding as no trace of pad contamination was observed under an optical microscope. The bonding conditions were: 16 W ultrasonic power, ~60 g bonding force per bump and 235°C bonding temperature. Figure 5 shows an optical image of a bonded chip, viewed through the carrier. It can be seen that good alignment between the bumps and the pads has been achieved.

Figure 5: Optical micrograph of a chip bonded to the bumps on a carrier, showing good alignment of the bumps to the aluminium pads on the chip. The image was taken through the quartz carrier.

Laser-driven release

The final steps in the bumping process are to release the bumped chips from the carrier by laser ablation of the polyimide layer, and to remove any polyimide residues remaining on the ends of the bumps. The chips can then be assembled onto a circuit board or MCM (multi-chip module) substrate using one of the established substrate attachment methods.

In this work the release process was carried out using an industrial excimer laser workstation (Exitech Ltd), incorporating a krypton fluoride excimer laser operated at 248 nm wavelength. The system includes a conventional fly's eye homogeniser to produce uniform illumination at the sample plane. This ensures that the mechanical impulse generated by the polyimide ablation is uniformly distributed over the bump array. Chip release was typically achieved by a single laser pulse at a fluence of around 100 mJ/cm^2 . At this fluence level only a very thin layer of polyimide (~0.1 μm) is vaporised during the release process.

The remainder of the polyimide on the bumps was removed by normal laser ablation at a slightly higher fluence of ~150 mJ/cm^2 . This fluence level was below the laser damage threshold of the chip passivation and underlying electronics, and so flood exposure could be used without risk of damage to the chip. Figure 6 shows SEM images of a chip with Au/Ni-Cu bumps after laser cleaning.

(a)

(b)

Figure 6: (a) SEM image of transferred bumps on a chip after laser cleaning of polyimide residues, and (b) detail of a single bumped contact pad.

Shear tests

Shear tests were conducted to determine the strengths of the bump-to-chip bonds. These tests were carried out using a Dage 4000 series machine. Each chip was attached to a 5mm x 5mm silicon substrate with epoxy glue for ease of mounting, and its bumps were sheared off individually. The chip was positioned roughly under the needle of the shear tester by moving the chuck in the X and Y directions. The needle was then lowered until its tip was just above the chip surface, and the chip position was adjusted such that the bump to be sheared was aligned to the needle, as shown schematically in Figure 7(a). The needle was then brought towards the bump to shear it off. The height of the needle tip above the chip was automatically set to a pre-determined value of 10 μm . A cartridge with a force range of 0 – 100 gf was used.

The graph in Figure 7(b) shows the distribution of shear strengths among the individual bumps on a particular chip. The results show an average shear strength of 39 gf, while the maximum and minimum bonding strengths are 93 gf and 10 gf respectively. These values are well above the 5 gf per bump specified in the US military standard

test method for microcircuits, MIL-STD-883E under the Method 2011.7 for flip chip devices [8]. The average bond strength is comparable to a value of ~50 gf obtained for gold wire bonding to aluminium pads (100 point average) [9]. The systematic variation in the bond strength across the chip is believed to be associated with the presence of slight non-parallelism between the chip and the carrier during the bonding process [6,7]. Unfortunately, there was no diagnostic tool for monitoring the parallelism between chip and carrier prior to bonding.

(a)

(b)

Figure 7: (a) Shear test configuration, and (b) typical distribution of bump shear strength across a chip.

The shear test failure modes of the bump-to-chip bonds were examined under an optical microscope and representative examples are shown in Figure 8. The preferred failure mode in Figure 8a, where the aluminium pad has been pulled from the chip, is associated with a higher shear strength, while the silicon cratering in Figure 8b corresponds to a lower shear strength. These failure modes have been widely reported previously in thermosonic bonding of gold wires to aluminium pads [10]. Silicon cratering is known to be related to excessive local stress at a bonding site generated by the bonding force and the applied ultrasonic energy.

Cross-sectioning

Cross-sections were performed on a number of samples to examine the bump-to-chip bonds, and to look for possible chip fracture in the underlying silicon. Figure

9 shows a typical result. The layer structure in the bump (in this case Cu-Ni/Au) is clearly visible, as is the interface between the gold bonding layer and the aluminium pad. No damage is evident in the underlying substrate, and this was the case for all samples studied. However, some structure is evident in the gold-aluminium interface, and it is not clear that this is purely an artefact of the sectioning process; this aspect requires further investigation.

Figure 8: Optical micrographs of contact pads after shear testing showing (a) desirable failure mode with high shear strength, and (b) silicon cratering resulting chip damage.

Figure 9: Optical micrograph showing a cross-section of a contact pad after bumping (Cu-Ni/Au bumps).

Summary

A new laser-assisted transfer bumping technique for flip chip assembly and packaging has been investigated. The bumping process, which could be implemented on a single bump transfer machine combining thermosonic bonding with laser ablation, offers two key advantages over the existing chip bumping methods: it is inherently parallel, and no under bump metallurgy is required resulting in minimal chip processing before bumping. Copper bumps with gold bonding layers and nickel barrier layers, have been fabricated using UV lithography and

electroforming, a micro-engineering technique suitable for fine pitch ($<100\text{ }\mu\text{m}$) flip chip interconnections [1]. Parallel bonding of 28 bumps has been realised and successful transfer of the bumps from a carrier to a chip has been demonstrated using the laser-driven release technique. Shear tests on individual bumps show adequate bond strength in the vast majority of cases. Reliability data for chips assembled onto substrates will be reported elsewhere.

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