Investigation of a Low Cost Solder Bumping Technique for Flip-Chip Interconnection

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Abstract

As the demand for flip-chip products increases, the need for high volume, low cost manufacturing processes also increases. All technology roadmaps point towards higher performance products based on finer pitch, high I/O count components. These requirements will push existing low cost solder bumping technologies to their practical limits and future products may have to use higher cost, lower throughput production strategies to achieve the requisite feature sizes.

Currently solder paste printing is the solder deposition method of choice for device pitches down to 150 – 200 μ m, however limitations in print quality and solder paste volume mean that this technology is not likely to move significantly below this pitch. The attractiveness of solder paste printing as a deposition technique due to its low cost and established infrastructure mean that methods for extending its application beyond 150 μ m pitch would be desirable.

This paper describes experiments conducted on carriers made from silicon for bumping of die using solder paste. An anisotropic etching process was used to generate pockets in the silicon surface into which solder paste was printed. Die were then placed against the carrier and reflowed to transfer the solder directly to the bondpads. An assessment was carried out of the potential application and limitations of this technique for device pitches at 225 and 127 μ m. This was based on experimental observations and model calculations of the efficiency with which the Si carrier apertures could be filled with solder paste.

Introduction

The implementation of flip-chip assembly in many products has prompted a rapid increase in interest in this relatively old technology. As the demand for smaller, lighter and more functional products has increased, so the demand for flip-chip technology has also increased, with a concomitant requirement for high volume manufacturing solutions to reduce costs. Currently a number of flip-chip products are in mass production around the world, which utilise existing

assembly processes. However, even with the implementation of flip-chip interconnect, the technology roadmaps for device packaging still point towards even higher performance products with more I/O at finer pitch.

For solder based flip-chip interconnection, a major step in the process route involves the deposition of solder onto the bondpads of the die for subsequent reflow onto the substrate lands. The requirements for finer pitch higher I/O components are already pushing existing low cost solder bumping technologies to their practical limits and future products may have to use higher cost, lower throughput production strategies to achieve the requisite feature sizes and pitches.

Many different methods have been employed for the solder bumping of bare die and these have been reviewed extensively in a number of publications [e.g. 1,2]. Currently solder paste printing onto electroless nickel bumped die represents one of the lowest cost methods for wafer bumping for device pitches down to 150 – 200 μ m [3]. However, limitations in print quality and solder paste volume due to stencil manufacturing limitations and solder particle size mean that existing printing methods are not likely to move significantly below this pitch. The attractiveness of solder paste printing as a deposition technique, due to its low cost and established infrastructure, mean that methods for extending its application below 150 μ m pitch would be desirable.

An alternative approach to the bumping of die involves the attachment of individual pre-formed solder balls onto the bondpads. One example uses sequential placement with immediate reflow *in-situ* by laser irradiation [4]. A number of similar processes for mass bumping use the placement of solder balls onto or into a carrier. This carrier matches the bondpad layout and holds the solder in place against the wafer during reflow [5,6,7,8]. Many of these methods appear to have their origins in the solder ball bumping of BGA and CSP components [5], however the extension of these technologies to flip-chip geometries is non-trivial due to the reduced size of the single solder particles. This

results in additional handling complications due to the low weight of the solder balls in comparison to the forces between particles that can be generated by surface contamination and electrostatic charges. An additional complication for the use of carriers occurs when they are reflowed with the wafer. Any variation in coefficient of thermal expansion (CTE) between the carrier and the wafer can result in a significant displacement of the solder balls from the bondpads during heating from room temperature to reflow temperature. With a stainless steel carrier, this can be as much as 200 μm over the diameter of a 4" wafer. This has led to the suggestion of the use of a Si carrier to match the CTE of the wafer [8].

As part of a programme of work on flip-chip assembly at Loughborough University, alternative technologies for solder bumping have been investigated. In particular we are interested in methods for low-cost assembly with the ultimate aim of assembling devices at pitches of less than 100 μm . This paper describes experiments to evaluate a solder bumping process that utilises a Si carrier for the reflow of solder paste onto bare die. This route combines a number of the ideas presented by other workers and is very similar to processes that have been patented by Delco Electronics Corporation [9] and Fujitsu Limited [10]. An assessment of the potential application and limitations of this technique for solder bumping of fine pitch devices will be presented, together with a description of the carrier manufacturing process.

Process Route

For any solder based process for the assembly of flip-chip devices, a first step in the process involves the deposition of an under bump metallisation (UBM) layer onto the Al bondpad to provide a solder wettable layer. In these experiments an electroless nickel plating process was utilised to deposit a cap of NiP onto the Al surface. This process has been described elsewhere [11] and has been implemented by a number of other groups and companies [3, 4, 12, 13].

The solder deposition process described in this paper was based on the route shown in figure 1. First, solder paste was printed into the apertures of a "stencil", or carrier that was fabricated from Si. After this, die, which were previously electroless nickel bumped, were placed over the carrier with their bondpads aligned with the apertures. The whole assembly was then reflowed to allow the solder to melt and wet the under bump metallisation. Finally, after cooling, the die were separated from the carrier and cleaned to remove the flux residues.

Two types of die were used in these experiments: die A consisted of a peripheral array of daisy-chain structures at 225 and 300 μm pitch, while die B had a peripheral array of bondpads at 127 μm pitch. The dimensions of the die are shown in table 1, together with the thickness of the electroless nickel bumps. It is worth noting that for die B, although the pitch was only 127 μm , the passivation opening over the bondpads was still 90 μm , i.e. larger than

Figure 1:- Process route for solder paste bumping of die. a) print solder paste into apertures (pockets) in Si carrier, b) place die onto carrier surface and reflow, c) separate die from carrier and clean.

Table 1:- Dimensions of die used in solder bumping trials.

Die Type	Pad Pitch / μm	Passivation Opening / μm	Electroless Nickel Bump Thickness / μm
A	225 and 300	75 diameter	6 and 30
B	127	90 square	6

that on die A. This was because die B was designed for wire bonding, while die A had been designed for flip-chip / MCM assembly. This demonstrates one of the difficulties of using die designed for wire bonding in a flip-chip product, but the adaptation of these die for flip-chip assembly forms one of the key aims of the research programme at Loughborough.

Figure 2:- Si carrier manufacturing process.

Si Carrier Manufacture

An important consideration for the implementation of this process for high volume manufacture is the availability of the Si carriers. The approach utilised for the preparation of the Si carrier substrate involved conventional micromachining technology, which is widely used in the formation of Si microstructures. The methodology is also similar to the route employed for the manufacture of conventional stencils. The starting material was a (100) oriented Si wafer, which underwent a series of process steps that are shown in figure 2. Initially, a thermal oxide layer was grown on the surface of the Si, before a photoresist was applied. The resist was then exposed and developed to reveal the oxide layer which was then etched away using hydrofluoric acid. Once this was complete, the photoresist was removed and the thermal oxide layer was used as the resist during the etching of the underlying

silicon with ethylene diamine pyrocatechol. The depth of the aperture was determined by the length of time for which this etching process was carried out. After etching was complete, the thermal oxide layer was then removed in a final hydrofluoric acid treatment.

The combination of the (100) oriented Si wafer, together with the etchant resulted in the production of tapered apertures with square openings as shown in figures 3 and 4. The etching process was anisotropic with the (111) plane etched at a rate 30 - 40 times slower than the (100) plane. This resulted in a taper angle of 54.7° to the surface plane, with only limited undercutting of the thermal oxide resist.

For die A, the aperture opening was 165µm with a depth of 75µm, while for die B, two different apertures were generated with openings of 95µm and 80µm at depths of 63µm and 56µm respectively. In the case of the 80µm aperture, the depth was limited by the intersection of the two sloping sides, effectively halting the etching process. This represents the physical limit of the aperture depth. The theoretical aperture openings that can be generated by this process are limited only by the bondpad pitch, however, the ability to mask and image the photoresist ultimately determines the minimum gap between the apertures. The aperture sizes used here were smaller than the bondpad pitches on die B as these were determined by the resolution of the original photoplotted mask. This resolution could have been significantly improved by using a chromium-on-glass mask, but this would have increased the cost of the process dramatically.

Solder Bumping

Initial trials of the process were conducted using die A. To fill the apertures in the Si surface with solder paste, a conventional squeegee printing process was employed. Two solder pastes were used during these studies: a water washable paste (WR) with a particle size range of 15-30 µm and a rosin active (RA) paste with a particle size range from 0 µm (dust) - 25 µm. These pastes were printed by drawing the squeegee blade over the surface by hand. In order to obtain the best print quality, a range of squeegees were tested. This was necessary to ensure that the surface of the carrier remained free of solder particles, which would interfere with the placement of the die, preventing it from lying flat and making good contact between the electroless nickel bumps and the solder paste in the apertures. While a soft rubber squeegee left very little paste over the carrier surface, it also "scavenged" a significant quantity of paste from the apertures leading to undersized solder balls during reflow. A metal squeegee was found to offer the best finish, leaving a well filled aperture with little extra paste on the carrier surface.

After filling the stencil apertures with solder paste, individual die were placed on the stencil using a fine pitch placement system to align the bondpads with the carrier apertures. The whole arrangement was then reflowed to allow the solder to wet the UBM and was then cooled. Following this, the die were held in contact with the Si

Figure 3:- SEM images of Si carrier for die A.

Figure 4:- Schematic diagram of aperture in Si carrier.

carrier by the flux residues remaining from the solder paste. In order to release the die, the assembly was immersed in a suitable solvent for the solder paste in use and ultrasonically agitated to encourage the penetration of the solvent underneath the die. After a few seconds cleaning, the die were released from the surface of the stencil and were then further cleaned to remove any final residues.

Figure 5:- Solder bumped die A after removal from carrier.

Cleaning of the Si carrier was similarly carried out in a solvent to remove residues from the apertures. The efficiency of this process depended greatly on the solder paste in use. It was found that, in general, water washable paste residues were the easiest to remove, leaving a clean surface after only a few seconds ultrasonic cleaning in water, while RA paste residues required many minutes cleaning in iso-propanol.

After removal of the die from the carrier, the solder deposits were found to be distorted as though they had been "cast" in the shape of the apertures during solidification (figure 5). In order to generate well-rounded solder bumps it was necessary to carry out a further reflow of the die away from the carrier material. Figure 6 shows an area of one die for which this was carried out. This die was originally bumped with $6\mu\text{m}$ of electroless nickel and shows the results that are achievable with this type of device. Due to the controlled volume of solder paste in the carrier apertures, the process generated solder balls of a very uniform height ($\sim 75\mu\text{m}$) and volume.

Attempts to extend the bumping process to die B at $127\mu\text{m}$ pitch were largely unsuccessful and only one or two pads on the die collected the solder from the apertures. Generally the electroless nickel bumps failed to contact the molten solder paste and the reasons for this will be discussed further in the next section.

Solder Volume Calculations

In order to guarantee transfer of the solder paste from the aperture onto the UBM during reflow, there must be sufficient volume of solder such that during reflow of the solder paste into a spherical ball, the resulting sphere will protrude above the stencil surface allowing contact to be made with the electroless nickel bump. Based on the highly controlled nature of the carrier aperture etching process, it was possible to calculate the solder volumes that would be generated for apertures of different aspect ratios. Following

Table 2:- Calculated and measured protrusion of reflowed solder paste above carrier surface (susp. indicates that solder ball is expected to be suspended in tapered aperture)

Aperture Opening / μm	Aperture Depth / μm	Aperture Volume / μm^3	Solder Paste Particle Size / μm	Calculated Maximum Packing Efficiency	Calculated Solder Sphere Diameter after Reflow / μm	Predicted Protrusion of Sphere above Carrier / μm	Measured Protrusion of Solder above Carrier / μm
165	75	10.1×10^5	15-30	47%	97	22	8 + 2
165	75	10.1×10^5	0-25	50%	99	24	10 + 2
95	63	2.02×10^5	15-30	34%	51	2 (susp.)	-4 + 3
95	63	2.02×10^5	0-25	38%	53	5 (susp.)	-2 + 2
80	56	1.21×10^5	15-30	32%	42	1 (susp.)	-4 + 4
80	56	1.21×10^5	0-25	36%	44	3 (susp.)	-4 + 2

Figure 6:- Bumped die after second reflow to centre solder deposits.

this, the reflowed solder sphere diameter could be determined and compared to the aperture depth. Although initially such calculations appear relatively simple, a number of extra features needed to be taken into consideration. First, in many situations, including the 80 and 95 μm apertures, the base of the aperture was very

narrow and, after reflow, the solder ball, if it remained spherical and did not wet the Si surface, would not touch the base. This situation is demonstrated in the micrograph of figure 7a, which shows a cross-section through an 80 μm wide aperture following reflow of the solder paste. Clearly the solder did not reach the bottom of the aperture and remained approximately spherical due to its surface tension. In these circumstances for the purposes of modeling the extent of protrusion of the solder ball from the aperture, it was necessary to calculate the height at which the solder ball was suspended by assuming it retained a spherical shape.

In addition to the above, it was initially assumed that 50% of the aperture volume would be filled with solder metal, equivalent to the solder metal content in the solder paste. However, as the volume of the aperture decreases and the particle size of the solder paste remains the same, this assumption becomes incorrect due to incomplete packing of the particles in the pocket. This situation was difficult to model without accurate information regarding the particle size distribution of the solder paste. However estimates of the packing efficiency could be made, using a computer model to maximise the packing of spheres into an aperture. Example calculations for the apertures used in this study are shown in Table 2, together with comparative data obtained from the experiments. For the model calculations presented, a uniform particle diameter distribution was chosen, and the particles packed into the aperture in a method similar to that indicated in reference 14.

For the larger 165 μm apertures, the calculations indicate that particle size has little effect on the packing efficiency and the assumption of 50% of the aperture volume reflowing as solder metal is still correct. However, for the smaller apertures, the packing efficiency can decrease to as little as 32%. From table 2 it can be seen that there is some agreement between calculation and experiment for the various aperture sizes, particularly the smaller ones. As expected, the model predicts a higher packing density for the finer particle size paste (0-25 μm), which, the experimental results appear to reflect. However, following the reflow process with the 0-25 μm paste, a number of small solder particles were observed in the aperture that

Figure 7:- Cross-section of reflowed solder paste in Si carrier apertures a) aperture opening of 80µm (die B), b) aperture opening of 165µm (die A).

were unattached to the bulk solder ball indicating incomplete reflow of the paste. This resulted in the reflowed solder ball being smaller in volume and led to reduced protrusion of the ball from the aperture. This highlights one of the major difficulties in using solder pastes with finer particle sizes; as the ratio of solder surface area to volume rises, the flux activity can be insufficient to allow all the particles to coalesce. Even with an RA flux in the paste the solder did not reflow completely.

The reason for the differences between experimental observation and calculation are unclear, but may reflect the fact that the solder volume calculations assume a uniform particle diameter distribution and the real printing process may not achieve such a high packing density. Using an excess of smaller particles in the computer simulations leads to more efficient packing, and similarly an excess of larger particles leads to lower volume fractions.

Deformation of the solder spheres, and a slight wetting of the solder to the Si may also account for the differences between theory and experiment. In particular, for the smaller apertures, the solder is expected to be suspended in the aperture (figure 7a) and may be slightly deformed due to its weight. This could result in the ball being slightly below the carrier surface as observed. It is difficult to

Figure 8:- Schematic diagrams of chip placement and solder reflow. a) Conventional process with 6µm electroless nickel bumps on die A, b) process with 30µm electroless nickel bumps on die A, c) 6µm electroless nickel bumps on die B, d) paste residue on carrier during reflow of die B, e) solder dipped die A placed on carrier.

ascertain from the micrograph in figure 7a whether the ball is deformed, due to the problems associated with polishing a soft material like solder, which can smear. However, the solder ball in the large aperture of figure 7b is clearly not spherical, as it appears to be wider than it is tall. This may explain some of the larger differences for the bigger apertures.

It is apparent from the results in table 2 that for die A, a good degree of protrusion of the molten solder was observed and this led to a good yield for the die used in these experiments. The above calculations assume that the UBM cannot project into the aperture, however, one advantage of the use of electroless nickel as the UBM for die A, was that the height of the bump allowed it to protrude into the aperture ensuring a good contact between the bump and the solder paste (figure 8a). This interaction could be enhanced by using die with thicker (e.g. 30µm) electroless nickel bumps (figure 8b). Unfortunately for die B, bumps significantly thicker than 6µm could not be used. This was due to the isotropic nature of the electroless nickel process which produced both outward as well as upward growth of the deposits and therefore could not be applied to die B as this would have shorted the bumps together. Furthermore, the width of the electroless nickel bump on die B was larger than the aperture opening and therefore the bumps could not protrude into the apertures to contact the solder paste (figure 8c). This was exacerbated by any solder paste particles left on the carrier surface following printing (figure 8d). The lack of good contact between the bumps

Table 3:- Calculated and measured solder bump heights on die after reflow (based on 15-30 μ m solder paste).

Aperture Dimensions Opening / Depth / μ m	Die Type and NiP thickness	Electroless Nickel Bump Dimensions	Predicted Solder Ball Height (excl. NiP) / μ m	Measured Solder Ball Height (excl. NiP) / μ m
165 / 75	A - 6 μ m	87 μ m diameter	77	69
165 / 75	A - 30 μ m	135 μ m diameter	54	50
95 / 63	B - 6 μ m	102 x 102 μ m	~17	-
80 / 56	B - 6 μ m	102 x 102 μ m	~10	-

and the solder paste during reflow resulted in almost complete failure for this bumping process when applied to die B.

In these studies no gold flash was applied over the nickel surface following bumping and the un-preserved nickel surface produced a number of failures due to the solder paste not wetting the nickel pads. In subsequent experiments, the solderability of the die was improved by applying a solder finish to the bumps using a simple dipping procedure [11]. This involved the fluxing of the die followed by immersion in a solder bath. This method left a small cap of solder on top of the nickel bump, which had a thickness of around 13 μ m for die A. In addition to creating a more wettable surface, this procedure also increased the height of the bump, which subsequently increased its protrusion into the aperture of the Si carrier after placement (figure 8e). The resulting enhanced contact between bump and paste and more solderable surface also improved the yield of the bumping process.

From the solder volume calculations presented above, the height of the final solder bump could be estimated, based on the diameter of the electroless nickel bump, using a straightforward calculation for a spherical cap [15]. Table 3 shows the results of these calculations. For a 6 μ m thick NiP bump on die A, the predicted bump height was 83 μ m (including the electroless nickel thickness), in fair agreement with the measured bump height of 75 μ m. It should be remembered that the spherical cap equation assumes wetting of a flat surface. In order to carry out more detailed calculations of bump height, the effect of the solder wetting the rounded sides of the electroless nickel bumps would need to be included. This may account for some of the difference between calculation and experiment

Of more importance, the figures in table 3 for the small apertures indicate that even if the process could be applied to die B, the small size of the apertures and the large surface area of the bumped bondpads would lead to extremely small solder bumps. This therefore indicates that the technique is unlikely to be useful for extension to the bumping of these fine pitch devices with large bondpads.

Figure 9:- Solder bumped die A with 30 μ m thick electroless nickel bump.

An indication of the approaching limit of this technique can be seen with the 30 μ m electroless nickel bumps on die A. As the electroless nickel process used for the UBM was isotropic, the diameter of the bondpads on the die with 30 μ m high NiP bumps was significantly larger than the original passivation opening of 75 μ m (i.e. final diameter of 135 μ m). Figure 9 shows a solder bump on one such die. Here the volume of solder was insufficient to wet the sides of the large nickel bumps and a bump shape was formed that was determined by the surface tension of the solder and the low contact angle made with the rounded edge of the electroless nickel bump.

Discussion

The process described above features a number of aspects that could allow a low cost reliable process to be achieved. In particular, the use of solder paste provides a relatively low cost source of solder and the technology and infrastructure to print solder paste and place and align wafers is already available in most stencil printing machines. This route also has potentially limited environmental impact, comparable to conventional stencil printing, but with significant advantages over alternative processes that require imaging and development of photoresists [16] or the disposal of used carrier materials such as polyimide tapes [7].

An important feature of the present process is that it does not rely on the paste releasing from the stencil apertures, as in the conventional printing process. This allows a simplified paste rheology and formulation to be designed and would allow for a greater range of flux vehicles to be used. This is particularly useful for the important process step of releasing the die from the carrier, which involves dissolving the flux residues and cleaning of the carrier apertures. Presently, this step of the process would make application of this method to whole wafers problematic due to the difficulties associated with encouraging solvents to penetrate between the wafer and carrier. If this process could be carried out efficiently by good design of the solder paste for easy cleaning, then a significant increase in throughput could be achieved, together with safer handling of bumped wafers.

The Si carriers used in this work were made from a relatively low-cost source material that allowed the carrier to expand and contract at the same rate as the wafer during reflow, maintaining the registration between the apertures and the bondpads. In addition, the Si provided a non-solder wettable surface to allow easy release of the bumped die. The manufacturing process for the carriers used existing technologies that could be easily applied to a high volume process. This is particularly important since in a high throughput wafer bumping line, a number of carriers would be required to allow some to be printed and die placed, while others were reflowed and cleaned. It is not envisaged though, that preparing multiple carriers of the same design would significantly increase the tooling costs.

The major limitation of this technique becomes apparent from the solder volume calculations above. The quantity of solder that can be deposited, is limited severely by the aperture shape, although by using solder pastes with different particle size distributions, the efficiency of the printing process could be improved. In the case of die B, there is insufficient solder metal volume in the aperture to form a ball that protrudes above the carrier surface to contact the chip. However, even if contact could be made, the volume that would be deposited would not be sufficient to form a suitable flip-chip joint due to the large area of the bondpads. Further investigations are planned to look at alternative carrier manufacturing processes to generate apertures with different shapes and also different particle size solder pastes to improve the aperture filling efficiency.

In order to increase the volume of solder, it was possible to repeat the process on previously bumped die. This effectively doubled the solder volume. Figure 10 shows solder bumps on top of 30 μ m electroless nickel (compare with figure 9) and shows clearly how the increase in solder volume has allowed the solder to cover the sides of the electroless nickel bumps. This is possible, as the volume printed into the apertures is constant and is simply added to the volume already on the die. By contrast, if a repeat printing stage were to be carried out with a conventional stencil printing process, the volume of solder would not be doubled, as the solder bump already formed on the die

Figure 10:- Die A with 30 μ m electroless nickel bumps following double solder application process.

would occupy a significant part of the stencil aperture, limiting the amount of additional paste that could then be printed. An alternative process route therefore suggests itself for some applications: due to the faster conventional stencil printing process this could be used to apply the first solder volume to the die while a subsequent Si carrier based process could be used to increase the final bump height. This could be useful for boosting the solder volume in applications where one printing process would not be sufficient.

Conclusion

This paper has evaluated the potential application of a low cost solder bumping route for fine pitch flip-chip assembly. This technology offers a reliable method to use solder paste as a bumping medium for devices around 200 μ m pitch, comparable to conventional printing. However, for very fine pitch devices, difficulties due to solder volume restrictions mean that this method may have limitations. Careful design of the carrier aperture size and shape and solder paste particle size distribution needs to be carried out to ensure the maximum bumping yield.

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