A CMOS-based light modulator for contactless data transfer: theory and concept.

Alexandru Serb, Konstantin Nikolic and Timothy G. Constandinou

Centre for Bio-Inspired Technology, Institute of Biomedical Engineering and
Department of Electrical and Electronic Engineering, Imperial College London, SW7 2BT, UK

ABSTRACT

A new technique pertaining to the optical contactless chip-to-board communication using a commercially available CMOS technology is under development. The main concept is to use mid-IR light from a small LED which will enter an IC from the underside, impinge upon one or more pn-junctions and be reflected by a metallic sheet so that it falls on an external, discrete photodetector. After propagation through the doped semiconductor, the light undergoes attenuation due to free carrier absorption. By varying the reverse bias across the pn-junction(s), the depletion region widths are changed and therefore modulation of light intensity can be achieved. Through this scheme, data readout can be realized optically, thus alleviating the need for galvanic contacts (most notably wirebonds).

Keywords: Free carrier absorption, CMOS, modulator, silicon photonics, lab-on-chip

1. INTRODUCTION

In recent years there has been growing interest in using optical, rather than electrical signals to transmit information to/from electronic chips. Work abounds on the use of silicon waveguides and light modulators as well as integrating light sources on a silicon chip. However, none of these ideas can as yet be implemented in commercially available CMOS technology, nor has a CMOS-based communication platform that transmits information via contactless optical interconnects been reported so far in the literature.

A variety of papers deal with optical modulation in silicon, however all of them are based on manipulating the real refractive index of silicon and creating silicon wave-guides that help optical signals propagate along the surface of the die rather than vertically, through the die.¹⁻³ For example, Liao et al.¹ deals with a system where a very accurate laser sends light through two different optical paths. Then, devices described as ‘phase shifting diodes’ are used to slow-down the EM beams by manipulating the real refractive index of the surrounding material, i.e. at the output, phase shifts are measured. Others propose systems^{2,3} that run along the same lines: phase shifting, interferometric methods, etc.

In the topic of light sources on-chip the literature is even more abundant as these papers demonstrate.⁴⁻¹² In these papers, a wide variety of methods is proposed to coax silicon into emitting light. They range from erbium implantation⁷ and dislocation loops¹⁰ to complex integrated Raman lasers⁹ and simple geometrical configuration solutions.¹² Meanwhile considerable effort has been expended in creating and optimising power scavenging devices in the form of solar cells,¹³⁻¹⁸ some explicitly stating that their achievements are fully CMOS compatible.¹⁴ Finally, a few very important papers deal with the general, optical properties of silicon and this work has relied heavily upon them.¹⁹⁻²² They describe the phenomenon of free-carrier absorption in Silicon, as well as various properties of heavily doped silicon.²²

The sheer multitude of published material indicates much interest in this field, however none of those reported tackle the problem from the same angle as viewed in this paper. We wish to exploit free carrier absorption to create a CMOS-compatible communication platform that is capable of transmitting and receiving signals, as well as receiving power without the need of galvanic contacts.

In order to achieve such a system we propose to exploit free carrier absorption to modulate a beam of EM-radiation sufficiently strongly for signal transmission to become practicable. More specifically, we use a mid-IR

Further author information: Alexandru Serb, E-mail: alexandru.serb05@imperial.ac.uk

LED as a light source located underneath the CMOS IC we wish to probe. The beam enters through the bottom of the chip and travels through the silicon substrate towards the top surface, where the highly doped well and diffusion regions will create free carrier absorption. Finally, the beam is reflected back towards the underside of the IC using a layer of metallization. Beneath the IC, a photodetector receives the signal. By modulating the widths of the depletion regions in the pn-junctions that the beam passes through, sufficient light modulation occurs for reliable signal readout at the detector end. Data read-in to the chip can be achieved easily via a photodiode, and power requirements can conceivably be achieved using solar cells, (depending on the power requirements). We have already identified this in the literature showing that this is feasible.

This paper describes the theoretical basis for this concept and is organised as follows: section 2 describes the physics that renders our concept theoretically possible. Section 3 describes the engineering background, which constrains our endeavours to transfer such concept from theory into practice. Section 4 unveils the details behind the concept and illustrates how it may be applied in a practical situation. Section 5 places a finer point upon the details of the concept by examining the assumptions used and challenging them, and finally section 6 is a brief summary of the entirety of this paper.

2. PHYSICS BACKGROUND

The entire system of communications described in this paper is based on the phenomenon of free carrier absorption, as observed in Silicon. Free carrier absorption is a physical phenomenon whereby EM radiation attempting to cross a volume of semiconductor (non-depleted) suffers absorption. Subject to the doping concentration of p- and n-type silicon the phenomenon of free carrier absorption may reach sufficient intensity as to allow accurate detection of the losses sustained by an EM beam crossing such material even if the aforementioned material only boasts a thickness in the scale of microns.

The solution of Maxwell's equations for the propagation of an EM wave through a conductive medium has the form²³ :

$$\vec{E}(z, t) = \vec{E}_0 \exp\left(-\frac{\omega n_i z}{c}\right) \exp\left[i\omega\left(t - \frac{n_r z}{c}\right)\right] \quad (1)$$

where E is the electric field, E_0 is the base amplitude of the electric field, ω is the angular frequency of the EM wave, n_i and n_r are the imaginary and real refractive indices, z is the distance the beam traversed through the medium from the point where it's vector was given by $\vec{E}_0$, t is time and c is the speed of light. The 1st exponential represents amplitude attenuation. The 2nd exponential represents the 'slowdown' that the EM beam is subject to when crossing the medium. The energy/intensity of a wave is proportional to the square of it's amplitude:

$$I \propto |\vec{E}|^2 \Rightarrow I_{im} = I_0 \exp\left(-2\frac{\omega n_i}{c}z\right) = I_0 \exp(-\alpha z) \quad (2)$$

where:

$$\alpha = \frac{2\omega n_i}{c} \quad (3)$$

which is the absorption coefficient. Eq. (2) is also known as the Beer-Lambert law.

Now, Maxwell's equations for the propagation of an EM wave in a conductive medium of complex conductivity σ indicate that the complex refractive index can be expressed as:

$$n^2 = \frac{\epsilon\mu}{c^2} \left(1 + i\frac{\sigma}{\epsilon\omega}\right) \quad (4)$$

Since $n^2 = (n_r + n_i)^2 \approx n_r^2 + i2n_r n_i$ for $n_i \ll n_r$, we can use equations 3 and 4 to link the absorption coefficient to the conductive properties of the material:

$$\alpha = \frac{Re(\sigma)}{\epsilon_0 n c} \quad (5)$$

for the assumption that $n \approx n_r$.

The Drude model for the AC field of frequency ω expresses conductivity as:

$$\sigma(\omega) = \frac{n_e e^2 \tau / m_e}{1 - i \omega \tau} \quad (6)$$

where n_e is the free electron concentration, e is the charge of a single electron, τ is the relaxation time (average time between two electron collisions), m_e is the electron mass and carrier mobility is given by:

$$\mu = \frac{e \tau_e}{m_e} \quad (7)$$

This leads to the formula that describes free carrier absorption for free electrons:

$$\Delta\alpha = \left(\frac{e^3 \lambda^2}{4\pi^2 c^3 \epsilon_0 n} \right) \left[\frac{\Delta n_e}{m_e^{*2} \mu_e} \right] \quad (8)$$

which then is extended with the term that takes free hole absorption also into consideration and gives the general formula as cited by Soref,¹⁹ given here with a few alterations to the names of variables (explained below):

$$\Delta\alpha = \left(\frac{e^3 \lambda^2}{4\pi^2 c^3 \epsilon_0 n} \right) \left[\frac{\Delta N_e}{m_{ce}^{*2} \mu_e} + \frac{\Delta N_h}{m_{ch}^{*2} \mu_h} \right] \quad (9)$$

where α is the absorption coefficient related to the FCA (free carrier absorption) phenomenon, e is the charge of an electron, λ the wavelength of the incoming EM beam, c the speed of light, ϵ_0 the electric permittivity constant, n the refractive index of unperturbed crystalline silicon, m_{cx}^* the conductivity effective mass of either free electrons or free holes depending on the character marked here as 'x', N_x the corresponding doping concentration and μ_x the corresponding mobility.

The key focus points here revolve around the dependance on the square of the wavelength of the incoming EM radiation, the proportionality to free carrier concentrations (which equal the corresponding doping concentrations in undepleted semiconductor regions) and the inverse proportionality with respect to mobility. Everything else is non-engineerable.

A very influential paper addressing the free carrier absorption phenomenon in Silicon is Soref's work on Silicon electrooptics.²⁰ Soref's paper presents a most useful compilation of results and observations from other researchers plus some results generated by Soref himself, see Figure (1), which help visualise the phenomenon of free carrier absorption.

Suitable wavelengths for the implementation of our communications system would lie in the near or mid-IR range, specifically the 1.3-8 micron wavelengths where silicon is transparent. Table 1.

3. ENGINEERING BACKGROUND

The selection of the mobility and the doping concentration in the silicon is a matter of semiconductor engineering. However, the objective of this work has been to develop a communications platform that has the ability of operating in an unmodified CMOS process. As such, we assume no real freedom of selection when it comes to mobilities and doping concentrations with the exception of those readily available in commercial CMOS processes. To be more specific, we retain the freedom of choosing whether to utilise pn-junctions created by ion implantation or diffusion processes, whether to lay out our design so that we stress the generation of vast horizontal junctions (large modulating device area) or extended lateral junctions (large modulating device perimeter), or indeed which technology we wish to create our platform in (see Figure (2) and Table 2). Horizontal and vertical junctions of the same type (implantation or diffusion) will feature very different doping profiles across their surfaces Table(2).

Figure 1. The results of Soref's data compilation on the topic of silicon electro-optics.¹⁹ In the left panel we see the perturbation in the refractive index of silicon as a function of free carrier concentration, in the middle panel the perturbation in the absorption coefficient of silicon as a function of free carrier concentration and in the the right panel a typical doping profile (doping concentration vs. depth from the surface of the die). The left and middle panels are valid only for the wavelengths displayed on them. Same applies for temperature.

Table 1. Optical properties of undoped silicon stating the real and imaginary parts of the dielectric constant for a variety of wavelengths (and by extension also photon energies).

E(eV)	$\lambda(\mu m)$	ϵ_{real}	ϵ_{imag}
0.4	3.099	11.79279	0.00000
0.8	1.550	12.11502	0.00000
1.2	1.033	12.71086	0.00136
1.6	0.775	13.68177	0.03714
2.0	0.620	15.19384	0.12400
2.4	0.517	17.71621	0.26331

Figure 2. In this figure we can see a selection of the available junctions accessible in every CMOS technology. Junction legend: 1) Horizontal diffusion on well. 2) Vertical butting diffusion to diffusion. 3) Horizontal well-on substrate. 4) Vertical well on substrate. 5) Horizontal diffusion on substrate. 6) Vertical diffusion on substrate. Butting diffusion are not necessarily made inside a well, but can be obtained on substrate equally easily.

Table 2. Comparison of the junction types commonly encountered in CMOS. In every case, side 1 and side 2 represent the two sides of a possible pn-junction and thus their dopant type (p or n) will be complementary. Region type refers indirectly to the fabrication procedure used to create the corresponding region. Diffusion regions are created through a diffusion process whilst well regions are fabricated by means of ion implantation. The orientation column shows whether we are dealing with a horizontal or a vertical junction. The peak doping columns show typical values for doping concentrations that can be encountered in CMOS processes. They refer to consistent peaks rather than patches of semiconductor where the concentration of dopants may reach extremely high levels because of random fluctuation. The figures are only indications of orders of magnitude. The doping gradients columns show how the profile will vary as we move from a region with peak concentration of dopants towards the metallurgical point of the specified junction. The doping gradient for wells in the horizontal direction is unknown and will most certainly vary according to the angle of implantation. The exact relation is unknown.

Region type			Peak doping [cm^{-3}].		Doping gradient near metallurgical point.	
Term. 1	Term. 2	Orientation	Term. 1	Term. 2	Term. 1	Term. 2
Diffusion	Diffusion	Vertical	10^{21}	10^{21}	Follows Fick's law	Follows Fick's law
Diffusion	Well	Horizontal	10^{21}	10^{17}	Follows Fick's law	Gaussian
Diffusion	Well	Vertical	10^{21}	10^{17}	Follows Fick's law	N/A
Diffusion	Substrate	Horizontal	10^{21}	10^{15}	Follows Fick's law	Flat
Diffusion	Substrate	Vertical	10^{21}	10^{15}	Follows Fick's law	Flat
Well	Well	Vertical	10^{17}	10^{17}	N/A	N/A
Well	Substrate	Horizontal	10^{17}	10^{15}	Gaussian	Flat
Well	Substrate	Vertical	10^{17}	10^{15}	N/A	Flat

Whichever technology we settle upon, the values of the characteristic doping concentrations at different distances from the metallurgical surface for each type of junction, be it diffusion to well, well to substrate or any other type the manufacturing process allows, need to be known. Naturally these values must be known for both horizontal and vertical junctions. Knowing the characteristic mobility for each process is not as important given that we have little choice over the matter once we have decided on a technology platform. As such that may be treated as a parameter.

In implementing the system in CMOS we may also choose to engineer the back-end side of our die (the term 'back-end side of the die' referring to the metal interconnects and silicon oxide that lie above the surface of the silicon die, as opposed to 'front-end' which refers to the silicon substrate and any devices or structures we create in it). This simply consists of using a chosen metal layer to create a reflector that may turn a beam around when necessary.

Outside of the IC on which we choose to implement our design, there will be a set of external components that will enable the platform to operate. These include LEDs in the suitable wavelength range and photodetectors with the capability of detecting the radiation emitted by the aforementioned LEDs.

4. CONCEPT OF IR MODULATION IN CMOS

The very fundamental concept behind the proposed system is that by varying a reverse-bias electric field across a pn-junction, the width of the junction's depletion region is modulated. Therefore it stands to reason that by modulating the width of the depletion region we are able to alter the overall optical path 'resistance' that the beam is subject to during its trajectory from the emitter to the detector. So long as the rest of the environment remains unchanged this modulation should be the only perturbation to the overall absorption suffered by the beam on its path.

Considering this from an engineering standpoint, we choose to create a pn-junction in a CMOS process, connect it to an electrical, reverse bias signal we can directly control, then create a metallic reflector in one of the metal interconnect layers that lie in the back-end of the CMOS process and subsequently proceed to emit a beam of EM radiation from a suitably positioned LED situated underneath the die and record ipsilaterally from an equally suitably positioned photodetector. A picture illustrating this configuration may be seen here

Figure 3. Design configuration for the proposed system of communication. Where I_x represents the 'x'th part of an example beam's trajectory (the index changes every time the beam crosses from one material to another -Air, Si doped or not, SiO_2), R_x and R'_x represent intensity losses due to reflection effects, n_x represent refractive indices and the shaded areas in I_2 and I_4 are areas where the beam is subject to heavy optical losses due to free carrier absorption. Image taken from the original project proposal.

Figure 4. (a) Cross section of an IC and its environment, as engineered to fit into a microfluidics application, using the traditional wire-bonding approach. (b) The proposed optical coupling architecture. Image taken from the original project proposal.

in Figure (3), whilst an illustration of how this system would compare to a traditional wire-bond approach in a microfluidic application is shown here in Figure(4).

Having set the geometry, we may now proceed to specify other important parameters, such as the doping concentrations in the different regions of the die that the beam crosses. For example, using typical values we may define that the pre-doped substrate has a doping concentration of 10^{16} dopants/ cm^3 , any well it may encounter 10^{17} and any diffusion region 10^{21} . Given those values we can assign absorption coefficients to these regions for the chosen wavelength by using results shown in Soref's paper,¹⁹ reproduced in this figure (Soref's absorption vs doping curves). As such, radiation moving through our material shall be subject to Beer-Lambert style attenuation with the suitable absorption coefficient. Finally for this step, we assume abrupt junctions.

The width of the depletion region as generated by a range of input voltages. From Sze's textbook²⁴ the equation describing the depletion region as a function of doing concentration is:

$$W = \sqrt{\frac{2\epsilon_0\epsilon_r}{e} \left(\frac{N_A + N_D}{N_A N_D} \right) \left[\frac{kT}{e} \ln \left(\frac{N_A N_D}{n_i^2} \right) + V_{bias} \right]} \quad (10)$$

Where N_X is the doping concentration of acceptors (A) or donors (D), k Boltzmann's constant, T temperature, n_i the intrinsic carrier concentration of silicon and V_{bias} the applied bias voltage.

Using the charge neutrality equation, namely $x_A N_A = x_D N_D$, and the fact that $x_A + x_D = W$ we are able to deduce what portion of the depletion region encroaches on either side of the pn-junction. Knowing this we subtract these widths, corrected for beam angle vs the perpendicular to the junction, from the nominal path length of each beam within those respective regions. Meanwhile equation (9) tells us that the absorption coefficient will increase proportionally to the doping/free carrier concentration. As such, if we increase the doping concentration in a depleted region of semiconductor by a hundred-fold and assume $N_A = N_D$, then our ability to modulate the depletion region width under a certain ΔV will shrink by 10 times (eq. (10)), but the optical resistance the surrounding undepleted region will present to the incoming radiation will increase by a factor of 100 (eq. (9)). In effect by applying a reverse bias ΔV to the pn-junction, we are ridding the EM radiation of a 10x shorter, but 100x more resistant part of its path. This is a very important conclusion because it allows us to ignore what happens in the lightly doped region of a pn-junction provided the doping concentration in that region is significantly lower than what we would expect to find in the heavily doped region.

With this geometry and modelling equations in mind we may attempt to create estimates as to the modulation efficiency of our mechanism. For a start, we can create a table of preliminary figures linking the efficiency of the proposed mechanism of operation to the doping concentrations to be found at the test junction. In this case we assume the simplest possible conditions: abrupt junctions, typical doping concentrations that we would expect from a CMOS process and modulation occurring between a high and a low bias voltage level expressed as $\Delta I/I_0$, that is to say detected light intensity difference between the two states over the baseline intensity occurring when we apply 0V bias at the test junction. Results are given in Table(3).

Table 3. Calculated values for change in absorbance due to a reverse bias modulation of 5V magnitude for $\lambda = 1,55 \mu m$ and a step junction model. As calculated using eq. (10)

N_D	10^{20}	10^{20}	10^{19}
N_A	10^{20}	10^{19}	10^{19}
$\Delta I/I$	0,23%	0,06%	0,025%

Given the fact that doping concentration figures in the $10^{19} - 10^{21}$ dopants/ cm^3 region are typical for diffusion regions in CMOS and $10^{16} - 10^{18}$ are typical for well regions, the numbers from Table (3) seem to indicate that the FCA phenomenon is strong enough to be used to data transmission. Despite the significant decrease in modulation efficiency that comes with a drop in doping concentration, the values of doping used for the generation of these estimates are well within what we are used to observing in standard CMOS. With the backing of these estimates we may proceed to commit a more thorough investigation using a suitable simulator.

The assumptions used to create the simulator will determine how accurate and meaningful its outputs will be. To that end we begin by creating a geometry as is shown in Figure (5). In our set-up, a point light source, floating in air, emits EM radiation with some specified and equal radiant intensity in every possible direction. Some of that radiation hits the bottom surface of a silicon die where it submits itself to reflection and refraction according to the Fresnel equations. The radiation then travels upwards through pre-doped substrate silicon until some of it hits a 'target', which is simply our pn-junction. We must specify the geometrical size of that junction. For simplicity we assume a disk-shaped junction and reduce the problem to 2D. The radiation crosses the depletion region and continues its upward journey through a highly doped well or diffusion region that defines the opposite side of the junction. Having crossed that region as well, we simply ignore any reflective-refractive effects at the Si/SiO_2 boundary and allow the radiation to proceed unaltered in any way right up to the metal reflector where it submits itself to total internal reflection. The downward journey that follows unfolds similarly to the upward one, including diffraction and refraction upon the exit of the radiation from the silicon substrate and into the airgap. The collection of this light is made by a detector that sits beside the light source and at a certain distance from it. Knowing its size and distance from the light source we may calculate the arc of angles within which light emitted from the point source reaches the target, as opposed to any other part of the die, and on the return journey meets the detector, rather than just the air-gap or the light source itself. Making the

Figure 5. Geometry of the optical path. LEGEND: 0: Light source. 1: Arc within which emitted light hits the detector directly. Ignored under the assumption that measures would be taken to prevent such eventuality. 2: Arcs within which emitted light hits the target on the upbound journey and returns to the detector on the downward journey. 3: Arc within which emitted light hits the target on the upbound journey without necessarily hitting the detector on the return leg. 4: The edges of the photodetector. 5: The target at the top of the die (described in the main text) 6: Example of a single ray's path. This ray lies at the extreme end of the useful arc described in number 2 of this figure. 7: The bulks of the photodetector and the die. 8: Airgap.

additional assumption that the % losses suffered by the EM radiation on the upward and the downward legs of its trajectory are equal we further simplify our system.

The Fresnel relations:

$$R_m = \left(\frac{n \cos(\theta) - N \sqrt{1 - \left(\frac{n}{N} \sin(\theta)\right)^2}}{n \cos(\theta) + N \sqrt{1 - \left(\frac{n}{N} \sin(\theta)\right)^2}} \right)^2 \quad (11)$$

$$R_e = \left(\frac{n \sqrt{1 - \left(\frac{n}{N} \sin(\theta)\right)^2} - N \cos(\theta)}{n \sqrt{1 - \left(\frac{n}{N} \sin(\theta)\right)^2} + N \cos(\theta)} \right)^2 \quad (12)$$

where the first one refers to the reflection coefficient in the TM mode, and the second one to reflection in the TE mode. R_m is the TM reflection coefficient, R_e is the TE reflection coefficient, θ is the angle of incidence of the beam (= angle of departure since the refractive surface is perpendicular to the axis of symmetry against which the angle of departure is taken), n is the source-side refractive index (air) and N the target-side refractive index (silicon).

With this enhanced model of the geometry, we may now model the light that passes through the close proximity of the depletion region thus: The close proximity features a total width of Y microns, of which Y_D on the donor side and Y_A on the acceptor side of the junction. Of those, a certain $x_A(V_{bias})$ and $x_D(V_{bias})$ is

depleted, these variables denoting exactly the same quantities they did previously. It also holds that $x_A \leq Y_A$ and similarly for the donor side. This is another assumption that simply gives meaning to the Y-variable and effectively means that the ‘close proximity of the depletion region’ we encountered previously refers to those parts of the semiconductor that we can deplete if we so wish. Anything outside that close proximity we either do not wish to, or may not deplete without causing irreparable harm to the semiconductor. As such, everything outside that close proximity is not within the limits of our control, which enables us to simply include any alterations in intensity suffered by our test radiation in those off-limits regions with a steady state constant we shall call I_0 again. Meanwhile, within the close proximity we control, there will still be some Beer-Lambert extinction, however this occurs for $Y_D - x_D$ in the donor side of the junction, with donor-side rules, and for $Y_A - x_A$ in the acceptor side correspondingly. Nevertheless, in real CMOS processes, the sheer difference in doping between the two sides of typical junctions is enough to allow the simplifying process of ignoring the effects in the lightly doped side. As such our final (unsimplified) equation becomes:

$$I(end) = I_0 e^{(Y_D - x_D(V_{bias}))^2} e^{2(Y_A - x_A(V_{bias}))^2} \quad (13)$$

With the new meaning of I_0 . Naturally we may expand the equation to its full extent by replacing x_A, x_D with their full expressions from (10), with the help of the charge neutrality equation. The squares are there for the sole reason that the beam passes through each junction twice; once upwards, once downwards, as we’ve seen.

Putting this system together we create a simulator that receives geometric data and a bias voltage and outputs an detected light intensity. By testing for more values of the bias voltage we obtain various degrees of modulation. By selecting what type of junction we have we test for different junction types available in CMOS. By altering the dopings specified for various regions, we test for the sensitivity of the results to doping concentration.

This table details the results of the most characteristic tests Table(4). Note: Assumptions include that the junctions are abrupt and homogenous, i.e. the doping is exactly the same through the entire volume of each ‘diff’, ‘well’ and ‘sub’ region. To create a fair comparison between vertical and horizontal junctions we also assume that the total depleted volume that the rising radiation encounters when hitting the target is the same for a vertical, as it is for a horizontal junction. In other words, vertical junctions are geometrically speaking considered to be horizontal junctions taken apart into little pieces and placed throughout the bulk homogenously scattered upright and with the doping properties of a vertical junction. To help with the visualisation of this process, imagine that each horizontal junction is cut into small squares with a side length equal to the junction depth. Then these squares are made to stand upright. Finally, if the doping concentration in the heavily doped side exceeds that of the lightly doped area by more than 1 order of magnitude, then the modulation effects in the lightly doped side are ignored.

The noticeable drop in efficiency with decreasing doping concentrations is ever present. Moreover, we can see a significant drop in efficiency compared to the initial estimates in the preliminary results Table(3). This occurs because now more of the geometry has been taken into consideration (including the reflected beam). Much of the power of the emitter is going to be wasted to begin with (missing the target and then the detector), which explains why only about 7mW remain out of 35.

5. DISCUSSION

The results are fairly encouraging since modulation in the 0,01% region is still detectable without having to make use of excessive signal processing. As such, a communications system utilising this method of data transmission seems viable. Predictions state that diffusion-to-diffusion, otherwise known as ‘butting’ will generate the most satisfactory results, followed by diffusion-on-well junctions, worst performers being well-to-substrate junctions. Whether this prediction will be confirmed by facts or not remains to be seen.

In terms of physical sizes, these pins; we may call them ‘optical pins’, will probably end up featuring rather large areas. LEDs are already manufactured that feature wavelengths in the correct region and sizes of, for example 1,6x0,8mm.²⁵ Given the large size of these devices, we may simply use pn-junctions/pins of similar size and cluster a group of 4 around a single LED. That way 4 pins will share a single light source Figure (6). A group of photodetectors will then be arranged suitably around the emitting LED and shielded from direct irradiation

Table 4. Simulated results. The conditions assumed are to the left. To the right we see the results for various types of junctions. Junction type strings mean diffusion for 'diff', well for 'well' and lightly doped substrate at 10^{15} dopants per cm^3 for 'sub'. The final figures in the columns for bias voltage equal to 0 or 5 Volts indicate the estimated power reaching the detector from the light source (in mW) and the very last column indicates the modulation in terms of power in ppm.

GEOMETRIC/PHYSICAL CONDITIONS		Junction		V = 0V	V = -5V	DV %
		Type	Orientation			
Target size	0,5mm	Diff-diff	Vertical	6.887926	6.893047	0.074292
Detector distance from light source (either side).	50 microns	Diff-well	Horizontal	6.883873	6.883991	0.001714
		Diff-sub	Horizontal	6.883926	6.883938	0.000174
		Well-well	Vertical	7.029387	7.029404	0.000384
Light source and detector surface to refractive index distance.	100 microns	Well-sub	Vertical	7.029377	7.029378	0.000014
		Well-sub	Horizontal	7.029377	7.029378	0.000014
Die thickness	300 microns					
Air refractive index.	1					
Silicon refractive index.	3,5					
Light source power.	35mW					

from the LED. To each pin there will be a corresponding photodetector. This may be large in comparison to standard wire-bond pins standing at tens of square microns, however the benefit of having all communication occurring on the nether side of the die may more than compensate for that in certain applications.

Naturally, there are many phenomena that have been left unaccounted for. Challenging our previous assumptions might reveal important information. The most important assumption we made concerned the exact nature of the doping profile in the vicinity of our junctions. We assumed rather simplistic abrupt junctions. However, in reality diffusion regions will exhibit doping profiles created under the government of Fick's law on diffusion, whereas well regions created by implantation shall exhibit Gaussian doping profiles. The aforementioned values of 10^{21} dopants/ cm^3 for diffusion regions and 10^{17} for well regions are characteristic of locations deeply within those regions, not near their borders. In reality, the doping concentration will decline as one approaches the metallurgical point of a pn-junction where the net doping concentration is zero. On the other hand, the depletion region will invade both sides of the junction and climb upwards towards regions of higher and higher doping concentration. The doping concentration at each edge of the depletion region is crucially important, since any modulation occurring in the depletion region width will be occurring in material of roughly that very same doping concentration. As such, the doping concentrations we should be using when we implement our equations about depletion region width modulation and by extending light modulation, should be these 'effective' edge concentrations. The practical implications of this realisation are enormous. In effect, the doping concentrations we are working with are substantially lower than what we initially expected. This might push the modulation vs baseline intensity ratio in the ppm region.

Along similar lines, the light source will most certainly not be of a homogenous, point character, there will be losses and reflection at the Si/SiO_2 boundary, the junction will most likely not be in the shape of a disk etc. Nevertheless, assuming we use pins that are significantly larger in size as compared to typical feature sizes associated with CMOS (distance between the 1st metal layer of the back-end and the die, depth of a well junction etc.; all smaller than a few microns) these effects vanish into insignificance. Other assumptions such as the symmetry of the ascending and descending light pathways and the fact that depleted semiconductor regions offer no resistance to the crossing EM radiation stand to reason anyway.

Finally, in terms of applications, this communications platform offers some advantages. First of all, in combination with wireless data read-in techniques (external LED to integrated photodetector) and power transmission techniques (Light source to power scavenging photodetector), the need for bond-wires is eliminated. This leaves

Figure 6. Example of how a configuration for emitter/targets/detectors can be implemented so that a single emitter services 4 targets and detectors i.e. 4 communication channels. The yellow square on the grid marks the spot where the LED will be positioned. The dark blue squares denote areas where the photodetectors will be placed. The light blue squares are not significant in the design. The green squares hovering above the 9-square grid below denote targets, i.e. pn-junctions that carry out modulation. Two light beam pathways have been drawn to illustrate the concept more clearly.

us with advantages in the domain of replacing ICs when needed. Moreover, in the domain of microfluidics, ICs manufactured to utilise this system of communications can be produced and placed into service without the need of using wire-bonds, or going through any of the effort required to maintain such wires protected from the liquid that is meant to be flowing on the surface of the IC. Instead, the IC can be kept in a specially carved notch on a panel or PCB by virtue of suction applied to it from beneath, thus leaving all communication and power transmission to occur on the nether side of the die wirelessly (as already seen in Figure 4).

6. SUMMARY

In conclusion, in this paper we have examined the theoretical foundations of a proposed communications platform between an IC and an external panel by means of wireless, optical coupling. We have panned over initial theoretical results, analysed the outputs of a simple, purpose-built simulator and challenged our own assumptions. Despite any indications that the phenomenon may turn out to be significantly weaker than expected, the robustness of the physics behind the concept gives us confidence that given sufficient fine-tuning and signal processing this system may be realised in practice.

ACKNOWLEDGMENTS

This work was supported by the UK Engineering and Physical Sciences Research Council (Grants ref: EP/G070466/1 and EP/H024581/1).

REFERENCES

- [1] Liao, L., Liu, A., Rubin, D., Basak, J., Chetrit, Y., Nguyen, H., Cohen, R., Izhaky, N., and Paniccia, M., “40 gbit/s silicon optical modulator for high-speed applications,” *Electronics letters* **43**(22) (2007).
- [2] Xu, Q., Schmidt, B., Pradhan, S., and Lipson, M., “Micrometer-scale silicon electro-optic modulator,” *Nature letters* **435**, 325–327 (2005).
- [3] Cutollo, A., Iodice, M., Spirito, P., and Zeni, L., “Silicon electro-optic modulator based on a three terminal device integrated in a low-loss single-mode soi waveguide,” *Journal of lightwave technology* **15**, 505–518 (1997).
- [4] Gao, Y., Wong, S., W, C., Shao, G., and Homewood, K., “Effect of implantation temperature on dislocation loop formation and origin of 1.55- μ m photoluminescence from ion-beam-synthesized fesi₂ precipitates in silicon,” *Applied physics letter* **83**(1), 42–44 (2003).
- [5] Snyman, L. W., Plessis, M., Seevinck, E., and Aharoni, H., “An efficient low voltage, high frequency silicon cmos light emitting device and electro-optical interface,” *IEEE Electron Device* **20**(12), 614–617 (1999).
- [6] Green, M., Zhao, J., Wang, A., Reece, P., and Gal, M., “Efficient silicon light-emitting diodes,” *Nature* **412**, 805–808 (2001).

- [7] Priolo, F., Franzo, G., Coffa, S., and Carnera, A., "Erbium implantation in silicon: from materials properties to light emitting devices.," *Elsevier materials chemistry and physics* **54**, 273–279 (1998).
- [8] Homewood, K. and Lourenco, M., "Light from si via dislocation loops.," *Materials today* (January), 34–39 (2005).
- [9] Rong, H., Kuo, Y. H., Xu, S., Liu, A., Jones, R., and Paniccia, M., "Monolithic integrated raman silicon laser," *OPTICS EXPRESS* **14**(15), 6705–6712 (2006).
- [10] Lourenco, M. and Shao, G., "On the role of dislocation loops in silicon light emitting diodes.," *Applied physics letters*. **87** (2005).
- [11] Milosavlevic, M., Lourenco, M., Shao, G., Gwilliam, R., and Homewood, K., "Optimising dislocation engineered silicon devices.," *Applied physics B, Lasers and optics*. (2006).
- [12] Plessi, M., Aharoni, H., and Snyman, L., "Two- and multi-terminal cmos/bicmos si leds," *Elsevier optical materials* **27**(5), 1059–1063 (2005).
- [13] Warneke, B., Scott, M., Leibowitz, B., Zhou, L., Bellew, C., Chediak, A., Kahn, J., Boser, B., and Pister, K., "An autonomous 16 mm³ solar-powered node for distributed wireless sensor networks," *Sensors, 2002. Proceedings of IEEE* **2**, 1510–1515 (2002).
- [14] Fish, A., Hamami, S., and Yadid-Pecht, O., "Cmos image sensors with self-powered generation capability," *IEEE transactions on circuits and systems* **53**(11), 1210–1214 (2006).
- [15] Guilar, N., Kleeburg, T., Chen, A., Yankelevich, D., and Amirtharajah, R., "Integrated solar energy harvesting and storage.," *IEEE transaction on very large scale integration (VLSI) systems*. **17**(5), 627–637 (2009).
- [16] Arima, Y. and Ehara, M., "On-chip solar battery structure for cmos lsi.," *IEICE electronics express*. **3**(13), 287–291 (2006).
- [17] Wu, H., Emadi, A., Graaf, G., Leijtens, J., and Wolffenbuttel, R., "Self-powered sun sensor microsystems.," *Proceedings of the Eurosensors XXIII conference* , 1363–1366 (2009).
- [18] Perenzoni, M. and Gonzo, L., "Solar-powered cmos image sensor.," Sent for publication to 'Electronics letters' journal. (August 2009).
- [19] Soref, R. A. and Bennett, B. R., "Electrooptical effects in silicon," *IEEE journal of quantum electronics* **QE-23**(1), 123–129 (1987).
- [20] Soref, R. A., "Silicon-based optoelectronics," *Proceedings of the IEEE* **81**(12), 1687–1706 (1993).
- [21] Schroder, D., Thomas, N., and Swartz, J., "Free carrier absorption in silicon.," *IEEE journal on solid state circuits* **SC13**, 180–187 (1978).
- [22] Isenberg, J. and Warta, W., "Free carrier absorption in heavily doped silicon layers.," *Applied physics letters*. **84** (2004).
- [23] R. P. Feynman, e. a., [*The Feynman lectures on physics.*], vol. 2, Addison-Wesley (1964).
- [24] Sze, S. M., [*Physics of Semiconductor Devices*], Wiley, 2nd ed. (1981).
- [25] "Sml-31 datasheet." Datasheet (Feb. 2010).