An Ultra Low Power Low Noise Chopper Amplifier for Wireless EEG

(Invited Paper)

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Abstract—The realisation of wireless EEG systems suitable for long term monitoring requires low noise, low power and low voltage circuit design. Presented in this paper is a 1 V, 1.4 μ W chopper amplifier implemented in a 0.35 μ m CMOS process. The achieved input referred noise voltage is 1.5 μ V rms and the gain is 44 dB. Since the dynamic range of the input EEG signal is dominated by the offset voltage generated at the electrode-tissue interface, a novel input high pass filter has been designed. The required filter capacitance is limited to 40 pF by recognising that the input chopper switches can be combined with the amplifier input capacitance to emulate a large resistance.

I. INTRODUCTION

Electroencephalography (EEG) plays a vital role in the diagnosis and treatment of neurological diseases such as epilepsy. Currently patients are normally monitored in-house with hard-wired cumbersome equipment for no more than 24hrs, resulting in limited data for diagnosis and assessment [1]. There is thus a strong need for the development of lightweight, wearable and wireless EEG systems to enable the long-term monitoring of patients in their everyday environment [1]. To meet the stringent size and weight constraints of a wearable system operation from a single miniature and perhaps flexible cell, such as those available from [2], is desirable. This demands ultra-low power and low voltage circuit design.

Scalp EEG signals exhibit amplitudes between about 1 μ V and 500 μ V [3] at frequencies below about 30 Hz [4]. CMOS is the technology of choice for low cost low power system-on-a-chip solutions [5]. The high flicker noise exhibited by CMOS devices demands much attention from the designer to achieve the required signal-to-noise ratio. A further challenge is caused by the EEG electrodes, which generate dc offset voltages typically in the tens of millivolts [6]. Being about 1000 times the actual signal, this dc offset will dominate the dynamic range if it is not rejected before amplification.

A. Specifications

The performance of the front end amplifier is key to any data acquisition system. The power, voltage supply and noise constraints combined with a signal dominated by offset make the design of this amplifier particularly challenging. An rms

input referred noise voltage of less than 2 μ V is required for a dynamic range of 8 bits. The gain should be between 40 dB and 50 dB to achieve the required resolution with an ultra low power analogue-to-digital converter, such as that presented in [7], whilst ensuring that the amplifier does not saturate. The current drain should be no more than a few microamps at 1 V supply and the large DC offset must be rejected in order to achieve the required dynamic range.

B. Current State of the Art

A brief review of the current state of the art demonstrates the trade-offs in achieving the above specifications. For instance, the chopper amplifier reported in [8] achieves an excellent rms noise voltage of only 260 nV over a 600 Hz bandwidth yet consumes 3 mW at a 5V supply. Employing a current feedback approach, [9] achieves a much lower current drain of only 31 μ A but the circuit exhibits a significantly higher rms noise voltage of 13 μ V integrated from 0.5 Hz to 500 Hz. An active high-pass filter is also implemented in [9]. The current mode amplifier reported in [10] achieves an impressive 1.27 μ V rms noise voltage over a 200 Hz bandwidth at 1 V supply, whilst also implementing an active DC rejection circuit. The power consumption is still relatively high at 50 μ W. Returning to the chopper technique, [11] reports a 891 nV rms noise voltage over a 200 Hz bandwidth for a power consumption of 34 μ W and a high supply voltage of ± 7.5 V. The EEG bandpass amplifier reported in [12] consumes only 900 nW, achieves an rms noise voltage of 1.6 μ V and rejects the DC offset, yet operates from a ± 2.5 V supply.

II. CHOICE OF ARCHITECTURE

At least one of the desired specifications is not met by each of the designs reported in the literature. Despite the promising performance of the amplifier presented in [12], at ± 2.5 V it is not suited to low voltage operation. The low noise strategy employed relies on certain transistors operating in strong inversion and the design also uses a complimentary cascode at the output. With the headroom available at 1 V it is unlikely, in the authors' opinion, that this circuit could achieve the required noise performance.

A chopper amplifier achieves exceptional noise performance and a very low offset voltage by upconverting the signal before amplification through modulation with a square wave at the chop frequency, f_c . Ideally, f_c is set to a frequency at which the flicker noise is negligible. After amplification at the chop frequency, f_c , the signal is downconverted to baseband, whilst flicker noise and any amplifier offset voltage are simultaneously upconverted to the chop frequency, where they can be filtered out.

The diagram shows a two-stage CMOS differential amplifier. The first stage is a differential pair with NMOS transistors connected to a common source resistor and PMOS transistors connected to a differential pair load. The second stage is a differential pair with NMOS transistors connected to a common source resistor and PMOS transistors connected to a differential pair load. The output is taken differentially from the PMOS nodes. Labels include C_F , ϕ_1 , ϕ_2 , V_{in} , V_{out} , and Reference.

III. OFFSET REJECTION

From switched capacitor theory it can be seen that the input chopper switches combined with the input capacitance of the differential amplifier emulate a resistor, R_F . The equivalent circuit is shown in figure 2. C_F and the effective resistance,

The diagram shows a circuit with two internal nodes. A voltage source V_{in} is connected to the first node through a capacitor C_F . The current entering the first node is i_{in} . The voltage at the first node is V_F . The first node is connected to the second node through a switch labeled ϕ_1 . The current flowing from the first node to the second node is i_1 . The second node is connected to ground through a switch labeled ϕ_2 and a capacitor $C_{in,1}$. The first node is also connected to ground through a switch labeled ϕ_2 and a capacitor $C_{in,2}$. The current flowing from the first node to ground through $C_{in,2}$ is i_2 .

Fig. 3. Differential amplifier

M_4 operate in weak inversion, being $36 \mu\text{m}$ (W) by $4 \mu\text{m}$ (L). The square of the equivalent gate referred channel noise voltage, v_n^2 , for a MOS transistor in weak inversion is given by [14]:

$$v_n^2 = \left[\frac{2kT(1+\eta)}{g_m} + \frac{KF}{f \cdot C'_{ox} \cdot WL} \right] \cdot \Delta f \quad (3)$$

where k is Boltzmann's constant, T is the absolute temperature, η is the ratio of the body-source transconductance, g_{mbs} to the gate-source transconductance, g_m , KF is an empirical flicker noise parameter, C'_{ox} is the oxide capacitance per unit area, W is the device width and L is the device length.

The square of the equivalent input referred noise voltage, v_{eq}^2 , of a MOS differential amplifier is [13]:

$$v_{eq}^2 = v_{n1}^2 + v_{n2}^2 + \left(\frac{g_{m3}}{g_{m1}} \right)^2 \cdot (v_{n3}^2 + v_{n4}^2) \quad (4)$$

where v_{nk} is the gate referred channel noise voltage of transistor M_k .

To minimise noise in this circuit there is little option but to increase the drain current. The noise will be predominantly thermal due to the frequency upconversion process and the transconductance in weak inversion can only be improved through increased drain current. Unlike strong inversion operation, this results in the ratio of device sizes being unimportant. (It should be noted that these assumptions are not completely true for this implementation since the chop frequency is relatively low at 500 Hz and transistors M_1 and M_2 actually operate in weak to moderate inversion.)

Transistors M_5 , M_6 , M_7 , M_8 and M_{10} form a second stage differential amplifier which provides the gain. Here the transistors are much larger than those of the first stage to ensure that mismatch and process variation has little effect; M_5 and M_6 are $72 \mu\text{m}$ by $10 \mu\text{m}$, M_7 and M_8 are $160 \mu\text{m}$ by $8 \mu\text{m}$. The current through each branch is 400 nA, sufficient for the second stage noise to be insignificant.

The differential output of the first stage is high pass filtered to control the input common mode of the second stage and

to reject offset voltage due to mismatch or process variation. The output is also high pass filtered before downconversion. The filtering is done using the diode connected $4 \mu\text{m}$ by $4 \mu\text{m}$ PMOS devices, M_{R1} , M_{R2} and M_{R3} , which form an extremely high incremental resistance ($> 10^{11}$) as described in [12], in conjunction with capacitors C_1 , C_2 and C_3 . C_1 and C_2 are 10 pF and C_3 is 1 pF. C_1 and C_2 are set to the higher value of 10 pF to reduce the capacitive division with the input capacitances of the next stage.

V. SIMULATION RESULTS

The circuit has been simulated in SPECTRE RF, using the transient, PSS, PAC and PNOISE analyses. Figure 4 shows the dependence of the input filter corner frequency on f_c . The chop frequency was chosen as 500 Hz as a good compromise between low cut-off frequency and effective flicker noise upconversion.

Fig. 4. Input filter transfer function for different values of f_c

Figure 5 shows that the amplifier has a midband gain of about 44 dB and a bandwidth of over 1 kHz.

Fig. 5. Gain and bandwidth

Figure 6 compares the noise performance of the amplifier in figure 3 operated with and without the chopper. Without the chopper the input referred noise voltage integrated from 0.5 Hz to 30 Hz is $5.54 \mu\text{V rms}$. Use of the chopper reduces this to only $1.5 \mu\text{V rms}$ by upconverting the low frequency flicker noise. The resulting output spectrum is explained in [11].

Fig. 6. Noise voltage comparison

Figure 7 shows the filtered transient output voltage for a 20 Hz, $100 \mu\text{V}$ input sinusoid with 20 mV of dc electrode offset.

VI. CONCLUSION

This paper has introduced a chopper amplifier design capable of achieving the required performance for a wireless EEG system. The circuit achieves a noise voltage of $1.5 \mu\text{V rms}$, a gain of 44 dB for a 1 V supply and a power consumption of $1.4 \mu\text{W}$. A DC rejection circuit is successfully implemented whilst keeping the total capacitance to only 61 pF.

Fig. 7. Filtered output transient voltage

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