A New Protection Model for Component-Based Operating Systems

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Abstract

This paper describes a new model of program protection particularly suited to component-based operating systems. Instead of the traditional separate user and kernel processor modes and paging, segmentation is combined with a simple software technique to avoid the use of separate processor modes while maintaining full protection. This new model offers dramatically improved performance, simplified and improved architectures and increased flexibility.

A component-based OS (called Go!) has been implemented using such techniques and early experiences with it are described in this paper. In this paper we show that Go! offers fully protected round-trip RPC in just 85 cycles on the Pentium, and the single processor mode allows the Object Request Broker (Go!'s analogue of a kernel) to be responsible only for component management. We show that such a system allows multithreading, device management, and even interrupt handling to be provided by separate 'application level' components without compromising protection.

1 Introduction

Traditional operating system kernels (monolithic and micro) are amorphous masses of code supporting several monolithic processes. Over the last year or two, several operating system kernels have been developed which exhibit component-based behaviour themselves [3, 11]. Here the kernel is replaced with a nucleus — a nano-kernel which manages components and their interaction. All other services are moved out into components which execute in user mode. However, certain services which have nothing to do with component management (e.g., interrupt and device management) must be provided by the nucleus because only it has sufficient privileges. That is, separate processor modes prevent protection being cleanly separated from management [8].

This paper examines protection in such systems, and proposes a novel protection model. The new

model allows improved performance, flexibility and software engineering. As a proof of concept, a new OS (Go!) has been developed using such a model. Early experiences with Go! are also reported.

Section 2 of this paper introduces component-based operating systems. Section 3 examines traditional OS protection, including separate processor modes, paging and segmentation. Section 4 describes how protection can be realised with a single hardware privilege level if segmentation is combined with a simple software technique, and section 5 addresses limitations of this model and explains how they can be overcome. Section 6 introduces Go! and its protection model. Section 7 gives some preliminary results from early experimentation with Go!, and section 8 concludes.

2 Component-base operating systems

This section introduces a new breed of operating systems: *component-based systems*, and explains briefly their advantages.

Over the last few years applications have changed. With modern component technology such as CORBA [13], Java [12] and COM[5], the boundaries between applications have become blurred and software is becoming a collection of cooperating *components*. For example, when using a Java applet inside your web-browser, you are not using a single application, but the web-browser, the Java VM and the Java applet.

A component is defined here as an object encapsulating state and behaviour in order to achieve some specific task. Components are isolated and protected from one another, as with conventional processes. Components differ from processes in that they are typed, each component realising at least one *interface*, which defines the operations available on that component. There are zero or more *implementations* of each interface, and several *instances* of each implementation may be created and destroyed dynamically. Components often use object-oriented techniques such as *interface-inheritance* and *polymorphism*. Compo-

nents differ from objects in that they are protected from one another and are fundamental building blocks of the operating system as well as applications.

For some time now, the benefits to software engineering of object-orientation and componentisation have been widely recognised. However, systems programmers have been denied these benefits. This is particularly ironic since OS programming is notoriously difficult and error-prone.

Over the last decade several object-oriented operating systems have been developed. This might mean the kernel was written in an object-oriented fashion (perhaps using C++) as with Choices [2], that the OS was tailored specifically to suit object-oriented applications (e.g., Clouds [6]) or that the OS used an orthogonal object-model in user and kernel space as in Spring [20].

During the last few years, several component-based operating systems have materialised [3, 11]. These abandon the tradition of a kernel supporting processes for a nucleus managing many user components.

Componentising operating systems has several advantages: system development is made considerably easier by the improved software engineering; such OSs have the potential to be more robust (due to finer-grained protection); they are more flexible (components can enter and leave the system at will); and they provide better support for modern component-based applications.

3 Traditional OS protection

Many modern operating systems offer protection to applications. This section describes briefly what protection means, and how traditional operating systems (such as Unix) provide it. Protection means that a buggy or malicious application is unable to bring the entire system down: it may only affect itself and those applications dependent on it. Protection needs support from the microprocessor as well as the operating system. In order to afford protection:

1. applications must be prevented from executing certain privileged instructions (e.g., disabling interrupts, since this would prevent the currently executing thread from being preempted, possibly live-locking the entire system).
2. applications must be prevented from accessing memory which they should not (e.g., another application's private memory).

Traditionally, these two aspects of protection have been provided by separate *processor modes* and *paging* respectively, both of which are described below.

By providing different privilege modes, microprocessors can catch unprivileged applications attempting to execute privileged instructions. All applications run in *user mode*, meaning that the attempted execution of a privileged instruction will alert the operating system (usually via a dedicated interrupt or *exception*). The OS executes in the *kernel* operating mode, in which any instruction may be issued. Special instructions are provided to enable user-code to call kernel-code in a controlled fashion. These instructions atomically switch to kernel mode and take control to well-known entry-points within the kernel, meaning applications cannot put themselves into kernel mode. Such a transfer of control to kernel mode is typically known as a *system call*.

Paging divides memory up into a series of fixed sized regions called *pages*. Each page (typically 4kB) has associated with it a set of access protection bits that specify whether a page is readable, writable, or executable. Any violation of these protection bits (e.g., attempting to write to a read-only page) is detected by the hardware and the operating system is alerted (usually resulting in the termination of the offending process).

There is another, less widely used, mechanism to prevent illegal memory access: segmentation. With segmentation, rather than grouping memory into a set of fixed size pages, memory is grouped into several variable sized, contiguous regions called *segments*. Each segment starts at an arbitrary address in physical memory, known as the *linear base address*. There are usually several different types of segments, including read/write and read-only data segments, stack segments, and code segments. A segment's *descriptor* identifies its linear base address, size and type. A *descriptor table* describes each segment in the system. A segment is identified by a *selector*, which is an index into this table. The processor contains several segment selectors in dedicated registers, often including a current data segment, code segment and a stack segment. Each memory reference is an offset into a particular segment, either identified explicitly or implicitly based on the instruction type. E.g. `JMP 50` will jump to offset 50 of the current code segment (linear address `code_segment.base + 50`). `JMP 8:30` would transfer control to offset 30 of the segment identified by selector 8 (`code_segment <- descriptor_table[8] ; PC <- 30;`). Any attempted illegal operation on a segment (e.g., accessing beyond its limit, or attempting to write to a read-only segment) alerts the operating system as with illegal instruction execution or page faults. Applications are free to load any segment

available in the descriptor table. On a context switch the OS kernel manipulates the descriptor tables in a fashion analogous to the way paged kernels manipulate page tables.

Paging is more popular than segmentation for several reasons: segmentation leads to external fragmentation; it complicates programming; and due to common misunderstandings. Adding paging orthogonally behind segmentation [17] can resolve the first two issues:

Figure 1: Orthogonal Segmentation and Paging

Combining segmentation with paging solves the fragmentation issue since segments are no longer required to exist in contiguous physical memory. This can actually *reduce* fragmentation over simple paging since paging causes *internal* fragmentation (unless all objects are page sized, or multiples thereof). In the case of single address space systems each segment still has the full virtual address range (4 GB on 32 bit systems), alleviating fragmentation of the virtual address space.

Segmentation complicates programming since pointers to objects must be dereferenced via the appropriate segment. This is particularly cumbersome when taking addresses of objects in the stack segment. Paging can be used to allow the data segment and stack segment to appear to overlap each other. This has slight space and time costs, but the programmer has the choice of whether or not to pay this price.

The misunderstanding about segmentation comes from the so-called segmentation offered by early Intel x86 microprocessors. The only thing the 8086 scheme has in common with real segmentation is its name: in reality this was a hack to allow a 16 bit machine to address a megabyte of memory. The Intel 80386 and up (aka IA32) provide orthogonal segmentation and

paging as described above.

Segmentation also means that components can exist in a single address space without requiring relocation on instantiation. This is because each component's data are linked at zero, relative to their data segment — the linear base address of a component's data segment effectively relocates it. In paged single address space systems, applications need to be relocated at load time, increasing load times and system complexity.

4 A new protection model

This section describes why traditional protection models are poorly suited to component-based systems and introduces a more suitable alternative: segmentation and a single processor privilege mode. The new model provides complete protection with several significant advantages.

Assuming that componentisation is desirable, then the finer-grained and more widespread componentisation can become, the better. Also, since encapsulation is one of the most fundamental aspects of componentisation, it is reasonable to stipulate that a component-based OS should provide protection on the basis of components (i.e., a component's data should be accessible to its code exclusively).

The separation of user mode and kernel mode implemented by modern microprocessors (referred to here as the 'system call barrier') works well for traditional kernel operating systems. Older object-oriented OSs such as Spring [20] use an identical object-model in both user and kernel mode, but the system call barrier renders the object-model of each side invisible to the other. This means that the benefits of object-orientation of applications are denied to the kernel, and vice versa. Modern component-based operating systems work hard to hide the distinction between user mode and kernel mode¹. The system call barrier imposes both architectural and performance bottlenecks on such component-based systems and thus is an inappropriate protection mechanism.

In the new model, all components and an Object Request Broker (ORB — the analogue of a kernel) execute in a single processor mode (with full privileges). However, most components are prevented from containing any instructions that would be illegal in user mode. This is accomplished by scanning a component's code section on loading, and rejecting components which contain instructions that they are not

¹Whether a component executes in kernel mode or user mode is of concern to its implementation only; it should not be possible to determine from the outside in which mode a component operates since this makes no difference to a component's client.

sufficiently privileged to execute. Such scanning takes only a few cycles per instruction, and needs to be performed just once per implementation type (when it is installed on the system).

If the code-scanning technique is extended to prevent applications loading segment registers with arbitrary values (restricting such privileges to the ORB) then holding a segment's selector in a segment register is effectively a capability to access that segment [18]. Context switching is made much more efficient too: rather than the usually expensive manipulation of complicated page/descriptor tables to effect a context switch, the ORB simply loads the code, data and stack segment registers with new values (approx. 3 cycles each on the Pentium). This also prevents the problem of self-modifying code (and so preventing applications changing themselves to gain privileges) since they are unable to load the code segment selector into the data segment register. Components are prevented from calling others arbitrarily because inter-segment jumps are classed as segment register loads and so prohibited by the code-scanning technique described above. However, to allow components to call the ORB at well-known entry-points, a few immediate inter-segment jumps are permitted (e.g. `call 0:0` calls offset zero of the segment at zero, transferring control to a well-known entry-point and swapping contexts atomically: the analogue of a system call).

This has the advantage of avoiding the often costly penalties of traversing processor modes on most interrupts as well as system calls, and also of removing the architectural bottleneck imposed by the system call barrier. The technique is also more flexible: components can be allowed restricted use of some privileged instructions but not others (e.g., a device driver might be permitted use of certain I/O control instructions but not the ability to clear interrupts).

The ORB handles component management only — i.e., instance creation/destruction, type (un)installation and inter-component method invocation/return. Application level components are used to manage devices, paging, and even to handle interrupts. Note that handling interrupts in this case does not mean that the ORB receives interrupts and dispatches them to handler components: because applications/components execute in kernel-mode the ORB can remain entirely ignorant of interrupts. This is possible in this model as such components can be allowed to contain the relevant privileged instructions. The use of separate processor modes to realise protection (as with other systems) restricts further componentisation of the nucleus. The nucleus needs

to be involved in interrupt/fault handling, thread preemption, and paging, since such tasks require the use of privileged instructions. However, these tasks are quite separate from component management, and so ideally, should be separated out into other components.

Note the different terminology: traditional systems use *kernels*, which manage processes and devices; modern component-based systems use a *nucleus* which is primarily responsible for component management, but must perform other tasks which require the processor's kernel mode (e.g. interrupt dispatching); and our model uses an *ORB* which is responsible for component management only.

Segmentation also has the obvious advantage over paging of not wasting space for inconveniently-sized objects since segments are variable size. This is especially useful for finely-grained component-based systems².

Note that the use of a single processor mode is not the same as downloading code into the kernel [1]. In reality everything executes in kernel mode, so one might argue everything is downloaded into the kernel. However, our concept is different: there is no kernel/user mode divide at all; one could equally argue that all code is uploaded out of the kernel.

5 Limitations of this model

This section introduces the few limitations of the model, and explains how they can be overcome.

This protection mechanism does not address the halting problem (i.e. where a server goes into an infinite loop, never returning control to its client) since it has been shown to be algorithmically insoluble [21]. Instead callers must arrange to respond to some watchdog timeout if they do not trust their callee to return (no different from traditional protection models).

This technique prevents self-modifying code since such code could break security after it had been installed. It also prevents arbitrary data being embedded in code sections, as such data might appear to be privileged instructions. However, both these techniques are very rarely used in modern computing, and modern microprocessors severely penalise the use of such techniques anyway [16]. Hence these penalties are considered worth the price in most situations. In the unlikely case that these techniques are required,

²Given uniform distribution of component sizes, on average $\frac{1}{2}nP$ bytes are wasted (where n is the number of components, and P the page size). n increases the finer the granularity, so that this figure becomes significant for finely-grained systems.

these few components could be run in some less privileged mode. Note that this system does *not* preclude dynamic code generation (such as a Java JIT).

Finally, machines with variable-length instructions expose a flaw in this system because immediate data can be executed as if they were instructions. For example, take the code: `mov al, 0xFA; jmp -2`; The first instruction places FAh into general purpose register `al`, and the second jumps back to the `mov` instruction (the first instruction consumes two bytes, hence `-2`). This will cause the executing thread to live-lock, but will not affect the system as a whole. Now take: `mov al, 0xFA; jmp -1`; This jumps into the middle of the `mov` instruction, and attempts to execute the immediate data FAh. FAh is the opcode to disable interrupts on Intel x86 processors so this sequence of instructions will lock the entire system until it is reset. The best solution to this is to use a processor with fixed-length instructions (e.g. any RISC machine). However, this can be overcome even on CISC machines by using more advanced code-scanning techniques, such as Proof-Carrying Code [19].

6 Go! : A single mode protected component-based system

This section describes Go!, a native operating system implemented on the Pentium. Go! was developed as a proof of concept vehicle of the protection mechanism described in this paper.

In many ways, the Pentium is a poor choice of architecture on which to implement Go!, mainly because of its CISC architecture (and therefore variable-length instructions). However, the Pentium was chosen despite this disadvantage since Go! is a proof of concept vehicle only, and the huge amount of free OS development resources as well test machines at our disposal would significantly simplify development.

Go! itself consists purely of the ORB, which deals with component management only. A library operating system called GTE (Go! Test Environment) is currently under development to complete the proof of concept. Thread management, device management, paging and even interrupt dispatching are all delegated to 'application level' components. Systems which divide the OS into a primitive supervisor part on top of which conventional OS services (e.g. threads) are provided, are called *library operating systems* [8]. Note though that the ORB is not a renamed nano-kernel. It supports life-cycle management and control transfer between components only. This does not mean that the ORB provides thin veneers for system services as with other systems [8]: since there is only one processor mode, application level components

can deal entirely with what are traditionally system services (e.g. interrupts).

Each component implementation type in Go! has its own code segment and the ORB maintains a method table (similar to a C++ v-table). Each component instance has its own data segment and shares its code segment and method table with others of that implementation. By preventing code segments from loading other data segments' selectors, each component can access only its own data, enforcing encapsulation on a per component level with minimal overheads.

The ORB provides 6 methods (analogous to system calls in traditional operating systems):

- install** Install a new component type.
- uninstall** Uninstall an existing component type.
- create** Create a new component instance.
- destroy** Destroy an existing component instance.
- call** Call a given method on a given component.
- return** Return from the most recent **call**.

Certain system components need to contain privileged instructions (e.g., the interrupt dispatcher must be able to load the interrupt descriptor table register). The ORB itself is not responsible for scanning code segments for privileged instructions, but delegates this to a component. It is also the responsibility of this component to ensure that certain components can contain the necessary privileged instructions. e.g., device driver components are likely to require I/O instructions, and the interrupt dispatcher can contain any instructions.

Go! uses a passive component model [10]. This means that the single thread of control³ transfers between components as method calls are issued.

A component can call another by placing the target component ID (its data segment selector) and method number into registers, and calling the ORB's **call** method. This transfers control to the relevant entry-point of the target component (looked up via the target component's method table). The current data segment is also replaced with that of the callee, and the stack segment is 'shrunk' so that the caller's stack frame is no longer accessible (but the arguments are). The ORB also passes the ID of the caller to

³Despite not providing multiple threads, the Go! ORB is re-entrant and supports multiple concurrent stacks. This means library OSs can implement their own threading-model with relative ease (GTE provides fully preemptive multithreading in just 1.2K of unoptimised C++).

the callee so that the caller can be securely authenticated (authorisation is left to the callee or library OS to implement).

`call` is the most performance critical ORB method. As an example, the algorithm for `call` is shown below:

1. push out-going data segment selector onto stack
2. load ORB data segment selector into data segment register
3. validate target component ID & method number
4. shrink stack by manipulating segment descriptor tables (since the stack grows towards zero, set `descriptor_table[ stack_segment ].limit` to the value of the current stack pointer)
5. increment current stack segment's 'call-depth'
6. look up code segment and offset in method table
7. load callee data segment
8. place caller's ID in general purpose register
9. jump into callee code segment at offset indicated by method table

If the call requires parameters they must be pushed onto the stack *after* the return address (parameters are conventionally pushed before the return address — i.e. instructions are issued `push; push; call`). This is because the shrinking of the stack segment must preclude access to the return address so that it is incorruptible, but parameters must be accessible to the callee.

Implementing shared memory in a component-based system involves a component granting access to its state to another. Despite breaking encapsulation, certain situations require this (e.g., a disk device driver committing a component's state to disk, or to achieve some optimisation). In Go! this is facilitated by a callee granting access to its state to a caller (through some `grant_access` method). To achieve this, the callee simply invokes a specialisation of the ORB's `return` method that copies the callee's data segment into the 'extra' segment register.

7 Results & comparisons with other systems

This section reports on results pertaining to Go!'s performance and compares them to that of other systems.

Inter-component communication is considered a good measure of performance because a) it can be

easily compared with other operating systems, and b) inter-component call times are critical to the success of finely-grained component-based systems. Inter-component timings are divided in two categories: null RPC and domain transfer. The former measures the time taken to return after calling a method of another component that takes no parameters, does no work, and produces no result. The latter measures the time simply to transfer control from one component to another without returning or recording information to do so. Go!'s measurements were made using the Pentium's RDTSC instruction which counts the number of cycles that have elapsed since the machine was reset. The test machine was a Pentium 90 with 32 MB of RAM. Results for comparison with other systems are extracted from published benchmarks [4], papers [14, 7, 9, 11] and experimentation. All results are in machine cycles.

<i>OS</i>	<i>hardware</i>	<i>Null RPC</i>	<i>Domain Transfer</i>
BSD	Pentium	55,000	13,000
Mach 2.5	MIPS	3,000	1,600
Spring	SPARC	-	880
L4	Pentium	665	121
Pebble	MIPS	-	114
Go!	Pentium	85	39

Note that some of the figures in this table were obtained on different hardware. However, despite the different architectures, it is clear that Go! significantly out-performs other operating systems. Also, the three most 'useful' results were all recorded on Pentium based machines. BSD gives a handle onto the current 'industry standard'. L4 [15] is a lean research operating system, and represents the 'best of the rest'. Note that although the table implies that Pebble outperforms L4, L4 on the MIPS outperforms Pebble (a one way IPC for L4 takes 86 cycles on a on a MIPS R4600, Pebble takes 114 cycles on a MIPS R5000). This suggests that should figures for Pebble on the Pentium be available they would show inferior IPC times than L4.

As mentioned above, Go! itself does not handle interrupts; a novel approach in operating system design. However, separating interrupt handling out to a server component implies poor interrupt latency. Component-based OSs which incorporate interrupt handling into their nucleus report an interrupt latency of 2000-3000 cycles [11]. It is anticipated that GTE will offer interrupt latency of up to an order of magnitude *improvement* over this. This is because to ensure a minimal nucleus other systems typically have interrupts signal a semaphore on which a handler thread

blocks. In GTE, the interrupt dispatcher directly suspends the current thread (50-100 cycles), and schedules a registered handler thread using a continuation [7] (taking another 50-100 cycles). Interrupt latency is reduced partly by the low overheads of a context switch in Go!, and not requiring a processor mode switch on an interrupt (due to the single processor mode). However, the main speed advantage comes from having the interrupt dispatcher at the same level of abstraction as threads and schedulers.

8 Conclusion

Using segmentation to restrict memory references and code-scanning to prevent the execution of privileged instructions by untrusted components provides protection without the need for separate processor modes. This leads to extremely efficient and finely-grained componentised systems and also simplifies their architecture. A further advantage is that the operating system can become truly componentised — e.g., interrupt dispatching and inter-component protection can be cleanly separated.

Unfortunately, modern microprocessors tend not to support segmentation (despite both Intel's and HP's current architectures (IA32 and PA-RISC) supporting segmentation, even their new joint venture chip (IA64) does not support segmentation). We believe this lack of segmentation to be a mistake as component software technology becomes more widespread.

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