Cost-effective fabrication of nanoscale electrode memristors with reproducible electrical response

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Abstract: This paper aims to promote basic research into memristors, which will help provide theorists with much-needed reliable benchmarks and will also aid the technology progress. It addresses an information gap presently in the literature on simple microfabrication techniques for the realisation of such devices. Consequently, a fabrication method is reported for implementing the full active-material stack, requiring a single lithography and evaporation step. A cost-effective technique that can reliably shrink device lateral dimensions towards the nanoscale is also demonstrated. Experimental results confirm the suitability of the proposed methods for fabricating memristors of varying dimensions that exhibit consistent electrical characteristics.

1 Introduction

The physical realisation by HP [1, 2] of Chua's proposed “missing circuit element” [3] has sparked huge interest in memristors and memristive devices in general, which are potentially useful for extending Moore's law [4] as well as for providing non-volatile memory solutions [5]. Much of this excitement has originated from the potential of constructing circuits that mimic aspects of brain function, like, for example, the learning process [6].

Memristive behaviour is critically dependent on the quality of the interfaces present as well as on the device geometrical characteristics. Many potential uses of memristors involve large device arrays with nanoscale electrode dimensions, to increase density and/or performance. To aid basic research on these devices, it is therefore essential to devise and investigate fabrication techniques that are applicable to the common research environment and can yield memristors with reproducible electrical response and continuous lateral dimension control down to the nanoscale.

Nanoimprint lithography (NIL) has been successfully employed for the fabrication of dense crossbar arrays with nanoscale electrode dimensions [7] and has been consequently applied to fabricate memristor arrays [8]. However, this technique is expensive and can be only justified when nanoscale lateral dimensions and high device density are simultaneously required.

Interface quality is of utmost importance for obtaining reproducible memristor response and is therefore desirable to be able to fabricate the nanoscale-thick, active stack (the two electrodes and the switching layer/s) in one step, without exposing the various layers to ambient, if possible. This requirement has been identified and satisfied in [8]. However, it involves employment of NIL and accurate rotation-angle control of the evaporator workholder bearing the samples, capabilities that

may not be readily available in many labs.

Therefore, for fabricating the memristor electrodes and active stack, it is desirable to use standard contact optical lithography followed by evaporation and lift-off, as these are cost-effective processes widely available in microfabrication labs. However, lift-off is normally incompatible with sputter evaporation, a common deposition method for the memristor switching layers, given the conformality of step coverage. Furthermore, it is also desirable to be able to controllably shrink electrode width towards the 100 nm range or below using these techniques. In the following paragraphs the authors describe cost-effective methods developed for implementing high-quality memristor active stacks as well as for shrinking device lateral dimensions towards the nanoscale, supported by experimental results.

2 Fabrication methods

For the fabrication of memristors, the authors use a deposition chamber that includes both electron-gun and RF-sputtering evaporation sources and employ contact optical lithography and lift-off for depositing the platinum electrodes and the titanium oxide switching layers. More specifically, the top and bottom electrodes consist of electron-gun evaporated Ti/Pt bilayers with respective thicknesses of 5 and 15 nm. The switching layers consist of two successive 30nm-thick titanium-oxide layers, sputtered off a stoichiometric TiO₂ target at a pressure of 1.8×10^{-2} mbar and a RF (13.56 MHz) power density of 8 W/cm², with the topmost one deposited in the presence of 12 sccm flow of oxygen gas, as an excess of oxygen in TiO₂ is known to act as p-type dopants [9].

Two distinct fabrication approaches were tested using the above conditions. The first one involves deposition of the bottom memristor electrode together with the switching layers in a single lithography and lift-off step. The top intersecting electrode is then fabricated following a second lithography, evaporation and lift-off process. Both these lithographic steps are performed by using an enhanced photoresist profile consisting of a double layer of sub-micron resolution positive photoresist (AZ 5214 E, Clariant), as shown in Figure 1a. In more detail, the first layer is flood-exposed prior to the spinning of the second layer, followed by exposure of the desired pattern through a photomask and subsequent development of both layers. As a result of this process, an undercut forms in the first layer, the extent of which can be reproducibly controlled by varying the development time. Figure 1b shows an optical microscope image of such a developed double-layer photoresist structure with 1 μm nominal electrode width. It can be seen that, while the top layer has retained a dimension close to the nominal value, an undercut of over 6 μm has formed within the bottom resist layer. This process makes it possible to lift-off sputter-evaporated layers, something not usually achievable with standard photoresist profiles, given the conformal step coverage of sputter deposition. Importantly, the resulting undercut profile can also be used to shrink electrode

width towards nanoscale dimensions, if required, by employing angle evaporation [10], as shown in Fig. 1a. In this case, the undercut in the photoresist profile, apart from facilitating lift-off, it also serves to accommodate the offsets required to shrink electrode lateral dimensions. By using angle evaporation, in combination with the enhanced photoresist profile, the authors demonstrated that it is possible to shrink electrode lateral dimensions controllably to below 100 nm. Figure 1c shows an array of 80 nm wide platinum electrodes fabricated by this technique. An optical microscope image of a $1 \times 1 \mu\text{m}$ memristor, fabricated using the approach described above, is shown in Figure 2.

The second memristor fabrication approach involves the deposition of the whole active stack (top and bottom electrodes and switching layers) in a single lithography and evaporation step, without exposing the unfinished device to ambient, leading to high-quality interfaces with reproducibly controlled characteristics. In more detail, a Ti/Au contact pad is first made on silicon substrate, onto which the whole stack is deposited via lift-off in a single lithography step. Then, a silicon nitride passivating layer is sputter deposited and a window is etched to uncover the memristor stack as well as the contact pad. Finally, a second contact pad, deposited onto the silicon nitride layer, provides the connection to the top end of the memristor stack. Fig. 3 shows a flowchart detailing the various processing steps of this fabrication method.

3 Results and discussion

The first fabrication approach described in the previous paragraph offers a cost-effective method of realising memristors by using standard photolithography and lift-off. These devices can be used for characterisation purposes as well as for integration up to a moderate density. As the method is compatible with the angle evaporation technique, it is possible to shrink electrode width down to under 100nm without resorting to expensive tools. The device stack has to be exposed to ambient prior to the completion of the fabrication process, which may be a concern with regard to the quality and reproducibility of the interfaces. However, this interruption is designed to occur at the top interface, involving an oxygen-rich titanium oxide layer and the titanium layer of the memristor top electrode.

The second fabrication approach also uses standard lithography and lift-off but offers higher interface quality, as the whole of the device stack is deposited in one step with no exposure to ambient. However, this benefit comes with the usual size limitations of standard photolithography, as angle evaporation is not an option in this case. Yet, the same method can be combined with NIL to yield reliable nanoscale devices.

Memristors, fabricated with both processing approaches described above, were consequently characterised. DC current-voltage measurements were performed on-wafer by contacting the top and bottom device electrodes with a pair of Wentworth probes, connected with a Keithley 4200

Semiconductor Characterisation System. Since the properties of the devices are dependent upon their previous state, the measurement procedure is of great significance. Thus, all devices were initially biased at the maximum negative voltage (-5V), then the applied bias was ramped up to the maximum voltage of 5V in 50mV, 1ms long steps and finally back to -5V again, in the same manner. For device protection purposes, current limiting to +/- 100mA was applied throughout all measurements. Additionally, all measurements were performed at room temperature for consistency. Typical current-voltage characteristics of 1 x 1 μm memristors, fabricated with the first approach, are shown in the graphs of Fig. 4. Transition from a high-resistance state (off state) to a low resistance state (on state) occurs at a bias of around +/- 1 V. Furthermore, there is an evident broadening of the hysteresis loop after each consecutive scan, which is attributed to the even increasing charge displacement. Similar memristive response is also observed on devices fabricated with the second method, as shown in the graphs of Fig. 5. In this case, the device cross-section is 5 x 5 μm and perhaps this is the reason that transition from an off to an on state is not as clear as in the previous devices. However, the broadening of the hysteresis loop after the second scan is more pronounced and the characteristic curves for all scans are smoother, suggesting a better quality device core.

4 Conclusion

The fabrication of memristors is reported, consisting of titanium dioxide switching layers, with two distinct ways that utilise standard photolithography and lift-off processes to yield quality devices that exhibit consistent electrical response. These techniques make it possible to realise the full active stack in one step and to controllably shrink the memristor electrodes towards nanoscale width dimensions in a cost-effective way, available in most microfabrication labs. Devices of various dimensions were fabricated and consequently characterised. DC current-voltage measurements show reproducible electrical response that is consistent with memristive behaviour.

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6 References

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Figure 1. First memristor fabrication approach: (a) Diagram of the double-layer photoresist and the angle evaporation principle: the shadow effect results in an offset and narrower metallisation compared to the nominal dimension defined by the window of the top photoresist layer. (b) Optical microscope image of a developed double layer photoresist structure. The photomask used has a linewidth of 1 micrometer. (c) SEM image of an array of 80 nm wide platinum electrodes fabricated by angle evaporation and lift-off.

Figure 2. Optical microscope image showing detail around the stack area of a 1 x 1 μm memristor, fabricated using first approach described.

Figure 3. Flowchart detailing various processing steps for fabrication of memristors with single photolithography and lift-off step.

Figure 4. Typical current-voltage characteristics of 1 x 1 μm memristors, fabricated with first approach described.

Figure 5. Typical current-voltage characteristics of $5\mu\text{m} \times 5\mu\text{m}$ memristors, fabricated with the second approach described in the text. These devices exhibit more consistent response that could be attributed to their high quality core.