H^∞ Control of the Neutral Point in Four-Wire Three-Phase DC–AC Converters

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Abstract—Inverters used as the interface for a distributed generator in a three-phase four-wire system sometimes operate with a large neutral current because of unbalanced loads and single-phase (possibly nonlinear) loads. Voltage balance within the dc-link of the inverter is important for proper operation of the inverter, and the neutral current is a significant disturbance to this. It is preferable to use fast acting control rather than dissipative balancing or large-valued capacitors. This paper develops a linear model of an actively balanced split dc-link and applies H^∞ control design to provide high-bandwidth robust control. The approach is developed for a conventional two-level inverter, but it remains valid (without change) for a three-level neutral-point clamped inverter. The controller achieves very small deviations of the neutral point (better than 0.5 V in 800 V) from the midpoint of the dc source despite the large neutral current (32 A_{RMS}). The controller design is described and verified first in a PSCAD simulation and second in experimental testing of a 30-kW 415-V (line) inverter.

Index Terms—DC–AC power converter, dc-link balancing, four-wire three-phase power system, H^∞ control, multilevel inverter, neutral line.

I. INTRODUCTION

THE dc-to-three-phase ac converters (inverters) have long been used in motor-control applications and are now becoming common as the interface between a dc power source and ordinary ac consumer loads. This is true for uninterruptible power supplies and for small distributed generation units which are not natural 50- or 60-Hz sources. In some circumstances, the inverter must supply a mixture of single- and three-phase loads via a four-wire three-phase distribution network. The traditional six-switch inverter must be supplemented with a neutral connection. This neutral connection will carry the zero-sequence current of the loads and will be composed of fundamental frequency imbalance current and the common-mode triplen harmonics caused by nonlinear single-phase loads such as simple diode rectifiers.

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There is also a need to provide a balanced neutral point for three-level inverters using the neutral-point clamped topology and, by extension, a need for balancing in higher level inverters based on the multipoint clamped inverter ([1]–[4] and the survey paper [5]). Although not a focus of this paper, the control techniques described could have applications in multilevel inverters.

If the dc power source is able to provide several separately regulated outputs, then balancing the dc-link of the inverter can be given over to the dc source. However, it is more common for the source to be a single dc voltage equal to the total voltage required in the dc-link. It is common then to split the available dc-link across several capacitors in a chain, and the challenge is then to ensure that the voltage is equally shared. The sharing is disturbed by the injection of current at intermediate points in the chain (such as the injection of neutral current into the midpoint) and by the overall variations of the dc-link voltage being imposed across a chain of imperfectly matched capacitors.

If the neutral line current of a four-wire system has significant low-frequency components, then the neutral-point voltage (the midpoint of the capacitor chain) may deviate severely from the true midpoint of the dc source. This deviation of the neutral point may result in an unbalanced or modulated output voltage, the presence of zero-sequence voltage components and, hence, an even larger neutral current. Thus, the generation of a balanced neutral point in a simple and effective manner has become an important problem. Although dc to three-wire three-phase electronic power converters have been widely studied in recent years [6], [7], dc to four-wire three-phase converters have received relatively little attention [8]–[10].

A straightforward way to provide balance of a split dc-link is to use bleed resistors, as shown in Fig. 1(a). The resistors correct long run imbalance in the capacitors and must be chosen to draw enough current to do this without causing excessive dissipation. The shorter term ripple of the neutral voltage can only be addressed by increasing the size of the capacitors, and this may require very large capacitors, if significant imbalance is expected in the ac loads. It is considered that this topology is not suitable for dc–ac converters which supply power to a network containing single-phase loads. A split dc-link of this form is used in four-wire active power filters, where rebalancing of the imbalance is not attempted and the system is free of dc components [11]–[12]. Some special pulsewidth modulation (PWM) schemes have been developed for three-level converters to balance the charging of the split link capacitors [3]–[14], but these apply to multilevel converters which do not make external connection to the neutral point (i.e., three-wire systems). In this

Fig. 1. Conventional topologies for providing a neutral line. (a) Split dc-link neutral connection. (b) A fourth-leg neutral connection used with three-dimensional space-vector modulation.

case, if the load current contains some harmonics, the balance cannot be maintained no matter how large the capacitors are, as discussed in [13].

An established way to provide the neutral point for a four-wire inverter is to add an additional fourth leg, called a neutral leg to the conventional three-leg inverter [8], as shown in Fig. 1(b). The space-vector-modulation (SVM) method has been extended to cover the four-leg inverter [10] by considering three-dimensional space vectors. An advantage of this approach is that there is no requirement for a split (and balanced) dc-link. In common with the three-leg SVM method, the four-leg SVM method provides a 15.5% voltage magnitude advantage over sinusoidal PWM (but as noted in [9], there are ways in achieving this with PWM methods). There is, however, a potential electromagnetic compatibility (EMC) problem because the dc-link is no longer ground referenced and is subjected to high-frequency voltage transitions with respect to the system neutral. In addition, the neutral leg cannot be independently controlled, and the corresponding control design (including the PWM scheme) becomes more complicated, as discussed in [10].

Instead of using a fourth leg to form the neutral point directly, the leg can be used to actively balance a split dc-link, as shown in Fig. 2. There are several advantages to this approach. First, the phase legs and the neutral leg can be controlled independently. Second, the majority of the neutral current flows through the neutral-leg switches rather than the dc-link capacitors, and thus, high-value capacitances are required to attenuate the ripple and volume and to make cost savings. Third, the dc-link and inverter circuit are at a constant potential with respect to the system neutral, and there is a reduced problem of driving high-frequency interference currents through parasitic capacitances in the inverter. The circuit of Fig. 2 was proposed in [15] by using the reasoning of combining a dc-dc buck converter and a dc-dc boost converter, and in [16] by using the reasoning of a class-B chopper. The reasoning proposed here is simpler and provides insight into the problem. In [15], the buck converter is used to increase the neutral-point voltage; the boost converter is used to lower it. In [15] and [16], a comparator with

hysteresis is used to activate one or the other of the two neutral-leg switches. This is a nonlinear controller. The possibility of a large neutral current is not discussed in [15] and [16] because in both cases a multilevel converter without a neutral connection was considered (and it appears that the control strategy of [15] is not suitable when a large neutral current is present).

In this paper, we develop a linear model for the neutral-leg circuit so that the design of a linear controller using advanced control techniques is possible. In this case, the H^∞ control technique is adopted with the aim of balancing the dc link when the neutral current is large (see [17] for the control design with classical techniques). The proposed design is tested in a PSCAD simulation and then verified through experimental testing of a 30-kW 415-V (line) four-leg inverter. This paper complements the results published in [18], where the voltage control problem of the dc-ac converter in a microgrid was discussed assuming the existence of a balanced dc link.

II. MODELING OF THE NEUTRAL LINE CIRCUIT

The circuit in Fig. 2 is consist of a dc to three-phase ac converter in which the inverter is a six-switch two-level example, and the neutral circuit contains further two switches, a pair of nominally similar capacitors and an inductor. The task for the controller is to generate firing pulses for the switches S_{N+} and S_{N-} . The general aim of the controller is to maintain the voltage at the midpoint of capacitors very close to the true midpoint of the dc link, measured as V_{ave} . If the dc-link voltage is constant, then the controller can maintain the link in balance by forcing the inductor current i_L equal to the neutral current i_N so that no current flows through the capacitors. However, the controller must also cope with perturbations in dc source voltage, as we shall see.

All voltages are measured with respect to the neutral point N . The total dc-link voltage is the difference between the two capacitor voltages measured with respect to the neutral point

$$V_{dc} = V_+ - V_- \quad (1)$$

We desire a balance between the two capacitor voltages, and this can be expressed by making V_{ave} very small, where the average voltage V_{ave} is defined as

$$V_{ave} = \frac{V_+ + V_-}{2} \quad (2)$$

Using Kirchhoff's laws, we obtain the following equations:

$$u_N = L_N \frac{di_L}{dt} + R_N i_L \quad i_N = i_L + i_c \quad (3)$$

where R_N is the equivalent series resistance of the inductor and

$$i_c = C_{N+} \frac{dV_+}{dt} + C_{N-} \frac{dV_-}{dt} \quad (4)$$

Equations (1) and (2) define a coordinate transformation

$$\begin{bmatrix} V_+ \\ V_- \end{bmatrix} = \begin{bmatrix} 0.5 & 1 \\ -0.5 & 1 \end{bmatrix} \begin{bmatrix} V_{dc} \\ V_{ave} \end{bmatrix}.$$

Fig. 2. Neutral line provision with active balancing. The inverter shown could be replaced by a three-level inverter or by other circuits without affecting the analysis and design developed in this paper.

Fig. 3. Neutral-leg switch state q (top line) and instantaneous neutral-leg voltage u_N (bottom line).

Hence, (4) can be reformulated as

$$i_c = (C_{N+} + C_{N-}) \frac{dV_{ave}}{dt} + \frac{C_{N+} - C_{N-}}{2} \cdot \frac{dV_{dc}}{dt}.$$

This equation reveals that the overall dc-link voltage is subject to change (perhaps because of the variation in the dc power source); then, the balance of the capacitor voltages is disturbed if the capacitor values are not equal. Because large-valued electrolytic capacitors are subject to large manufacturing tolerances, this can be a significant effect. A new voltage variable is defined to represent this disturbance

$$V_0 = -\frac{C_{N+} - C_{N-}}{C_{N+} + C_{N-}} \cdot \frac{V_{dc}}{2}. \quad (5)$$

The equation for i_c now becomes

$$i_c = (C_{N+} + C_{N-}) \frac{d(V_{ave} - V_0)}{dt}. \quad (6)$$

The variable q is used to represent the state of the neutral-leg switches:

$$q = \begin{cases} +1, & \text{if } S_{N+} \text{ is ON and } S_{N-} \text{ is OFF} \\ -1, & \text{if } S_{N-} \text{ is ON and } S_{N+} \text{ is OFF.} \end{cases}$$

The voltage u_N follows the same shape as q , as shown in Fig. 3, in which h is the switching period and $h = 1/f_s$. As it

Fig. 4. Block diagram of the uncontrolled neutral-leg system.

is common in switch-mode circuits, the switching action is at a high enough frequency f_s to have little impact on the dynamics of the circuit, and so, we consider the average values of the signals over the period h . The average of q is p , so that $p \in [-1, 1]$; the duty-cycle of S_{N+} is

$$d = \frac{1+p}{2}$$

and the average of u_N is

$$u_N = dV_+ + (1-d)V_- = \frac{p}{2}V_{dc} + V_{ave}. \quad (7)$$

Equations (3), (6), and (7) define the blocks of the control model of the neutral-leg balancing circuit, as shown in Fig. 4. V_0 is considered as an external disturbance, and p is the control variable. Strictly speaking, even this simplified model is non-linear because p is multiplied with the variable V_{dc} . However, since the variations of V_{dc} are relatively small, we will, in the design that follows, consider that the term V_{dc} appearing in the first block in Fig. 4 is equal to its nominal value of V_{dc}^{nom} . If the variations of V_{dc} are expected to be large, then they can be compensated by measuring V_{dc} and multiplying the output p of the controller with the correction factor V_{dc}^{nom}/V_{dc} (however, simulations show that the effect of this correction is not significant).

III. CONTROLLER DESIGN

The control objective for the plant in Fig. 4 is to maintain a stable and balanced neutral point, i.e., to make V_{ave} as small as possible while maintaining the stability of the system. The disturbances are the neutral current i_N and the equivalent external disturbance V_0 defined in (5). Since the current i_c contains significant ripple at the switching frequency, it must be sensed

Fig. 5. H^∞ control problem is to minimize the norm of the transfer function from w to z . The weighting functions W_v and W_u need not be implemented physically; they are only mathematical tools.

through a low-pass filter F , as shown in Fig. 5. The remaining ripple after this filter will be interpreted as a measurement noise n (see again Fig. 5). We denote the Laplace transformation by a hat. Then, V_i , the signal available to the controller from the measurement of i_c , is given by $\hat{V}_i = F\hat{i}_c + \hat{n}$. From the H^∞ control point of view, the simplest formulation of the problem would be to minimize the H^∞ norm of the transfer function from $[i_N \ V_0 \ n]^T$ to the average voltage V_{ave} . Such a formulation would be unrealistic since it would ignore the fact that the disturbances are expected in a certain frequency range and it would not reflect that we must avoid the signal u_N getting too large (because for obvious physical reasons, $V_- < u_N < V_+$). Thus, as it is usual in applications of the H^∞ theory, we introduce the weighting functions W_v to multiply V_{ave} and W_u to multiply u_N . We also introduce two new variables I_0 and I_n , which are proportional to V_0 and n via the factors ρ and ζ . These weighting factors are needed to adjust the relative importance of the three disturbances i_N , V_0 , and n in the H^∞ -norm minimization process (because i_N , I_0 , and I_n will have equal importance). The H^∞ control problem is then formulated to minimize the H^∞ norm of the transfer function from $w = [i_N \ I_0 \ I_n]^T$ to $z = [V_v \ V_u]^T$, denoted $\mathbf{T}_{zw} = \mathcal{F}_l(\mathbf{P}, \mathbf{K})$. The closed-loop system can be represented in terms of Laplace transforms, ignoring initial conditions, as

$$\begin{bmatrix} \hat{z} \\ \hat{y} \end{bmatrix} = \mathbf{P} \begin{bmatrix} \hat{w} \\ \hat{u} \end{bmatrix}, \quad \hat{u} = \mathbf{K} \hat{y}$$

where $\mathbf{P}$ is the generalized plant and $\mathbf{K}$ is the controller to be designed. A nearly optimal $\mathbf{K}$ can be obtained by the H^∞ control algorithm (which solves two Riccati equations at each iteration) (see [19] and [20] for details). In the sequel, we derive the realization of $\mathbf{P}$ (which is needed to obtain $\mathbf{K}$) and the realization of the closed-loop transfer function from $w' = [i_N \ V_0 \ n]^T$ to $z' = [V_{ave} \ u_N]^T$.

A. Realization of $\mathbf{P}$

If the state variables of the original plant are chosen to be the inductor current i_L and the voltage $V_c = V_{ave} - V_0$, i.e.,

$x = \begin{bmatrix} i_L \\ V_c \end{bmatrix}$, and if the control input u is p , then the following state equations can be obtained from Fig. 5:

$$\dot{x} = Ax + B_1 w + B_2 u \quad (8)$$

where

$$A = \begin{bmatrix} -\frac{R_N}{L_N} & \frac{1}{L_N} \\ -\frac{1}{C_{N+} + C_{N-}} & 0 \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 & \frac{\rho}{L_N} & 0 \\ \frac{1}{C_{N+} + C_{N-}} & 0 & 0 \end{bmatrix}$$

$$B_2 = \begin{bmatrix} \frac{V_{dc}}{2L_N} \\ 0 \end{bmatrix}.$$

The output equations are

$$V_{ave} = C_a x + D_{1a} w + D_{2a} u$$

$$u_N = C_{1b} x + D_{11b} w + D_{12b} u$$

$$i_c = C_{2b} x + D_{21b} w + D_{22b} u \quad (9)$$

where

$$C_a = \begin{bmatrix} 0 & 1 \end{bmatrix} \quad D_{1a} = \begin{bmatrix} 0 & \rho & 0 \end{bmatrix} \quad D_{2a} = \begin{bmatrix} 0 \end{bmatrix}$$

$$C_{1b} = \begin{bmatrix} 0 & 1 \end{bmatrix} \quad D_{11b} = \begin{bmatrix} 0 & \rho & 0 \end{bmatrix} \quad D_{12b} = \begin{bmatrix} \frac{V_{dc}}{2} \end{bmatrix}$$

$$C_{2b} = \begin{bmatrix} -1 & 0 \end{bmatrix} \quad D_{21b} = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix} \quad D_{22b} = \begin{bmatrix} 0 \end{bmatrix}.$$

Assume that the realization of the weighting function W_v is

$$W_v = \begin{bmatrix} A_v & B_v \\ C_v & D_v \end{bmatrix}$$

(this notation means that $W_v(s) = D_v + C_v(sI - A_v)^{-1}B_v$, see, for example, [19]). Then

$$\begin{aligned}\hat{V}_v &= \left[\begin{array}{c|c} A_v & B_v \\ \hline C_v & D_v \end{array} \right] \hat{V}_{\text{ave}} \\ &= \left[\begin{array}{c|c} A_v & B_v \\ \hline C_v & D_v \end{array} \right] \left[\begin{array}{c|c|c} A & B_1 & B_2 \\ \hline C_a & D_{1a} & D_{2a} \end{array} \right] \begin{bmatrix} \hat{w} \\ \hat{u} \end{bmatrix} \\ &= \left[\begin{array}{cc|cc} A & 0 & B_1 & B_2 \\ B_v C_a & A_v & B_v D_{1a} & B_v D_{2a} \\ \hline D_v C_a & C_v & D_v D_{1a} & D_v D_{2a} \end{array} \right] \begin{bmatrix} \hat{w} \\ \hat{u} \end{bmatrix} \quad (10)\end{aligned}$$

(recall that a hat is used to denote the Laplace transformation). Similarly, assume that the realization of the weighting function W_u is

$$W_u = \left[\begin{array}{c|c} A_u & B_u \\ \hline C_u & D_u \end{array} \right]$$

then

$$\begin{aligned}\hat{V}_u &= \left[\begin{array}{c|c} A_u & B_u \\ \hline C_u & D_u \end{array} \right] \hat{u}_N \\ &= \left[\begin{array}{cc|cc} A & 0 & B_1 & B_2 \\ B_u C_{1b} & A_u & B_u D_{11b} & B_u D_{12b} \\ \hline D_u C_{1b} & C_u & D_u D_{11b} & D_u D_{12b} \end{array} \right] \begin{bmatrix} \hat{w} \\ \hat{u} \end{bmatrix}. \quad (11)\end{aligned}$$

Assume that the implementation of the low-pass filter F is

$$F = \left[\begin{array}{c|c} A_F & B_F \\ \hline C_F & D_F \end{array} \right]$$

then

$$\begin{aligned}\hat{V}_i &= \left[\begin{array}{c|c} A_F & B_F \\ \hline C_F & D_F \end{array} \right] \hat{i}_c + \zeta \hat{I}_n \\ &= \left[\begin{array}{c|c} A_F & B_F \\ \hline C_F & D_F \end{array} \right] \left[\begin{array}{c|c|c} A & B_1 & B_2 \\ \hline C_{2b} & D_{21b} & D_{22b} \end{array} \right] \begin{bmatrix} \hat{w} \\ \hat{u} \end{bmatrix} + \zeta \hat{I}_n\end{aligned}$$

$$\begin{aligned}&= \left[\begin{array}{cc|cc} A & 0 & B_1 & B_2 \\ B_F C_{2b} & A_F & B_F D_{21b} & B_F D_{22b} \\ \hline D_F C_{2b} & C_F & D_F D_{21b} + \begin{bmatrix} 0 & 0 & \zeta \end{bmatrix} & D_F D_{22b} \end{array} \right] \\ &\times \begin{bmatrix} \hat{w} \\ \hat{u} \end{bmatrix}. \quad (12)\end{aligned}$$

Combining (8)–(12), we obtain the realization of the generalized plant $\mathbf{P}$, with inputs w and u and outputs z and y , as shown in the expression at the bottom of the page.

B. Realization of the Closed-Loop Transfer Function

Denote $y = \begin{bmatrix} V_{\text{ave}} \\ V_i \end{bmatrix}$ and denote by $\tilde{\mathbf{P}}$ the transfer function from $\begin{bmatrix} w \\ u \end{bmatrix}$ to $\begin{bmatrix} z' \\ y \end{bmatrix}$. Then

$$\begin{aligned}\tilde{\mathbf{P}} &= \left[\begin{array}{cc|cc|cc} A & 0 & B_1 & B_2 & & \\ B_F C_{2b} & A_F & B_F D_{21b} & B_F D_{22b} & & \\ \hline C_a & 0 & D_{1a} & D_{2a} & & \\ C_{1b} & 0 & D_{11b} & D_{12b} & & \\ \hline C_a & 0 & D_{1a} & D_{2a} & & \\ D_F C_{2b} & C_F & D_F D_{21b} + \begin{bmatrix} 0 & 0 & \zeta \end{bmatrix} & D_F D_{22b} & & \end{array} \right] \\ &\doteq \left[\begin{array}{c|c|c} \tilde{A} & \tilde{B}_1 & \tilde{B}_2 \\ \hline \tilde{C}_1 & \tilde{D}_{11} & \tilde{D}_{12} \\ \hline \tilde{C}_2 & \tilde{D}_{21} & \tilde{D}_{22} \end{array} \right].\end{aligned}$$

Assume that the controller to be designed is realized as

$$\mathbf{K} = \left[\begin{array}{c|c} A_K & B_K \\ \hline C_K & D_K \end{array} \right]$$

where, usually, $D_K = 0$, if $\mathbf{K}$ is obtained from the H^∞ algorithm. However, D_K may be nonzero after controller reduction. According to the star-product formula [19], the transfer function from w to z' is shown in the first expression at the bottom of the next page, where

$$\tilde{R} = (I - D_K \tilde{D}_{22})^{-1} \quad R = (I - \tilde{D}_{22} D_K)^{-1}.$$

$$\mathbf{P} = \left[\begin{array}{cccc|cccc} A & 0 & 0 & 0 & B_1 & & B_2 & \\ B_v C_a & A_v & 0 & 0 & B_v D_{1a} & & B_v D_{2a} & \\ B_u C_{1b} & 0 & A_u & 0 & B_u D_{11b} & & B_u D_{12b} & \\ B_F C_{2b} & 0 & 0 & A_F & B_F D_{21b} & & B_F D_{22b} & \\ \hline D_v C_a & C_v & 0 & 0 & D_v D_{1a} & & D_v D_{2a} & \\ D_u C_{1b} & 0 & C_u & 0 & D_u D_{11b} & & D_u D_{12b} & \\ \hline C_a & 0 & 0 & 0 & D_{1a} & & D_{2a} & \\ D_F C_{2b} & 0 & 0 & C_F & D_F D_{21b} + \begin{bmatrix} 0 & 0 & \zeta \end{bmatrix} & & D_F D_{22b} & \end{array} \right]$$

Hence, the closed-loop transfer function from $w' = \begin{bmatrix} i_N \\ V_0 \\ n \end{bmatrix}$ to z' (this is the relevant closed-loop transfer function in terms of the original variables) is

$$\mathbf{T}_{z'w'} = \mathbf{T}_{z'w} \begin{bmatrix} 1 & 0 & 0 \\ 0 & \frac{1}{\rho} & 0 \\ 0 & 0 & \frac{1}{\zeta} \end{bmatrix}.$$

IV. DESIGN EXAMPLE

The example here is of an inverter to be used to export power from micro gas turbine via a high-frequency rectifier and dc link. The converter is the one which will be used in the experimental verification rated at 30 kW and is designed to work in a four-wire system with a nominal phase voltage of 240 V_{RMS}. Further discussion of this application can be found in [18], [21], and [22]. The parameters of the neutral-leg circuit are: $L_N = 2.5$ mH, $R_N = 0.2$ Ω , $C_{N+} = C_{N-} = 6600$ μ F, and $V_{dc} = 800$ V. The switching frequency is $f_s = 10$ kHz and $F(s) = 1000/(s + 1000)$.

A. Selection of the Weighting Functions

It is not easy to choose suitable weighting functions for a specific H^∞ control problem. These functions have to reflect the relative weight of different signals, their frequency characteristics, and at the same time they must be chosen such that the problem is solvable. It is difficult to find guidelines on this problem in the literature (some general guidelines are provided in [19] and [20]). The selection of the weighting functions for our H^∞ control problem is detailed below.

The weighting function W_v has to be large for the range of significant disturbance frequencies (50 Hz and a few multiples of it), and it has to decay for larger frequencies, since the switching frequency limits the realizable control bandwidth. (In any case, the capacitors are effective at attenuating high-

frequency ripple voltage). The weighting function $W_v(s)$ can be chosen as

$$W_u(s) = g \frac{s + \omega_h}{s + \omega_l} = \left[\begin{array}{c|c} -\omega_l & g \\ \hline \omega_h - \omega_l & g \end{array} \right]$$

where g is a tuning parameter to move the Bode plot of W_v up or down.

The signal u_N is closely related (almost proportional) to $u = p$. We want to prevent u from becoming large, especially at high frequencies. Therefore, the weighting function W_u is chosen small for low frequencies and large for high frequencies. The usual algorithm employed in H^∞ control requires that the matrix $\begin{bmatrix} D_v D_{2a} \\ D_u D_{12b} \end{bmatrix}$ has full column rank. Since $D_{2a} = 0$, D_u cannot be zero. Hence, W_u has to be nonstrictly proper. The weighting function W_u can be chosen as

$$W_u(s) = k \frac{s + \omega_l}{s + \omega_h} = \left[\begin{array}{c|c} -\omega_h & k \\ \hline \omega_l - \omega_h & k \end{array} \right]$$

where k is a tuning parameter to move the Bode plot of W_u up or down. In this application, the fundamental frequency is 50 Hz, and the high-frequency components under consideration are up to the 31st harmonic. Therefore, ω_h is chosen to be 10 000 rad/s. The Bode plots of the weighting functions $W_u(s)$ and $W_v(s)$ are shown in Fig. 6 for $k = 0.1$ and $g = 10$.

B. H^∞ Controller Design

The tuning parameters are chosen to be: $k = 0.1$, $g = 10$, $\rho = 0.01$, and $\zeta = 0.01$. The weighting parameters are chosen to be $\omega_l = 1$ rad/s and $\omega_h = 10 000$ rad/s. Using the μ -analysis toolbox from MATLAB, the H^∞ controller $\mathbf{K} = [\mathbf{K}_v \quad \mathbf{K}_i]$ is obtained, as shown by the second expression at the bottom of the page. This controller is somewhat unrealistic because the sampling frequency is usually limited (in the experimental case it is the same as the switching frequency 10 kHz). In order to make the controller implementable, any zeros or poles which correspond to a corner frequency much larger than $\omega_h = 10^4$ rad/s are substituted by a proportional gain (i.e., ignoring s). Then, the controller derived earlier is reduced to $\mathbf{K}_r(s)$, shown at the bottom of the next page.

$$\mathbf{T}_{z'w} = \mathcal{F}_l(\tilde{\mathbf{P}}, \mathbf{K}) = \left[\begin{array}{cc|c} \tilde{A} + \tilde{B}_2 \tilde{R} D_K \tilde{C}_2 & \tilde{B}_2 \tilde{R} C_K & \tilde{B}_1 + \tilde{B}_2 \tilde{R} D_K \tilde{D}_{21} \\ B_K R \tilde{C}_2 & A_K + B_K R \tilde{D}_{22} C_K & B_K R \tilde{D}_{21} \\ \hline \tilde{C}_1 + \tilde{D}_{12} D_K R \tilde{C}_2 & \tilde{D}_{12} \tilde{R} C_K & \tilde{D}_{11} + \tilde{D}_{12} D_K R \tilde{D}_{21} \end{array} \right]$$

$$\mathbf{K}_v(s) = \frac{-0.0025(s - 9.134 \times 10^{10})(s + 8.041 \times 10^4)(s + 1.002 \times 10^4)(s + 80.12)(s + 73.21)}{(s + 3.126 \times 10^8)(s + 1.032 \times 10^5)(s + 6061)(s + 76.03)(s + 1)}$$

$$\mathbf{K}_i(s) = \frac{5.9668 \times 10^8(s + 10^4)(s + 1000)(s + 80)}{(s + 3.126 \times 10^8)(s + 1.032 \times 10^5)(s + 6061)(s + 76.03)}.$$

Fig. 6. Bode plots of the chosen weighting functions.

Fig. 7. Bode plots of the controllers $\mathbf{K}$ and $\mathbf{K}_r$.

The Bode plots of these controllers are shown in Fig. 7. The Bode plots of the corresponding closed-loop transfer functions using the original H^∞ controller $\mathbf{K}$ and the reduced controller $\mathbf{K}_r$ are shown in Fig. 8. The curves are very close: Only the transfer functions from i_N to u_N differ a little at very high frequencies that are much higher than the switching (sampling) frequency.

V. SIMULATION AND EXPERIMENTAL RESULTS

The system described so far was time-step simulated using PSCAD/EMTDC with a component-level model of the inverter. A Tustin discretized form of the reduced controller $\mathbf{K}_r$ has been used in our simulations. In the simulation (as in the experiment), the three-phase inverter operates in stand-alone mode (not connected to a stiff utility grid) and supplies a single-phase load, so that a large neutral current exists. Two example

Fig. 8. Bode plots of the closed-loop transfer function from i_N to V_{ave} and to u_N .

loads have been used in our simulations: Load-A is a linear resistive-inductive impedance ($R = 87 \, \Omega$ in series with $L = 8 \, \text{mH}$), which draws a relatively small load current; load-B is a lower impedance ($R = 7 \, \Omega$ in series with $L = 8 \, \text{mH}$) and draws approximately $7.5 \, \text{kV} \cdot \text{A}$ ($32A_{\text{RMS}}$) at 50 Hz. The connection is switched from load-A to load-B at 0.2 s. Some of the signals have been filtered by a hold filter H , in order to plot them more clearly, without the ripple at multiples of 10 kHz. Here

$$H(s) = \frac{1 - e^{-sh}}{sh} \quad h = 10^{-4} \, \text{s}. \quad (13)$$

This is a notch filter whose notching frequencies are the switching frequency $f_s = 10 \, \text{kHz}$ and its nonzero integer multiples.

A set of simulation waveforms are shown in Fig. 9. With load-A in place ($t < 0.2 \, \text{s}$), the peak value of V_{ave} is 0.075 V [Fig. 9(a)]. When the connection is switched to load-B, V_{ave} reaches 0.28 V in the transient and then settles to within 0.16 V. The inductor current [Fig. 9(c)] closely follows the neutral current [Fig. 9(b)], and the dc-link capacitor current i_c (after hold filtering) [Fig. 9(d)] is very small and not greatly disturbed by the load switch. The simulations show that the neutral point is balanced with respect to the dc terminals and contains only a very small ripple despite the large neutral current. During the load change, the controller demonstrates a very good dynamic performance.

In the experimental system, the controller is implemented on a dual DSP system using a TMS320C6713 and a TMS320LF2407A. The TMS320LF2407A is a fixed-point processor with many integrated peripherals. It is used to process the analog signal inputs from sensors, generate the PWM output, and perform protection and monitoring functions. The TMS320C6713 is a floating-point processor used to process all the control algorithms, including the PLL, the overall power

$$\mathbf{K}_r(s) = \begin{bmatrix} 0.5692 \frac{(s + 1.002 \times 10^4)(s + 80.12)(s + 73.21)}{(s + 6061)(s + 76.03)(s + 1)} & 1.9088 \frac{(s + 10^4)(s + 1000)(s + 80)}{(s + 1.032 \times 10^5)(s + 6061)(s + 76.03)} \end{bmatrix}$$

Fig. 9. Neutral circuit waveforms from simulation of a step change in impedance of a single-phase load. The signal i_c has been filtered to remove switching frequency ripple, as described in the text.

control, the H^∞ repetitive control of the phase voltages (which is described in [18]), and the dc neutral-point controller that is the subject of this test. Interprocessor communication uses the serial peripheral interface (SPI). The filter $F(s)$ of Fig. 5 has been realized using op-amps on the conditioning board to avoid aliasing problems. Quantization error and noise in the A/D converter measuring V_{ave} caused considerable difficulty. These problems have been overcome by reducing the active range of the conditioning amplifier to $|V_{ave}| < 1$ V (i.e., above 1 V, the amplifier saturates).

Experimental tests were conducted to replicate the tests performed in the simulations. The results are shown in Fig. 10. The peak values of V_{ave} under the two load conditions are about 0.1 and 0.25 V, respectively. These values are somewhat larger than those in the simulations, and this is attributed to external interference and parameter mismatch in the experimental system. The peak of the transient response is about 0.38 V. The plots show that almost all the neutral current flows in the neutral-leg switches rather than in the dc-link capacitors. The dc-link capacitor current consists mainly of switching frequency ripple. These experimental results have verified the good tracking and dynamic performance of the controller.

VI. CONCLUSION

The provision of a balanced and low-ripple split dc-link has been examined for the provision of a neutral line in four-wire three-phase inverters. A linear model has been developed for an active balancing circuit consisting of a conventional neutral leg and a split dc-link. The intention was to avoid the need for large capacitors or dissipative passive balancing by implementing high-bandwidth robust control. The control of the neutral leg has been formulated as an H^∞ control problem. In order to make the H^∞ control problem solvable, an artificial signal (measurement noise) n is introduced. Due to its high bandwidth, the nearly optimal controller has to be reduced

Fig. 10. Experimental results for the same step-change of load as in the simulations shown in Fig. 9. The origin of the time axis has been chosen as 0.17 s, so that the step-change occurs at 0.2 s to match the simulation conditions.

so that it can be implemented. The choice of weighting functions for the H^∞ design process is discussed in terms of the required controller properties. The achievable performance is illustrated in Bode plots of the closed-loop transfer function. The performance of the system was verified through time-step simulation in PSCAD and experimental testing on a full power prototype inverter. Simulation and experimental results show that the neutral point is controlled to be better than 0.5 in 800 V, even in the presence of a transient single-phase load of close to the maximum inverter current.

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