Towards a reconfigurable sense-and-stimulate neural interface generating biphasic interleaved stimulus

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Abstract—This work presents an eight channel neural stimulator interface based on an address event communication protocol. The system developed decodes, integrates and interleaves the spike patterns using a continuous interleave sampling (CIS) strategy, which drives a complex biphasic current waveform to a bipolar electrode configuration. This paper describes the basic concept, circuit design, simulation results and hardware implementation in a standard $0.35\mu\text{m}$ CMOS technology.

I. INTRODUCTION

The field of neuroprosthetics has been evolving over the last five decades and its application base is expanding considerably. From functional electrical stimulation (FES) restoring muscular movement in paraplegics and stroke patients, to the mainstream medical device industries developing pacemakers, cochlear and soon retinal implants, neuroprosthetics have revolutionised treatment of previously incurable conditions. This is further emphasised with the development of neuromodulation devices for rehabilitation after spinal cord injury, pain relief and treatment of epilepsy and depression [1].

Most commercially available stimulators are open-loop, featuring externally-controlled or pre-programmed stimuli. However, results indicate that they are power consuming and therapeutically ineffective due to their inability to activate muscles or organs automatically when the need arises.

For this reason it is desirable to achieve a sense-and-stimulate system, both for closed-loop FES as well as for neural lesion bypass devices, where activation of a muscle affected by a severed neural path is triggered by command bio-signals generated by nerves preceding the injury.

The idea of closed-loop stimulators and neural-bypass systems was first expressed in the sixties, as illustrated in Fig. 1 [2], and at the time it was mostly viewed as non-implementable. However, research in neurostimulation coupled with advances in integrated technologies has made such systems technically feasible and in the last two decades closed-loop systems are the main research focus in this field.

Making a such a system implantable is not a trivial task, with the front-end (neural-monitoring sensors) suffering from biocompatibility issues, low SNR and poorly documented specifications. The processing stage is limited by power and area constraints and the output stage has to satisfy issues of power, safety and selectivity. In addition, the need for wireless transcutaneous communication with an external device offering supply and data transmission increases the overall complexity.

Other than these constraints, important factors hindering development in this field is the intense diversity between devices being developed for different applications. According to Troyk et. al [3], research in stimulation in the past 20 years has been erroneously focusing mainly on studying particular neurogenic disorders. This then yields the need for specific technologies to be developed, rather than developing appropriate advanced devices that can then

be tailored for specific conditions. This yields a variety of electrode configurations, as well as different stimulus current amplitudes and waveforms for different types of interfaces. Moreover various signal processing and transmission methods, all with their own advantages have been developed [4].

Thus it is evident that the development of a generic sense-and-stimulate device featuring multiple re-configurable channels would revolutionise neuroprostheses leading to much more coherent research and delivering highly efficient rehabilitation practices.

Fig. 1. Reproduction of a 1964 figure from [2] illustrating an "electronic bypass for motor neuron lesion"

The work presented here is part of a project that considers the development of a generic sense-and-stimulate system with adaptable architecture whose purpose is to offer an alternative to single-use devices in the field. In the context of the overall project, parallel development of all three stages of signal sensing, processing and transmission as well as stimulation takes place. The portion of the project presented in this paper is concerned with the last two stages, with the front end briefly described in the next section. The rest of the paper is organized as follows: Part II provides some theoretical background regarding stimulation parameters, while Part III outlines the system architecture. Part IV describes the implementation of the various blocks, Part V presents system simulation results, and finally, Part VI summarizes the system submitted for fabrication and discusses future work.

II. STIMULATION THEORY

Typically, in electrical neural stimulation, a minimum of two electrodes are used to produce a nerve activation current. The pair can be used in monopolar or bipolar configuration [5]. In multipolar stimulation schemes, the bipolar scheme (active and reference electrode are placed close to the nerve) is preferred as it allows greater activation selectivity because each pair generates a more localized field [5] (compared to monopolar).

Stimulus pulse parameters include frequency, amplitude and duration. The former affects the smoothness of muscle contractions and needs to be adjusted to prevent muscle fatigue. The latter two

parameters affect the strength of contraction by altering the charge injected.

As established by [6], in order to avoid harmful electrochemical processes, the stimulus waveform has to be biphasic. In such a waveform the first pulse causes activation, followed by a second one with opposite polarity to balance the charge delivered by the first [5]. However, it has been reported [1] that two opposite pulses back to back actually act to prevent the generation of an action potential. To overcome this, a short time delay needs to be introduced between the pulses [1]. Additionally, using an extended anodic pulse with reduced amplitude can compensate for charge distribution and thus reduce fatigue.

III. SYSTEM OVERVIEW

The system was developed such that virtually any sense signal can be interfaced to the front-end providing the input to the system. The requirement for the system is that at the sensor output (i.e. system input), an event must occur, causing a trigger. The trigger is transmitted via an asynchronous digital bus, in the form of a pulse using an Address Event Representation (AER) architecture [7]. Input events causing the trigger can be of any form, for example, a threshold crossing, frequency detection, etc.

The overall system developed incorporated an ion-selective field-effect transistor (ISFET) to sense Potassium (K) ion concentration, modulating a spiking neuron circuit that in turn provides the required pulse stream stimulus to an address-event transmitter. The back-end stimulation interface described here consists of an address-event receiver (i.e. event demultiplexer) feeding multi-channel stimulus generators. Each of these includes a ripple counter, digital-to-analogue converter (DAC), CIS controller and biphasic waveform driver.

The full system architecture is shown in Fig. 2, with the back-end portion annotated. The system described uses a pulse stream to generate a stimulus pulse whose magnitude is linearly related to the number of trigger events. Although the system does not include hardware to pre-process the input stimulus, for example, by scaling or providing non-linear compression, such functions can be easily implemented by intercepting the AER bus and performing pulse stream processing [8].

The stimulus pulse itself has been chosen to follow a biphasic profile and to stimulate one or more bipolar electrode configurations. To generate this stimulus the system is designed in three stages. Firstly, the spike (or pulse) rate (indicating the stimulus trigger magnitude) is measured and converted to a current level. This current

Fig. 2. General system architecture illustrating three main blocks: An 8-bit asynchronous ripple counter (capturing the number of events in each integration cycle), a binary-weighted current mirror that converts the number of pulses to a current level and a CIS biphasic waveform generator.

generated directly provides the stimulation magnitude to be delivered via the electrodes. In the sections following the sequence of events from trigger pulses to biphasic waveform will be described.

IV. IMPLEMENTATION

A. Spike-rate to current conversion

The spike-rate capture was implemented by means of an asynchronous ripple counter that is reset each stimulation cycle. Although there exist several alternative methods of achieving this, the chosen method, generating a binary representation can then directly control a binary weighted current mirror. Depending upon this value, binary weighted currents can be switched in and summed at a central node (Fig 3) to generate the required current. By doing this, using an accurate current mirror implementation, a monotonically increasing current conversion is achievable, representing the pulse rate, essentially integrated over each CIS cycle.

Fig. 3. The method used to double the current reference in each of n-stages. The output current, I_{out} , is fed to a summing junction if its binary weighting is high. For example, for an input 01, $Cntrl1$ will be high (i.e. feeds current) and $Cntrl2$ would be low.

Due to the relatively variable efficiency for artificial electrical stimulation, a total of 256 output levels (in linear increments) is sufficient for this system and thus an 8-bit counter was required. This has been implemented using a cascade of asynchronous t-flip-flops with common asynchronous reset for clearing the counter on completion of the output sequence for that CIS cycle. Furthermore, this counter is disabled during the readout phase in order to prevent variation in the output current during stimulation. In a similar fashion, this inhibit signal is used at several points to prevent unnecessary current flow and therefore minimise power consumption. For example, the current mirrors feeding the stimulation current are enabled only during each channels stimulation slot. This spike-rate to current conversion hardware has been repeated for each channel. Although this is not completely necessary for this CIS implementation, (i.e. the output of the 8 counters could have been multiplexed such that only a single binary-weighted current tree is required), a repeatable block is preferred to simplify timing constraints and maintain scalability.

B. Continuous Interleave Sampling Controller

The CIS strategy is an attractive scheme for systems requiring multi-channel stimulus delivered to stimulation points within close proximity. In comparison to alternative strategies, including compressed analog (CA) and spectral peak (SPEAK), the CIS strategy has been shown to be beneficial [9], particularly in cochlear implant technology. One of its fundamental features is the reduction in cross-talk between adjacent channels caused by interaction of electric fields from simultaneous electrode stimulation. Although conventional CIS strategy is not highly accurate in residual charge balancing, introducing an electrode shorting phase in the stimulation cycle can eliminate this effect.

It is with this insight and ease of implementation that the CIS strategy is chosen for this system. This was implemented by simply cycling through the different channels and sequentially driving the stimulation electrodes with their respective current stimulus. Thus no two channels are ever simultaneously active, reducing power dissipation. This is achieved by generating an enable sequence as shown in Fig. 4. In case more than two channels need to be active, respective modules like the system described here can be combined in a single chip, featuring fewer individual channels to keep power consumption low.

Fig. 4. Implemented CIS timing illustrating channel selection using a sequential enable phase. The biphasic output waveform is also shown.

To implement the sequence in Fig. 4, a 5-bit ripple counter is used, with the three most significant bits being used to provide the various channel enable signals, therefore achieving four clock cycle stimulation phases as described below. With this clocking sequence, the eight channels can be easily interleaved by using an address decoder to provide the "enable signal" for each channel. Modifying the digital logic that governs the "Enable Pulse Generator" (Fig. 5) operation will allow variation of the stimulation strategy.

Fig. 5. Block diagram illustrating the implementation of the CIS strategy using a 3-bit counter.

C. Stimulation Stage

In light of the required stimulus parameters discussed earlier, the system was developed to generate a four phase stimulation waveform as shown in Fig. 4. In order to achieve such a four phase biphasic waveform it is necessary to generate the necessary control signal to drive the H-bridge configuration as shown in Fig. 6. These switches are controlled by a 2-bit ripple counter, used to generate four phases (11,00,01,10).

When the channel enable signal (shown in Fig. 4) is high for a particular channel, then the clock signal is applied to the counter, generating the four phases (hence the need for four clock cycles, mentioned in IV-B). Combinational logic is included to guarantee the start-up conditions, i.e. power-on-reset. The external enable signal

Fig. 6. Circuit schematic for the biphasic waveform generation using an H-bridge configuration. The control signals are generated using the remaining 2-bit counting sequence and the enable pulse to short the electrodes when channel not in use (for residual charge removal).

TABLE I
COMBINATIONAL LOGIC TO CONTROL BIPHASIC CURRENT STIMULATION

	E1	E2	S1	S2	S3	S4
$\phi 1$	0	1	0	1	1	0
$\phi 1$	0	0	0	0	1	1
$\phi 1$	1	0	1	0	0	1
$\phi 1$	1	0	1	0	0	1

is used to ensure that the electrodes are shorted (as described in IV-B).

The combinational logic required to control the switches such that the current sourcing and sinking electrodes are configured as required is shown in Table I. Furthermore, during the last two phases it is necessary to halve the stimulus current, due to the waveform profile described previously, i.e. to maintain area equivalence on both pulses. This is achieved by switching in (in the last two phases) a current mirror stage between the current generating stage (described in section IV-A) and the biphasic current control switches (Fig. 6). The method followed here will be similar if the system has to be designed with the charge-balancing pulse longer and lower in amplitude. Moreover, the stimulus current amplitude, duration and frequency can be adjusted, according to the application.

V. SIMULATION RESULTS

This design is implemented in the AMS C35 CMOS technology using the HITKIT (3.70) design kit under the Cadence IC (5.1.41) design environment. The floorplan and layout of the design submitted for fabrication is shown in Fig. 7.

This section presents key simulation results, demonstrating intended system operation. Firstly, Fig. 8 illustrates a monotonically increasing spike-to-current conversion over the entire output range (256 levels). One observation is regarding the charge injection during switching, caused by the release of charge built-up during the off-state. This is introduced at two levels, firstly at the switched binary-weighted current mirror, and secondly at the channel selection switch. However, although the peak charge-injection current magnitude seems significant, the transition time is extremely short. Hence, the actual amount of charge injection is negligible (Fig. 8b). Furthermore, as previously mentioned, all inactive electrodes are routinely shorted during the electrode reset phase, ensuring that no residual charge remains after stimulation.

Next, Fig. 9 illustrates the biphasic waveform profile generated in the CIS sequence. This simulation incorporates a neural interface

Fig. 7. Chip floorplan and lay of the spike-driven neural stimulator

Fig. 8. Monotonicity of the event-count to current conversion, illustrating: (a) switched current output, and (b) current integral, i.e. charge transfer

macromodel assuming a $1K\Omega$ equivalent electrode impedance [10]. The pulse waveform is clearly visible to have four phase profile, following: (i) a single period anodic current, (ii) a single period break and (iii) a two period attenuated (halved) cathodic current. Also the CIS strategy can be observed, with each channel cycled through sequentially with no overlapping outputs.

Fig. 9. Biphasic pulse waveform generated sequentially using a CIS strategy. The pulses have a four phase profile, but with equal anodic/cathodic charge distribution for removal of residual charge on the nerves

VI. DISCUSSION

The design specifications for this system are summarised in Table II. An architecture was presented for generating multi-channel biphasic stimulus for neural stimulation using the CIS strategy. The system developed is the core of a generic, closed-loop sense-and-stimulate system architecture. The system is designed such that a

TABLE II
DESIGN SPECIFICATIONS FOR THE SPIKE-DRIVEN NEURAL STIMULATOR

Technology	AMS 0.35 μ m 1P4M CMOS
Supply voltage	3.3V
System device count	4106
Channels	8
Stimulation strategy	Continuous Interleave Sampling (CIS)
Electrode configuration	Bipolar
Stimulus profile	Complex biphasic waveform
Stimulus Range	100 μ A-5mA (tunable)
Input/output dynamic range	48dB (8-bits)
Refresh rate	100Hz-20kHz (tunable)
Area	3mm ²
Power Consumption	0.7-25.2mW (stimulus current dependant)

range of input neural recording interfaces can be used at the front-end. The detected neural activity is then used to trigger stimulation. The key stages described can be configured to generate a variety of stimulus waveform characteristics, and a combination of different electrode configurations through different connection arrangements, making it appropriate for use on both central and peripheral nerves.

It was shown how an event-triggered address-encoder can be used to directly generate a biphasic current pulse whose magnitude is proportional to the input activity. The output stimulus pulse train was optimum for tissue safety and can be incorporated in multipolar electrode combinations. Its amplitude range can be externally programmed for different applications.

Being reconfigurable, the system presented here may lead to coherence in neuroprosthetics research and will deliver highly efficient rehabilitation practices.

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