A Micropower Tilt Processing Circuit

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Abstract—This paper describes a novel analogue circuit for extracting the tilt angle from the output of a linear MEMS accelerometer. The circuit uses the accelerometer signal together with the gravitational acceleration vector to generate the tilt signal. Using a current-mode representation with MOS devices operating in weak inversion, the appropriate trigonometric function has been realised to compute tilt. Furthermore, implementing a long-time constant filter to extract the mean tilt level provides adaptation to the static tilt level. Specifically, this circuit has been designed as part of an implantable vestibular prosthesis to provide inclination signals for bypassing dysfunctional otolith end-organs. The circuit has been fabricated in AustriaMicroSystems 0.35 μm 2P4M CMOS technology and this paper presents the theory, implementation and measured results.

Index Terms—tilt, inclination, trigonometric function, arcsin, vestibular prosthesis, analogue signal processing

I. INTRODUCTION

AN increasing number of medical devices including implantable prosthetics and body worn instrumentation are incorporating sense systems within and around the body. Physical constraints demand such systems to be compact and lightweight, and the need for autonomy imposes stringent power budgets on such systems. One such sensor is the *inclinometer* (or tilt sensor), which senses its orientation with respect to gravity.

Tilt sensors are typically implemented using hybrid structures incorporating a stationary reference and movable mass. Traditionally these have been realised using electrolytic fluid-filled cavities, for example- a container in which an array of incremental electrodes are patterned and which is filled with mercury (or non-toxic alternatives). More recently, a number of silicon-based inclinometers have been developed [1]–[4] implemented in various MEMS technologies. Although these typically rely on a proof mass being deflected, alternative approaches have been reported using convection [5] and optical micro-filters [6]. It has also been shown how to derive inclination using an unmodified accelerometer [7]–[9].

In this paper, we present a novel hardware implementation of a front end circuit to interface to an accelerometer and generate a tilt signal. This has been implemented as part of a vestibular prosthesis to provide cues about inclination and bypass dysfunctional otolith end-organs within the vestibule in the inner ear. This paper describes the application (Section II), the concept and system architecture (Section III), circuit

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Fig. 1. Simplified organisation of the vestibular prosthesis illustrating the signal flow chain for each channel. The presented tilt processing circuit (highlighted) is required for the two linear (i.e. otolith) channels taking an accelerometer input and feeding the arcsine output to the current-mode stimulator.

implementation (Section IV), simulated and measured results (Sections V and VI).

II. VESTIBULAR PROSTHESIS

Individuals suffering from dizziness and balance disorders can benefit from recent advances made in neural prostheses and more specifically, cochlear implants. The inner ear constitutes two sub-organs, the *cochlear* and the *vestibule*, responsible for sensing sound and inertia and sending the information to the brain via the VIII'th cranial (i.e. vestibulocochlear) nerve. The vestibular system senses the head's motion and orientation using the ampullary (within semicircular canals) and otolith (utricle and saccule) end-organs which help stabilise vision via the vestibulo-ocular reflex (VOR). Vestibular dysfunction often manifests itself as dizziness, imbalance, blurred vision and instability in locomotion, due to abnormal signalling to the brain. It is therefore possible, that damage to this system can be overcome by applying similar methodologies to those used in modern neural implants. Specifically, it has been shown that restoration of balance can be achieved by bypassing a dysfunctional element in the vestibular pathway using artificial stimulation [10], [11].

The vestibular system consists of three semicircular canals positioned approximately orthogonal to each other to sense radial acceleration in the three axes. Additionally it includes two *Otolith* organs; the *Utricle* and *Saccule* which function to detect linear acceleration relative to gravity in two planes again approximately orthogonal to each other. The Utricle and Saccule are positioned to have their sense axes approximately parallel to the horizontal (axial) and vertical (coronal) planes respectively. These detect inertia by moving a deformable

Fig. 2. The concept of obtaining tilt from an accelerometer using the gravitational acceleration vector.

damped mass and use tiny hair cells to transduce inertia (mechanical energy) to electrical impulses.

Our vestibular prosthesis aims to bypass dysfunctional elements in the vestibular organ by using MEMS sensors (i.e. gyroscopes and accelerometers) to detect inertia and convey the appropriate signal to the VIIIth nerve using artificial electrical stimulation at the afferent nerve endings. This process is illustrated in Fig. 1, with the linear acceleration channel highlighted. Here, as both the input and output of the arcsine processor interface with analogue signals (i.e. voltage output from MEMS accelerometer and current input to stimulator), an analogue realisation would be hugely desirable. A conventional approach based on a look-up table would additionally require analogue-to-digital and digital-to-analogue converters and therefore would significantly increase complexity. As our application has limited output dynamic range, i.e. the usable range for electrical stimulation is typically limited to 20-25dB [12], it is acceptable to tolerate some error in the signal flow without compromising system performance. We therefore propose to utilise a fully analogue arcsine approximation, detailed herein.

III. SYSTEM OVERVIEW

The circuit presented in this paper is based on the concept that for any sensed acceleration there exists a component due to the gravity, except in the case that the axis of reference is perpendicular to the gravitational acceleration vector. This concept is illustrated in Fig. 2. As the inclination is varied, (i.e. the angle between the horizon and the accelerometers sense axis), the detected inertia (i.e. acceleration) changes proportionally to the sine of the tilt angle. The sensed acceleration is in fact the component of gravitational acceleration and therefore can vary from $-g$ to $+g$ (corresponding to -90° to $+90^\circ$). Consequently, this means that any accelerometer can be used as a tilt sensor provided the following criteria are met: (1) the accelerometers range is equal to or greater than the gravitational constant i.e. $\pm g$ and (2) the accelerometer does not exhibit any out-of-plane non-linearities, i.e. due to proof mass sagging. However most MEMS-based capacitive accelerometers fulfil this criteria as they are typically designed to be stiff in the out-of-plane axis.

The system architecture of the proposed front-end is shown in Fig. 3. This has been designed to be used with an off-the-shelf accelerometer taking a voltage output centred between the supply rails. Specifically the Analog Devices ADXL330 has a nominal output (i.e. at $0g$) of $0.5VDD$ and sensitivity of

Fig. 3. System architecture for the implementation of the tilt processor concept.

$0.1VDD/g$. For a 3.3V supply this translates to an input range between 1.32V ($-1g$) and 1.98V ($+1g$) which corresponds to a tilt of between -90° and $+90^\circ$.

To extract the DC level (i.e. zero tilt ratiometric output) of the accelerometer a long time constant low-pass filter based on an operational transconductance amplifier-capacitor (OTA-C) (i.e. GM1 and C) realisation has been used. This assumes the target object will be changing tilt at a higher rate and will inherently provide adaptation to a change in static inclination. For our application this is crucial as this mimics the biomechanical and neural adaptation within the physiological vestibular organ. Alternatively this filter can be replaced with a DAC or voltage reference if an absolute measure of tilt is required about a static reference. The voltage signals (accelerometer output and extracted DC level) are then converted to a differential current output using a linearised transconductor. This allows for the implementation of a transimpedance arcsine transfer characteristic.

IV. CIRCUIT IMPLEMENTATION

A. Low-pass OTA-C filter for DC level extraction

To extract the DC-level of the accelerometer output, a long time constant filter ($\tau > 10s$) has been implemented using an OTA-C implementation. The schematic for the OTA is shown in Fig. 4(a) [13]. The adopted implementation is based on a balanced OTA and has a 10nA split tail current feeding two PMOS differential pairs Q6-Q7 and Q8-Q9 which share the signal current in a ratio of 1:4. Any mismatch here would affect the current division and therefore manifest itself as a signal imbalance. Thus we have designed large area devices to achieve good matching (20/20 and 80/20 respectively). The effective differential pair has been actively linearised by Q5 and Q10, as the required linear input range and current magnitudes made resistive degeneration an unviable option. The current is further scaled in the NMOS current mirrors Q11-Q14 and Q15-Q18 by a ratio of 5:1. Cascoded current mirrors were used to ensure a well-balanced output and all the inner mirrors (i.e. Q3-Q4, Q11-12 and Q15-Q16) have been realised using thick oxide devices. This has been engineered specifically to limit the drain-source leakage at low current levels ($< 20pA$) especially within the standard NMOS devices. We have chosen to implement only the inner mirrors using thick oxide devices to save headroom, i.e. $V_{threshold}(\text{standard oxide}) = 0.46V$ whereas $V_{threshold}(\text{thick oxide}) = 0.7V$, whilst

Fig. 4. Circuit schematic for the tilt processing circuit (excluding bias generation). Shaded regions illustrate: (a) OTA-C low pass filter for DC level extraction, (b) linearised OTA for V to I conversion, and (c) arcsine transimpedance converter.

still maintaining the leakage current limiting performance. We have primarily used large device sizes ($W \times L$) to achieve the required level of matching but this also aids to reduce both the flicker and thermal noise contributions. Additionally, the devices have been designed to have relatively long channel lengths ($L=10\mu\text{m}$) to further improve thermal noise (i.e. by reducing the W/L aspect ratio). The achieved transconductance is 18pS and this coupled with a load capacitance of 40pF , provides a low pass characteristic with time constant of approximately 14s .

B. Linearised OTA

The OTA used to obtain a fully differential current output to drive the arcsine system is shown in Fig. 4(b). This uses a fully differential topology using resistive degeneration to achieve a linearised response for an input range of $\pm 330\text{mV}$. To ensure good matching between the source degeneration resistors ($R1$ and $R2$), these have been implemented as a single resistor, i.e. $R=R1+R2$ and the bias current has been split at each node, i.e. 333nA are sourced at each node. We have chosen this approach as MOS devices can be made to match better than poly-poly capacitors and therefore matching two currents is easier than matching two resistor values. Furthermore, to limit the value (and silicon area required) of the degeneration resistor ($1.2\text{M}\Omega$) required to provide a linear input range the source current has been selected to be 667nA . However, the requirement to feed the arcsine system an input no greater than $\pm 45\text{nA}$ requires an output current scaling of $10:1$. This is implemented using scaled current mirrors $Q25$ - $Q27$ and $Q28$ - $Q30$. Additionally, to achieve a bidirectional output current, these mirrored currents are cross-coupled via PMOS mirrors $Q19/Q22$ and $Q20/Q21$. This transconductor therefore achieves a linear transconductance of 136.4nS (i.e. $\pm 45\text{nA}/\pm 330\text{mV}$).

C. Arcsine System

It has been shown possible to generate a sinusoidal transfer characteristic based on an exponential primitive. Meyer et al. [14] were amongst the first to report that a differential pair with emitter degeneration could be used as a triangle-sine wave converter in bipolar technology. Gilbert [15] extended this technique to provide realisations of other trigonometric functions including their inverses. With weak inversion CMOS technology it has been shown possible to achieve the sine function [16]. We use this technique in reverse to realise the inverse function. This requires driving the differential pair with a current and reading out the voltage at what was previously the input node.

The implemented circuit producing an arcsine transfer characteristic is shown in Fig 4(c) [17]. This is based on a weak inversion MOS differential pair which has been diode connected to have a logarithmic input current to output voltage transfer. The emitter degeneration has been implemented in the form of the preceding V to I conversion (linearised OTA detailed previously).

Arcsine approximation: Based on the methodology used by [14], we have applied this to the arcsine function using weak inversion MOS devices. Starting at the outputs, the node voltages can be expressed (via KCL) as:

$$V_{OUT1} = V_{GS(Q32)} + V_{GS(Q34)} + I_{IN}/G_{M2} \quad (1)$$

$$V_{OUT2} = V_{GS(Q31)} + V_{GS(Q33)} - I_{IN}/G_{M2} \quad (2)$$

Where G_{M2} is the transconductance of the linearised OTA stage and therefore I_{IN}/G_{M2} represents the differential output voltage (assuming a perfectly linear transconductance). Assuming devices $Q31$ - $Q34$ are identical and well-matched, then $V_{GS(Q31)} = V_{GS(Q33)}$ and $V_{GS(Q32)} = V_{GS(Q34)}$, and

combining with (1) and (2) gives:

$$V_{OUT1} - V_{OUT2} = 2 \left(V_{GS(Q32)} + \frac{I_{IN}}{G_{M2}} - V_{GS(Q31)} \right) \quad (3)$$

If devices Q31-Q34 are all operating in weak inversion then the basic expression for gate source voltage is given by: $V_{GS} = nV_T \ln(I_D/I_S)$, where n is the subthreshold slope factor, V_T is the thermal voltage, I_D is the source-drain current and I_S is the pre-exponential saturation current. Substituting this into (3) gives:

$$V_{OUT1} - V_{OUT2} = 2 \left[\frac{I_{IN}}{G_{M2}} + nV_T \ln \left(\frac{I_{D(Q32)}}{I_{D(Q31)}} \right) \right] \quad (4)$$

By substituting $I_{D(Q31)} = I_{BIAS} - I_{IN}$ and $I_{D(Q32)} = I_{BIAS} + I_{IN}$ and re-arranging, the following expression is given:

$$V_{OUT1} - V_{OUT2} = 2 \left[\frac{I_{IN}}{G_{M2}} + nV_T \ln \left(\frac{1 + \frac{I_{IN}}{I_{BIAS}}}{1 - \frac{I_{IN}}{I_{BIAS}}} \right) \right] \quad (5)$$

Expressing the logarithmic term (for $|I_{IN}| \leq I_{BIAS}$) using a Taylor series expansion gives:

$$\ln \left(\frac{1 + \frac{I_{IN}}{I_{BIAS}}}{1 - \frac{I_{IN}}{I_{BIAS}}} \right) = 2 \left(\frac{I_{IN}}{I_{BIAS}} \right) + \frac{2}{3} \left(\frac{I_{IN}}{I_{BIAS}} \right)^3 + \frac{2}{5} \left(\frac{I_{IN}}{I_{BIAS}} \right)^5 + \dots \quad (6)$$

Substituting (6) into (5) and re-arranging gives:

$$\frac{V_{OUT1} - V_{OUT2}}{2nV_T} = \left(2 + \frac{I_{BIAS}}{nV_T \cdot G_{M2}} \right) \left(\frac{I_{IN}}{I_{BIAS}} \right) + \frac{2}{3} \left(\frac{I_{IN}}{I_{BIAS}} \right)^3 + \frac{2}{5} \left(\frac{I_{IN}}{I_{BIAS}} \right)^5 + \dots \quad (7)$$

If this is now compared to a Taylor Series expansion for the arcsine function:

$$\sin^{-1} \left(\frac{I_{IN}}{I_{BIAS}} \right) = \left(\frac{I_{IN}}{I_{BIAS}} \right) + \frac{1}{2} \frac{1}{3} \left(\frac{I_{IN}}{I_{BIAS}} \right)^3 + \frac{1}{2} \frac{3}{4} \frac{1}{5} \left(\frac{I_{IN}}{I_{BIAS}} \right)^5 + \dots \quad (8)$$

Therefore, to achieve the following relationship:

$$V_{OUT} = V_{OUT1} - V_{OUT2} = A \cdot \sin^{-1} \left(\frac{I_{IN}}{I_{BIAS}} \right) \quad (9)$$

Substituting (8) into (9) gives:

$$V_{OUT} = A \cdot \left[\left(\frac{I_{IN}}{I_{BIAS}} \right) + \frac{1}{6} \left(\frac{I_{IN}}{I_{BIAS}} \right)^3 + \frac{3}{40} \left(\frac{I_{IN}}{I_{BIAS}} \right)^5 + \dots \right] \quad (10)$$

Therefore, to approximate (10) to (7) we define the arcsine gain term:

$$A = 2nV_T \left(2 + \frac{I_{BIAS}}{nV_T \cdot G_{M2}} \right) \quad (11)$$

This should be used when designing the circuit to match (as closely as possible) the third and fifth order terms between the

Fig. 5. Simulated AC response of the OTA-C low pass filter showing magnitude (top) and phase (bottom) response.

two expansions (i.e. logarithmic and arcsine). To achieve this, the design parameters that can be varied are: I_{BIAS} and G_{M2} . Firstly, I_{BIAS} is selected such that the weak inversion dynamic range is maximised. Specifically I_{BIAS} is selected such that at that bias the devices are at the transition between moderate and weak inversion. During balanced operation however, the nominal drain currents will be half this value and therefore there is some margin to the non-ideal (distorted exponential) region. G_{M2} is then designed by calculating the constant required to ensure correct scaling, i.e. between (7) and (10).

V. SIMULATION RESULTS

The circuit was simulated using the Cadence Spectre (5.1.41isr1) simulator with foundry supplied BSIM3v3 models.

A. AC Analysis

The AC response of the OTA-C low pass filter is shown in Fig. 5. This shows that the time constant of the filter is 13.9s (i.e. F3dB=72mHz).

B. Transient Analysis

Transient simulations taking a static DC operating point and a triangular wave as inputs illustrate the linearity of the transconductor used for the V-to-I are shown in Fig. 6. For input voltages of $V=1.65V$, $1.32V \leq V \leq 1.98V$, the output currents are $-45nA \leq I_{out}(-/+) \leq 45nA$.

The arcsine transfer function has been simulated by providing a differential sinusoidal current to the circuit and observing the differential voltage output. The transient simulation results has been reported in [4]. The simulated output error relative to an ideal triangle wave is 2.76% (based on RMS calculations).

C. Noise Analysis

A noise analysis of the arcsine processing circuit reveals the input-referred noise to be approximately $90\mu V$ at 1Hz (shown in Fig. 7). Assuming a differential input signal of $\pm 330mV$ gives a signal-to-noise ratio (SNR) of 77.3dB. As

Fig. 6. Simulated transient response for the linearised transconductor. Shown is: (a) input voltages (V^- and V^+), (b) output currents (I^- , I^+ and I_{diff}), and (c) parametric analysis showing effect of resistive emitter degeneration (for $0 \leq R \leq 1.1M\Omega$).

Fig. 7. Simulated noise analysis for the complete arcsine processing circuit. Shown is the input referred noise plot versus frequency.

this is much higher than the dynamic range of the arcsine processing circuit, which is currently limited because of the arcsine approximation (see above) and implementation non-idealities (see discussion on sources of error further below in measured results), therefore it is safe to neglect the noise contribution of the circuit.

VI. INTEGRATED CIRCUIT AND MEASURED RESULTS

The circuit has been designed and fabricated in a commercially available CMOS technology (AMS 0.35 μ m 2P4M). The chip microphotograph is shown in Fig. 8.

Fig. 8. Chip microphotograph of the tilt processing circuit with floorplan overlaid.

Fig. 9. Measured results illustrating the arcsine response to a 200Hz input sine waveform. The signals (from top to bottom) are as follows: (a) input signal, (b-c) differential outputs, (d-e) single-ended output and ideal output (triangle wave), and (f) error (absolute and % linear).

Fig. 10. Measured results illustrating operation of the tilt processing circuit within a $\pm 75^\circ$ range. The signals (from top to bottom) are as follows: (a) input signal (sinusoidal variation in acceleration), (b-c) differential outputs, (d-e) single-ended output and ideal output (ramp, i.e. linear variation), and (f) error (absolute and % linear).

To measure circuit performance, the die has been packaged in a JLCC44 package, housed in a custom PCB to connect with the required instrumentation. The circuit outputs are buffered at PCB-level using OPA602 unity-gain configured op-amps to drive the BNC load. Power supply and bias currents are sourced using Keithley sourcemeters (model: 2602) and the output is captured on a 4-channel oscilloscope (LeCroy WavePro 7300A). Measured data confirm the circuit operates to the intended design specification.

Measured results are shown in Figs. 9 and 10. The operation of the arcsine operator is illustrated in Fig. 9. These results show the response of the circuit ($vout(arcsine)$) to a 200Hz input sinusoid (vin), and therefore a triangular output wave would represent a perfect arcsine. The generated waveform (i.e. $vout1-vout2$) is subtracted from the expected,

TABLE I
MEASURED SYSTEM SPECIFICATIONS

Technology	AMS 0.35 μ m 2P4M CMOS
Die area (core)	750 μ m $\times$ 250 μ m
Supply voltage	3.3V
Device count	152
Low-pass filter bandwidth	-3dB @ F=72mHz
Input voltage range	1.32V to 1.98V
Output voltage range	$\pm$ 225mV (differential signal)
Conversion gain, A	0.682
Arcsine error (simulated) [†]	2.76% (over $\pm$ 90 $^\circ$ range)
Total system error (measured) [†]	3.76% (over $\pm$ 75 $^\circ$ range)
	6.96% (over $\pm$ 90 $^\circ$ range)
Total system power consumption (simulated, measured)*	4.950 μ W, 4.963 μ W

$$\dagger \text{error}(\%) = \left[A \cdot \sin^{-1}(V_{in}) - (\Delta V_{out}) \right]_{rms} \cdot \left[A \cdot \sin^{-1}(V_{in}) \right]_{rms}^{-1}$$

*Current consumption excludes bias (1.1 μ A).

i.e. vout(ideal) and the error signal is shown (bottom trace). The measured rms error is approximately 7.0% over the entire waveform. Fig. 10 illustrates the operation within the tilt sensing range, i.e. $\pm$ 75 $^\circ$. As the point of maximum distortion occurs at the crest and trough of the input wave, limiting the range of operation of the tilt sensor to $\pm$ 75 $^\circ$ (instead of $\pm$ 90 $^\circ$) improves the accuracy, i.e. the average error is reduced from 7.0% to 3.8%. This error can be attributed to the following three sources:

- 1) Due to the arcsine approximation from the Taylor expansion, only the first three terms have been considered, thus even a perfect implementation would include an error.
- 2) The weak inversion region of a MOS device is typically limited to two to three orders of magnitude, with a pure exponential response only within a central band. Any deviation from an exponential would distort the logarithm and therefore distort the arcsine characteristic.
- 3) Since the DC operating point is extracted using a low pass filter, this inherently results in an output offset. This is firstly because the filter implementation itself is not perfectly linear, i.e. the transconductor uses active degeneration for linearisation. Secondly, the use of the filter to extract the DC level means that for signals comparable (within 1 order of magnitude) to the filter cut-off, there will inevitably be some feed-through.

It can therefore be concluded that the 2.76% error determined from the simulated results is due to the arcsine distortion, i.e. source (1) listed above. Therefore, the remaining discrepancy between simulated and measured data, i.e. 6.96 - 2.76 = 4.20% can be attributed to sources (2) and (3) listed above.

The system specifications are summarised in Table I.

VII. CONCLUSION

In this paper we have presented an integrated circuit for use in generating a tilt signal from an accelerometer output. The system designed takes a voltage input from a standard accelerometer. We have aimed to produce a fully analogue implementation for applications requiring an analogue tilt

signal. Furthermore, the circuit extracts the DC operating point through means of a long time constant low pass filter, alleviating the need for calibration or tuning. This additionally provides adaptation to a non-static reference level which is advantageous in many biomedical applications. The intended application for this circuit is as part of a fully implantable vestibular prosthesis for the restoration of balance. Through an analytical formulation of the circuit theory the key concept is developed, and confirmed experimentally with simulated and measured system results.

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