Modular Multilevel DC/DC converter architectures for HVDC taps

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Abstract

DC/DC connections between DC voltage levels in High Voltage Direct Current (HVDC) schemes are useful for interconnection between links and as taps to inject/extract relatively small amounts of power. Taps with high voltage transformation ratios (such as 500 kV to 50 kV) are particularly challenging to achieve with reasonable use of semiconductor ratings. Four architectures of DC/DC converter covering both direct connection and transformer-interfaced are analysed and compared in terms of the ratio of their apparent power rating (rated current times rated current summed across all stacks of the cells) to the throughput power. It is found that the direct conversion architectures have reasonable power capacity factor only for low transformation ratios (of 2:1 or less) but the inclusion of a transformer and intermediate square-wave operation allows much wider transformation ratios with a reasonable power capacity factor. For each design the nature of the cell-balancing currents has been determined since this is a major factor in determining the total current flow in each cell stack.

Introduction to HVDC Transmission

Across Europe renewable energy sources (RES) are becoming an ever more important component of the energy mix. Whilst the exact goals for RES content might vary between nations, most anticipate an increase in RES capacity over the coming years. RES however are inherently inflexible in terms of location of generation which requires new transmission corridors to facilitate this expansion.

High Voltage Direct Current (HVDC) transmission technologies are seen as the key component to connect a number of planned off-shore wind-farms as well as provide greater transmission capacity between countries. Some concepts envisage a transmission backbone which stretches from the Norwegian hydro plants through central Europe to Northern Africa [1]. Whilst this may or may not happen in the distant future, a number of projects are pointing the way already. One such example is the recently published plan to build three north-south transmission corridors in Germany using HVDC [2]. A number of connections to off-shore wind-farms in the north-sea may become the foundation for a multi-terminal HVDC network for northern Europe [3].

For such multi-terminal applications, Voltage Source Converter (VSC) technology is considered most suitable [4]. The Modular Multi-level Converter (MMC) [5] is currently the most commonly promoted architecture although alternatives exist in the literature [6-7]. The popularity of the MMC is not least due to its modular design using sub-modules, or cells, consisting of half- or full-bridges. Such cells can be series connected to form a stack of cells which provides voltage generating capabilities in the converter. As the voltage of each cell is typically capable of projecting a small voltage compared to the total maximum stack voltage, very smooth voltage waveforms can be generated this way. Each stack can thus be thought of as a controlled voltage source.

Most HVDC schemes built to date are point-to-point schemes. The converters at the terminals are typically rated at the full power capacity of the link. En-route connections from the link to local loads or generators are not necessarily rated at the full link power. Such partial power connections are referred to as HVDC taps and are typically rated at 1-10 % of the link's capacity [8]. This paper presents four architectures of DC/DC converters for use in HVDC VSC taps.

The HVDC Tap

A tap provides the interface between the DC link and a local AC network. As the tap is commonly considered for lower than link capacity power rated applications, the AC network it connects to is typically a medium to low voltage one. As a HVDC transmission line is typically operated at very high voltages such as $\pm 320\text{kV}$ and a local AC network may have a voltage rating of 50 kV, the tap has to provide a significant voltage step.

Taps can be split into either series or parallel connected arrangements [8-9]. Series taps are directly integrated into the line and therefore have to be able to withstand the full current rating of the line. Although the voltage potential across the converter is relatively small compared to the line voltage, it will have to be insulated to the full voltage rating. In a series tap design such as discussed in [9-10] this causes some component to require a large DC insulation, in this case the transformer.

For the purpose of this paper we focus on parallel connected taps. Such taps, as discussed in [11-14], have to be able to withstand the full line voltage but only handle a small fraction of the line current rating. Fig. 1 shows two possible parallel tap topologies. A more traditional design is shown on the left using a conventional fully voltage rated, three-phase DC/AC converter followed by a three-phase transformer (or three single-phase transformers depending on power rating). The alternative to such an arrangement is shown on the right, where a DC/DC converter provides the voltage step and the DC/AC conversion is done at a much lower voltage. Depending on the design of the DC/DC converter such an arrangement may be beneficial as the DC/DC converter is not necessarily a three-phase arrangement and the DC/AC converter is rated to a much lower voltage.

Fig. 1: Parallel tap topologies using a conventional DC/AC converter followed by a transformer (left) and an alternative design with a DC/DC converter followed by a DC/AC converter (right).

DC/DC converters for HVDC applications is an area of increasing interest. A design using a front-to-front arrangement suitable for high power ratings and low transformation-ratios can be found in [15]. Alternatives with larger transformation-ratios are discussed in [16-17] and some thoughts on DC converters using cells can be found in [18]. This paper introduces four alternative DC/DC architectures utilising cell stacks. All architectures discussed are for synchronous monopole arrangements.

Direct Conversion DC/DC Architectures

Since the stacks of a modular multilevel converter can be thought of as controlled voltage sources, they can be used to provide a DC step. Two architectures will be introduced for conversion between two different DC voltages without the use of any magnetic coupling components.

Parallel Output Pole Architecture

This Parallel Output Pole architecture can be thought of as a DC version of the MMC. Each terminal of the lower DC voltage side (V_{d2}) is connected to the midpoint of a phase leg consisting of two stacks of cells as

shown in Fig. 2. The arm inductors $L_{a,b}^{+,-}$ are used to set the rate of change of the stack currents $I_{a,b}^{+,-}$ which are controlled by the cell stacks.

The DC voltages and currents are related to each other through the converter transformation-ratio (κ_v) as per (1) and (2) such that V_{d2} is the lower voltage. The transformation-ratio is defined in (3).

$$V_{d2} = \kappa_v V_{d1} \quad (1)$$

$$I_{d2} = \frac{I_{d1}}{\kappa_v} \quad (2)$$

$$\kappa_v = (0,1] \quad (3)$$

The DC currents (I_{d1} and I_{d2}) split equally across both phase legs such that the arm currents can be described as in (4) and (5). From these equations it can be seen that the currents of the opposing stacks are symmetrical between the two phases.

$$I_a^+ = \frac{I_{d1}}{2} - \frac{I_{d2}}{2} = \frac{I_{d1}}{2} \left(1 - \frac{1}{\kappa_v}\right) = I_b^- \quad (4)$$

$$I_a^- = \frac{I_{d1}}{2} + \frac{I_{d2}}{2} = \frac{I_{d1}}{2} \left(1 + \frac{1}{\kappa_v}\right) = I_b^+ \quad (5)$$

The cell stacks not only control the currents through the converter but also generate the required voltages to interconnect the different DC terminals. The required voltage capabilities are described in (6) and (7). The same kind of symmetry as for the stack currents (4) and (5) is also observed.

$$V_a^+ = \frac{V_{d1}}{2} - \frac{V_{d2}}{2} = \frac{V_{d1}}{2} (1 - \kappa_v) = V_b^- \quad (6)$$

$$V_a^- = \frac{V_{d1}}{2} + \frac{V_{d2}}{2} = \frac{V_{d1}}{2} (1 + \kappa_v) = V_b^+ \quad (7)$$

Fig. 2: Circuit diagram of parallel output pole, direct conversion DC/DC converter.

Series Output Pole Architecture

The series output pole architecture consists of two phase legs connected in series with each other. The midpoint of each phase leg connects to a lower DC voltage terminal. A circuit diagram is shown in Fig. 2.

The input/output relations described in (1) and (2) remain true. The current through the cell stacks are described in (8) and (9).

$$I_o^+ = I_{d1} = I_o^- \quad (8)$$

$$\begin{aligned} I_i^+ &= I_{d1} - I_{d2} = I_{d1} \left(1 - \frac{1}{\kappa_v}\right) \\ &= I_i^- \end{aligned} \quad (9)$$

The voltage capability requirements of the stacks is described in (10) and (11).

$$\begin{aligned} V_o^+ &= \frac{V_{d1}}{2} - \frac{V_{d2}}{2} = \frac{V_{d1}}{2} (1 - \kappa_v) \\ &= V_o^- \end{aligned} \quad (10)$$

$$\begin{aligned} V_i^+ &= \frac{V_{d2}}{2} = \frac{\delta V_{d1}}{2} \\ &= V_i^- \end{aligned} \quad (11)$$

Fig. 3: Circuit diagram of series output pole, direct conversion DC/DC converter.

Energy balancing for direct conversion DC/DC architectures

As for all modular-multilevel converters, the energy in the cells' capacitors has to be maintained throughout the operation. Considering only the DC currents and voltages required to interconnect two DC links with each, the cell stacks in the direct conversion architectures all suffer from energy drift. This means that the stacks will either completely discharge or overcharge with time during normal operation. To counteract this energy drift additional AC balancing currents and voltages have to be incorporated into the operation of the converters.

One option to achieve this is by generating a square-wave voltage at the points where the HV2 terminals are connected to the converters. As long as these square-waves are in phase with each other the voltage across the

HV2 terminals will remain constant. To exchange energy between the stacks, a square-wave current is controlled to flow through the stacks without entering either DC link. The principle of operation of this balancing mechanism is illustrated in Fig. 4. From it the main difference in the voltages generated by the stacks can be noted.

Whilst the voltage across the HV2 terminals remains unchanged, its terminal-to-ground voltages will vary. To reduce this voltage fluctuation, the magnitude of the balancing voltage ($\hat{V}_e$) can be chosen to be relatively small, such as the voltage equivalent of one cell.

Fig. 4: Operating principle of the AC energy balancing voltages and currents for (a) parallel pole and (b) series pole direct conversion DC/DC circuits.

DC/DC architectures with intermediate AC step and galvanic isolation

Rather than providing a direct DC to DC voltage conversion, an intermediate AC step can be introduced. By using square-waves for the AC link a single-phase arrangement can be used and maintain constant power throughput. A rectifier on the HV2 side with little filtering can convert the AC waveform back to DC. Furthermore a transformer can be used to interconnect the cell stacks and the rectifier, providing galvanic isolation to the converter.

The overall transformation-ratio in these circuit topologies can be split into two components. On the one hand the cell stacks can provide a certain voltage step by generating the AC waveform with a magnitude less than that of the HV1 DC link. On the other the transformer can be used to provide a further step.

DC/AC/DC architecture with shunt connected primary

The first DC/AC/DC presented consists of a single phase leg with the transformer's primary connected between its midpoint and the midpoint of the split HV1 DC link capacitors. A circuit diagram is shown in Fig. 5. The square-wave voltage and current applied at the primary are defined in (12) and (13).

$$V_p(t) = \hat{V}_p \cdot \text{sqw}\left(\frac{t}{T_0}\right) \quad (12)$$

$$I_p(t) = \hat{I}_p \cdot \text{sqw}\left(\frac{t}{T_0}\right) \quad (13)$$

$$\text{sqw}\left(\frac{t}{T_0}\right) = \begin{cases} 1 & \text{if } 0 \leq t < \frac{T_0}{2} \\ -1 & \text{if } \frac{T_0}{2} \leq t < T_0 \end{cases} \quad (14)$$

The primary voltage and current magnitudes can be defined as shown in (15) and (16), linking them to the HV1 side through the stacks' transformation-ratio (κ_s). Similarly the transformation-ratio across the transformer (κ_t)

can be used to define the secondary and primary sides, as in (17) and (18). Finally the HV1 and HV2 sides can be expressed in terms of each other using both transformation-ratios as per (19) and (20).

$$\hat{V}_p = \kappa_s V_{d1} \quad (15)$$

$$\hat{I}_p = \frac{I_{d1}}{\delta_s} \quad (16)$$

$$\hat{V}_s = \kappa_t \hat{V}_p \quad (17)$$

$$\hat{I}_s = \frac{\hat{I}_p}{\kappa_t} \quad (18)$$

$$V_{d2} = \hat{V}_s = \kappa_s \kappa_t V_{d1} \quad (19)$$

$$I_{d2} = \hat{I}_s = \frac{I_{d1}}{\kappa_s \kappa_t} \quad (20)$$

Fig. 5: Circuit diagram of DC/DC architecture with intermediate AC transformation and shunt connected primary.

Each cell stack carries half of the primary current and the HV1 DC current as described in (21) and (22).

$$I_t(t) = I_{d1} + \frac{I_p(t)}{2} \quad (21)$$

$$I_b(t) = I_{d1} - \frac{I_p(t)}{2} \quad (22)$$

The stacks' voltage profile is shown in (23) and (24).

$$V_t(t) = \frac{V_{d1}}{2} - V_p(t) \quad (23)$$

$$V_b(t) = \frac{V_{d1}}{2} + V_p(t) \quad (24)$$

DC/AC/DC architecture with series connected primary

The last architecture is a variation on the shunt connected primary DC/AC/DC architecture as shown in Fig. 6. It also consists of two cell stacks which apply a square-wave across the transformer. The primary is however connected between the two stacks and is therefore left completely floating. The transformer equations are the same as for the previous architecture, thus the equations (12) to (20) still hold true.

Each cell stack now experiences the same current, consisting of the full primary AC as well as the HV1 DC current, as described in (25).

$$I_{t,b}(t) = I_{d1} + I_p(t) \quad (25)$$

The stacks have to generate voltages as shown in (26).

$$\begin{aligned} V_t(t) &= \frac{V_{d1}}{2} - \frac{V_p(t)}{2} \\ &= V_b(t) \end{aligned} \quad (26)$$

Fig. 6: Circuit diagram of DC/DC architecture with intermediate AC transformation and series connected primary.

Cell energy balancing in DC/AC/DC architectures

As both DC/AC/DC architectures have to generate AC voltages and currents during normal operation, their stacks do not in fact suffer from energy drift, provided that the relation between the HV1 DC and primary current, see (16), is satisfied. Under normal operation the energy of each stack is the same. Due to transient events a difference in energy level may develop which requires rebalancing. Such a stack-to-stack energy rebalancing mechanism can be implemented by modulating how the AC currents are split between the top and bottom stack for the shunt connected primary architecture. For the series connected primary DC/AC/DC, a DC voltage offset can be added to the stack voltages. Provided that an equal and opposite voltage is applied to the top and bottom stacks, the voltage across the primary remains unchanged. Since such energy imbalances tend to be relatively small, a single cell's worth of voltage can be used to provide these offsets.

Semiconductor effort and discussion

Each cell stack has to be rated for a peak voltage and maximum current which can be used to calculate the stack's apparent power rating, as defined by (27). It is arguable whether peak, average or RMS current should be used depending on the thermal limits and commutation limits of the device. Here, peak current will be used as representative of the current rating. The ratio of the sum of all the cell stacks' apparent power ratings (called S_Σ) to the power throughput is a measure of the power rating of the cells that needs to be installed per Watt of power to be transferred between the DC links. It is defined by (28) and known here as the power capacity ratio. The power capacity ratio normalises converter ratings and can therefore be used to compare converter architectures against each other and indicate the relative cost of them. This measure is independent of the number of cell stacks, phase legs and general converter structure as it takes into account all the cell stacks of a converter and normalises their installed power capacity with respect to P_1 .

$$S_{stack} = |\hat{V}_{stack}| |\hat{I}_{stack}| \quad (27)$$

$$\lambda_P = \frac{S_\Sigma}{P_1}, \quad : P_1 = V_{d1} I_{d1} \quad (28)$$

Earlier it was shown that the currents and voltages of the stacks are a function of the transformation-ratio that the stacks apply. Therefore the power capacity utilisation also varies with transformation-ratio, as illustrated in Fig. 7. The results shown take the energy balancing requirements of the direct conversion architectures into account and assume that the AC balancing current has the same magnitude as I_{d1} . The value of λ_P for two well-studied modular VSCs can be calculated in a similar manner. A front-to-front (F2F) connection of sine-wave inverters, such as discussed in [15], requires two such converters and can therefore be used as a DC/DC alternative indicator, as illustrated in the diagrams.

The direct conversion architectures can be seen to suffer from particularly high power capacity ratios at high transformation-ratios ($\kappa_v \rightarrow 0$). First, this is due to the fact that as the transformation-ratio is increased, the stacks have to generate larger voltages. At the same time the currents flowing through them increase to maintain power parity. Secondly, as the currents through the stacks increase, so does their energy balancing current magnitude. At lower transformation-ratios these effects are less prominent and consequently for $\kappa_v \geq 0.5$, the series pole DC/DC architecture in particular, performs better and in fact has the lowest power capacity ratio of all converters considered. This makes the direct conversion architectures particularly suitable for applications to interconnect legacy HVDC links which have similar but different nominal voltages.

Fig. 7: Power capacity ratio for direct conversion DC/DC, see a), and for DC/AC/DC converters, see b), with references for MMC and AAC equivalent power capacity ratios. Results shown for a range of transformation-ratios applied by the cell stacks.

The converter architectures with an intermediate stage both have a minimum power capacity ratio of 4. Since the transformer in these architectures can also contribute to the overall transformation-ratio, they could be

operated at the voltage ratio κ_s which minimises the power capacity ratio. The DC/AC/DC architectures therefore lend themselves to applications with high transformation-ratios, such as HVDC taps.

In the diagrams in Fig. 7, the power capacity ratios for the F2F arrangements are also illustrated for reference. It can be noted that they suffer a higher λ_p than all four architectures for most transformation-ratios. This implies that they appear to have the worst semiconductor utilisation of all the DC/DC conversion mechanisms considered here.

In part this is because they utilise sinusoidal wave-forms which have a worse peak-to-RMS ratio than square-waves do. Also they essentially utilise two series connected converters utilising stacks of cells which provides them with the added advantage of bi-directional power flow. If the passive rectifier in the DC/AC/DC architecture, as shown here, were to be replaced by an active one, to allow for bi-directional power transfer, the architectures' overall power capacity ratio would increase by four points as each switch would have an apparent power rating equivalent to P_1 . This would still allow them an advantage in terms of installed power capacity compared to the F2F architectures.

The power capacity of the cell stacks is not the only concern in a system design and this study should be extended to consider the volume of the passive components required (principally the cell capacitors but also the high frequency transformers and limb reactors) and the power losses.

The transformer in the DC/AC/DC architectures is a significant component in terms of volume and power losses. Transmission transformers for 50 Hz operation are large and heavy devices. The AC link in the presented circuits however is fully internal to the converter and therefore not restricted to operate at any particular frequency. By raising this frequency the transformer core can be made smaller as the peak flux is inversely proportional to frequency and so the cross-sectional area can be reduce. Increasing frequency will increase hysteresis and eddy current losses per unit volume in the core and therefore a trade-off could be found which balances volume reduction with loss increases. On top of reducing the size of the transformer, the benefits of a higher AC frequency also extend to the size of the cell capacitors as was also found to be the case for the front-to-front architecture [15]. These are typically designed to tolerate a certain voltage deviation caused by the AC currents flowing through them. By increasing the frequency the voltage deviation caused is reduced allowing for smaller capacitor to be used. Again though, this will need to be weighed up against an increase in switching losses in the semiconductors.

The direct conversion DC/DC circuits utilise half-bridge cells and are therefore susceptible to faults on the HV1 side. As the stacks do not possess any reverse polarity voltage capabilities, the HV2 terminals would be shorted to the faulting HV1 terminals through the anti-parallel diodes in the cells, leading to uncontrolled fault currents. As the DC/AC/DC circuits have an internal AC link as well as galvanic isolation they can provide full fault propagation prevention services in case of DC faults in either link.

Conclusion

Both direct and transformer-coupled architectures of modular DC/DC converters for HVDC use have been studied. The basic operation of two variants of each architecture has been analysed and they have been compared to each other and to the so-called front-to-front DC/AC converter connection. The comparison is in terms of voltage and current requirements of the stacks which was calculated in terms of a power capacity ratio (the ratio of apparent power rating of the stacks of cells to the power throughput). The power capacity ratio serves as an approximate indicator of the normalised capital cost of the converters.

The direct conversion architecture uses cell stacks to generate the required voltage difference between the DC voltages. The cell stacks have to provide the full DC step as a result. These circuits suffer from an energy drift and require an internal AC rebalancing current to be circulated. This adds to the current and voltage ratings of the stacks and so these architectures have a high (i.e., poor) power capacity factor which gets worse as the ratio between the DC voltages (the transformation ratio) increases. However, for transformation-ratios of 2:1 and lower they perform particularly well. This means that they are not suited to interfacing small amounts of power to a large HDC link (such as tapping in a small wind farm) but would be suitable for connecting to HVDC links of similar but different nominal voltages.

The transformer-coupled DC/DC architecture with an intermediate square-wave AC stage was also presented. The transformer and the stacks of cells each have a role in the overall transformation-ratio. This flexibility allows some optimisation of the architecture's apparent power rating thus achieving a lower (i.e., better) power capacity factor than the direct conversion architecture. The AC frequency can also be optimised to achieve the most suitable trade-off between transformer size and switching losses.

Compared to front-to-front DC/AC converter connections using conventional VSCs, which have been suggested in the literature as an alternative DC/AC/DC conversion process, the architectures presented here have a significantly lower power capacity ratio. Presently there are no indications that these architectures could not also be scaled up to full link power levels. This means they could also be considered for other HVDC applications.

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