Lab-scale Experimental Multilevel Modular HVDC Converter with Temperature Controlled Cells

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<<Converter Circuit>>, <<Converter Control>>, <<Multilevel Converters>>, <<High Voltage Power Converters>>, <<Multi-terminal HVDC>>, <<HVDC>>, <<Voltage Source Inverters>>

Abstract

It is important to be able to produce representative experimental results when researching HVDC grids and converters. This paper reports on a lab-scale multi-level converter build. The converter was built with a large number of cells to enable experiments with cell balancing effects and with temperature control to investigate thermal effects and appropriate responses. The converter is able to behave as both a traditional MMC (or CTLC which is functionally similar) and as the newer AAC converter. Results are presented that show the converter is able to charge up from the DC bus and is able to function well with both static and changing power references.

Introduction

The area of High Voltage DC (HVDC) transmission is receiving a large amount of academic and industrial research interest. Most of the research into HVDC converters and links/grids is performed using simulation models as these are very complicated systems. However, it is still important to be able to verify these results using lab hardware as much as possible. This paper outlines the build and test of a lab-scale HVDC converter suitable to verify simulation results. The converter was designed to be a significantly scaled down version of an HVDC converter whilst still maintaining as realistic dynamics as possible.

HVDC Converters

Many of the large power electronic companies now produce voltage source HVDC converters (VSC-HVDC) [1, 2, 3]. Early models were built as variations of the standard 2-level inverter. Due to the difficulty manufacturing high voltage devices and complicated gate drive considerations this type of converter is very difficult to build at HVDC scale and the requirement for PWM means high losses. Whilst VSC-HVDC converters have advantages in controllability over the established current source designs the 2 level style converters could not compete on power rating or efficiency, this has led to a requirement for a new high efficiency design.

Modular Multilevel Converter

Siemens popularised the multi-level VSC-HVDC converter design with the introduction of the Modular Multilevel Converter (MMC) [4]. This design uses a large number of capacitor cells to build the output voltage in a series of small steps. Due to the high number of steps there is very little harmonic noise in the output. This removes the requirement for AC side filtering that is often required with PWM converters. This significantly increases the efficiency of the converter. The switching frequency of the individual semiconductor devices is much reduced due to not needing PWM, resulting in much lower losses.

The MMC cell contains 2 IGBT switches and a capacitor allowing it to produce output voltages of $0V$ or V_{cell} . These cells are arranged into 6 arms; 2 per phase. A single phase of an MMC is shown in Figure 1(a). Each arm is connected to one of the DC rails and the AC connection point. The arms must be able to produce the full AC voltage magnitude from the DC rails using the two available output voltages, so the AC voltage peak must be lower than the DC rail voltage. The application of third harmonic injection can enable MMC converters to work with a higher AC voltage. The sum of the cell voltages in an arm must be equal to or greater than the DC voltage. All 6 arms are in conduction at all times. Each pair of arms carries $1/2$ of the AC current and $1/3$ of the DC current. This results in a smooth DC-side current, removing the need for lossy DC side filtering. The cells are kept charged to the correct level by controlling a DC current to flow through the converter. The requirement for the AC voltage peak to be below the DC voltage means that the MMC is not able to continue function during DC faults. The IGBT diodes are forced into conduction during a DC fault and an uncontrolled current will flow.

Alternate Arm Converter

Alstom Grid have recently published the design of another alternative circuit layout for a multilevel converter. The Alternate Arm Converter (AAC) [2] alternates conduction between the two arms in a phase. This is achieved by having a pair of series IGBT valves to direct the current between the upper and lower arms on each phase. The current in the outgoing arm is controlled to zero before the director is operated, allowing for a simpler IGBT valve design. The converter is effectively a hybrid of a slow switching 2-level converter (the director switches switch at only 50 Hz) and a multilevel converter. As each arm is only required to conduct half of the cycle, they don't need to be able to support the full voltage. This allows the converter to work with a reduced number of cells compared to an MMC. Figure 1(b) shows the circuit layout of a single phase of an AAC.

As there is no longer a continuous conduction path for DC current the issue of balancing the cells becomes more difficult and a short period of arm overlap is required to allow a DC balancing current. The operation of the converter as described in [5] exhibits a sweet-spot ratio between the AC and DC voltages where minimum balancing effort is required. At this ratio the AC voltage is higher than the DC voltage by 27%. This means that the AAC cannot use half-bridge cells like the MMC. The full bridge cells used in the AAC allow the arm to produce voltages higher than the DC rail voltage as they can output $-V_{cell}$ in addition to $0V$ and V_{cell} . This also has the added benefit of allowing the converter to block DC faults as it can operate when the AC voltage is larger than the DC voltage. The inductance arrangement of the AAC is different to the MMC due to the different current control requirements. The main inductance is now found in the AC phase shared by the two arms and each arm only has a small inductance to help control currents during overlap.

Figure 1: Diagram showing a single phase of an MMC (a) and an AAC (b)

These converter designs, and others that behave similarly, such as the ABB CTLCL[1], are likely to play a big part in future HVDC systems and as such the lab scale converter should be able to represent them all.

Design Brief

It is desired that the converter is able to represent the converter types described above realistically but at low voltage and low power. In order to represent different converter types the lab converter will need to be reconfigurable to operate in 2 different setups: an MMC setup and an AAC setup. Changing between setups will require the addition of director switches, the rearrangement of the arm and phase inductors, and an increase in AC voltage for the AAC.

Cell Configuration

It is impractical to attempt to create a lab scale converter with the hundreds of cells found in a full scale converter. However, it is still important to have a large enough number of cells so that cell balancing issues are exhibited and control techniques can be verified. Additionally, for very low numbers of cells the AC current control is difficult due to the coarseness of AC voltage output. For this converter the number of cells per arm, N_c , was chosen to be 10 as this provides a good balance between presenting cell balancing issues and wiring complexity. This also means that the number of IOs for firing of semiconductors and measurement of cell voltages is kept manageable.

The converter is intended to represent the real behaviour of a converter with cells at approximately 1.5-2 kV and IGBTs that exhibit a voltage drop of around 2.5 V each. When scaled down it is not likely to be possible to keep the ratio of cell voltage to IGBT voltage drop. It is possible to acquire small IGBTs which exhibit a V_{ce} of approximately 1.7 V. To keep the ratio the cell voltage would need to be above 750 V and the DC voltage (for 10 cells and an MMC setup) of 7500 V. This voltage is too high to be considered 'lab-scale'. A cell voltage of approximately 150 V is high enough that the IGBT voltage drop should not affect the results significantly. This gives a DC voltage in the region of 150 V which is more appropriate for a lab. When using the system as an AAC and keeping the number of cells constant the cell voltage now falls to 106 V to represent the lower voltage capability of an AAC arm.

To enable the converter to act as both an AAC and an MMC the cells must be of the full-bridge configuration, they can later be partly disabled to act as half-bridges. The director switches for AAC operation will be built from larger IGBTs so that they do not require a large series valve arrangement.

Using the calculations presented in [6] we require a capacitance of around 440 μF to keep voltage variations within 10 % of nominal with the AAC. Variations will be larger in the MMC setup but if the capacitors and devices are rated to take the higher voltages this will not be an issue. Still, a value of 500 μF was chosen as a good compromise. The capacitors are placed on a daughter board separate to the cells so that different values can be used if an experiment needs this.

System Voltage and Power

Having chosen 150 V cells for the MMC setup and hence a DC voltage of 1500 V the AC voltage peak must be below 750 V. Thus the AC line to line voltage must be below 918 V. When representing an AAC it is desired that the DC voltage and number of cells remains the same. To run at the sweet spot the AC peak is 27 % higher than the DC voltage therefore, the AC voltage for the AAC setup is 1170 V.

Having selected appropriate voltages for the DC, AC and cells the DC current (or power) must be set to allow appropriate device choice. A DC current of 10 A (power of 15 kW DC) was chosen to allow the use of small TO220 and TO247 devices.

Passive Components

The AC side of the converter is supplied through a variable autotransformer and a delta-star transformer. The transformer provides a fixed ratio of 415 V:1170 V. This is suitable for the higher voltage AAC setup. Reducing the input voltage by 27 % using the variac is required for the MMC setup.

The phase inductance for the converter was chosen to be 0.1 pu (24 mH in our system). For the MMC setup this is split into two arm inductors of 12 mH. For the AAC setup these are placed in series to give a single 24 mH phase inductor. Arm inductors of 0.65 mH are added to provide the required arm reactance for an AAC.

In order to prevent DC current ripple affecting the DC voltage significantly (which might be an issue for the device supplying the DC side) a DC bus capacitor of 210 μF was used. This was implemented as 2 bus capacitors of 420 μF each to provide a midpoint on the DC side.

Control System

The controller for the converter was chosen to be an OpalRT simulator as it allows rapid changes in the control system using simulink block layouts and provides a large number of IO. The system needs at least 180 digital out signals for the IGBTs and at least 74 analogue in signals for measurements of the cell voltages, arm currents and AC and DC system voltages and currents. As the cell voltages can vary greatly with respect to ground all control signals and measurements returned to the OpalRT must be isolated. This is achieved using optical drive signals and isolated voltage and current transducers.

Ancillary Equipment

The converter has a DC and an AC contactor, the sensors for the AC and DC voltage are ‘outside’ the contactors so that the information is available to the controller before the contactor is closed. In addition to the main connection contactors, a DC side charging system is provided to allow the converter cells to be charged from the DC side. This consists of a pair of resistors in the DC conduction path that can be short circuited by a contactor when the cells are charged. These resistors prevent a large inrush current from damaging the devices.

Completed Specification

The key specifications for the converter are laid out in Table I.

Table I: Lab-scale Converter Specifications

Specification	Value (AAC/MMC)
DC Voltage	1500V
DC Current	10A
AC Voltage	1070/918V
Number of Cells	10
Cell Voltage	106/150V
Phase Inductor	24/0mH
Arm Inductor	0.65/12mH
DC Bus Capacitor	210uF
DC Charging Resistor	47 Ω

Build

As each component of the converter is completed, it must be tested. Each cell was tested to ensure correct switching action, as was a complete arm. The first opportunity to test the entire converter’s function as a whole with controller, cells and power transfer was when half of the cells were completed. This can be operated as as 5 cell per arm converter. The next section of the paper shows the test results for this 30 cell reduced voltage converter.

MMC Results

DC Charging

Before any tests on the functionality of the system can be performed the cell capacitors need to be charged to the correct voltage. When the DC contactor is closed all of the cells will naturally charge via the diodes on each IGBT. The cells will charge to $V_{Natural} = V_{DC}/N$ where V_{DC} is the pole voltage and N is the number of cells per arm. If this is not the desired voltage a DC charging algorithm is required to rotate the cells so that they charge to the correct voltage.

$$V_{Natural} = V_{DC}/N \quad (1)$$

$$V_{Charge} = V_{DC}/N_C \quad (2)$$

$$\overline{V_{Cell}} = \frac{\sum V_{Cell(i)}}{N} \quad (3)$$

$$N_H = \lceil \frac{V_{DC}}{V_T} \rceil \quad (4)$$

$$N_L = \lfloor \frac{V_{DC}}{V_T} \rfloor \quad (5)$$

Figure 2: Flowchart for the DC Charging Algorithm

The DC charging algorithm used is shown in figure 2. The converter must always have a whole number of cells in conduction in each arm, N_C , these will charge to V_{Charge} . If the target voltage, V_T , is not a whole divisor of the DC voltage then the converter will need to alternate between rounded up and rounded down value of V_{DC}/V_T , N_H and N_L . The algorithm checks if the average cell voltage $\overline{V_{Cell}}$ is above or below the target voltage V_T . If it is above, N_L cells are used and if it is below N_H are used. The average is checked and the cells rotated every millisecond to keep the cells charged to the correct voltage.

The cells in Figure 3 in this experiment charge from their 30V natural voltage to a target of 70 V. It can be seen that the DC charging resistor reduces the current inrush for the initial part of charging. At 0.4

Figure 3: DC start-up algorithm running on hardware

s the average cell voltage reaches approximately 90 % of the target voltage and the charging resistor is removed from the circuit. At this point the charging currents rise significantly for the last part of the charging, which happens at a much greater rate. The two plots on the right hand side show the charging algorithm holding the cell voltages around the target cell voltage by exchanging discharged cells for charged ones and rotating between the upper and lower cell number. As the charging resistor is not in circuit for this last part the charging currents are larger as each cell is rotated in and charges up to the appropriate voltage.

Low cell number operation and last cell PWM

As the converter is being tested with a reduced number of cells compared to the original design it is to be expected that the output current would not be well regulated. To counter this effect the converter was modified to use PWM on the last cell, thus providing finer output voltage control and thus better current regulation. This technique is used in other implementations of low cell number MMC style converters [7].

Figure 4: The effect of last cell PWM on the AC phase current

The effect of adding PWM at 2.5 kHz to the last cell is shown in Figure 4. The current regulation is clearly much improved by the addition. This technique is obviously not going to be used in full scale HVDC MMC style converters as the high switching rate would increase losses. However, when the number of cells is low, as in this prototype converter, the technique is useful. All results from here on in will use the last cell PWM technique.

Steady-state power transfer

A test where the converter is commanded to produce 1 pu power constantly is shown in Figure 5. The arm and phase currents are well controlled and low ripple, partly aided by the last cell PWM. This shows that controller is well tuned and running at a sufficiently high rate to maintain control. The cell voltages vary in the manner expected and predicted in [6]. The cell voltages remain well grouped which indicates the converter is stable and the energy controllers are working well. Finally the DC current is constant throughout as would be expected of an MMC. Some noise is present on the signal, mainly caused by the PWM and relatively low cell number.

Figure 5: Steady state power transfer with MMC configuration

Power reference change

A power reference change from 1 pu to -0.8 pu is shown in Figure 6. A full scale MMC would not be asked to perform such a large power change in a short time (outside of fault conditions) as this would likely disrupt any connected AC systems. The ramp rate is 10 pu/s.

Figure 6: Ramped power reversal with MMC configuration

During the ramped change the phase current, arm current and DC voltage all behave as expected. The average cell voltages for each arm however, diverge during the power reference change, one arm ends up overcharged and the other undercharged. As the cell energy deviation curves for the two power references are different (as described in [6]) the transfer between the two states causes the arm energies to be disturbed rather than return to their original state. The energy balancing controller is bringing the two arms back into energy parity but this will occur over a long period of time. Due to cooling issues we were unable to capture this with the prototype converter.

AAC Results

When converting from MMC mode to AAC mode, the most significant change to the circuit is the addition of the director switch. The inductor arrangement must also be changed. The design of this switch is covered in the next section. The DC startup charging mechanism is identical between the two converters so will not be covered again. The AAC circuit also uses last cell PWM to counter the low cell number.

Arm Director Switch Design

Under normal conditions the director switches of the AAC are soft-switched and so should experience minimal transient voltage overshoot during turn-offs. However for a lab scale experimental set-up it is desirable that the director switch design be flexible and robust enough to operate under hard-switching conditions. The director switch has been designed as a series pair of IGBTs driven by delay matched gate drivers each with an RC snubber circuit to absorb the energy from the arm inductors during a hard switch. The director switches have been tested under hard-switch conditions with full load current of 10 A through the arm inductor. The results are shown in Figure 7. The director switch shows good transient sharing of voltage between the devices and limited overshoot.

Figure 7: Director switch test output showing the current and voltage across the two IGBTs

Steady state power transfer

The AAC steady state power transfer test is shown in Figure 8. The AC phase current is smoother than that obtained with the MMC circuit as the AAC has more voltage output levels for the same number of cells. The arm currents however are vastly different from those seen in an MMC. It can be clearly seen that the arms are alternating correctly, each arm produces one half-cycle of the phase current. The short periods of overlap current produce relatively high instantaneous currents in order to balance the arms when there is no dedicated DC current path. These short pulses of high current are also present on the DC side current which means the AAC will require a relatively large DC bus capacitor. This is to be

expected. The cell voltages in the AAC are lower than those in the MMC. The target voltage for the converter was 45 V. It is clear that the average voltage for all the cells at their ‘static point’ is controlled well to the target. The variation of cell voltages is as predicted in [6].

Figure 8: Steady state power transfer with AAC configuration

Ramped power reversal

As with the MMC configuration the AAC converter is unable to change power output instantaneously. The power reversal does not change the arm voltages in such a clear manner when the converter is in an AAC configuration. This is due to the slow action of the balancing controller. In addition to the two arms diverging during the ramp, the whole energy balance of the converter is disturbed. This is largely due to the fact that as explained in [5] the different energy balancing controllers are interdependent. However, the converter has largely stabilised within a few seconds of the power ramp without showing distortion on the phase currents.

Figure 9: Ramped power reversal with AAC configuration

Conclusions and Future Work

The design and specification of a lab-scale multi-level HVDC converter has been described. The initial build progress and first experimental results have been presented, showing their correlation with the simulations presented in previous papers. Despite the fact that this prototype converter is half the scale of the final build the results are promising with regard to output current smoothness and cell behaviour. The converter has been shown working in both the MMC and AAC configurations at a range of power references. In the future the converter will be completed to original specifications with a full 60 cells and two further converters are being built to enable multi-terminal and point to point configurations. These systems will be tested under normal power transfer and faulted power transfer conditions.

References

- [1] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, and T. Jonsson, "VSC-HVDC Transmission with Cascaded Two-Level Converters," in *CIGRE*, 2010.
- [2] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, D. R. Critchley, and R. W. Crookes, "A new hybrid multi-level Voltage-Source Converter with DC fault blocking capability," in *AC and DC Power Transmission, 2010. ACDC. 9th IET International Conference on*, pp. 1–5, oct. 2010.
- [3] Siemens AG, "Siemens Website HVDC PLUS (VSC Technology): Details." <http://www.energy.siemens.com/us/en/power-transmission/hvdc/hvdc-plus/modular-multilevel-converter.htm>.
- [4] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, vol. 3, pp. 6 pp. Vol.3–, 2003.
- [5] M. Merlin, *Hybrid multi-level HVDC converter and Multi-Terminal DC networks*. PhD thesis, Department of Electrical and Electronic Engineering, Imperial College London, 2012.
- [6] M. M. C. Merlin and T. C. Green, "Cell capacitor sizing in multilevel converters: Cases of the mmc and aac," *IEEE Transactions on Power Electronics*, p. in press, 2013.
- [7] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Pulse width modulation scheme for the modular multilevel converter," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, pp. 1–10, Sept 2009.