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Single-electron effects in heavily doped polycrystalline silicon nanowires

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We have observed single-electron charging effects in heavily doped polycrystalline silicon nanowires at 4.2 K. Wires of approximately 20 nm by 30 nm active cross section were defined by electron-beam lithography and thermal oxidation in standard polycrystalline silicon material. We have measured a Coulomb staircase and periodic current oscillations with gate bias, attributed to localized carrier confinement resulting from a statistical variation in the intergrain tunnel barriers. A sharp change in the current oscillation period is seen and we speculate that it is due to electrostatic screening of the gate bias by grain boundary defect states. © 1998 American Institute of Physics. [S0003-6951(98)02534-0]

The single-electron transistor (SET) can be more compact, more power efficient and less vulnerable to random carrier fluctuations than classical complementary metal-oxide-semiconductor (CMOS) devices.^{1,2} SETs based on silicon are advantageous for incorporation into established CMOS fabrication lines, and devices have been reported in crystalline material, particularly silicon-on-insulator. These use either lithographically defined islands^{3,4} or multiple-tunnel junctions created by material/structural disorder effects.^{5,6} By contrast, polycrystalline silicon has been somewhat neglected for SET applications despite a greater flexibility of fabrication. Single-electron effects have been observed in devices using polysilicon,^{7,8} but these rely on interlayer tunnelling rather than intrinsic polysilicon properties. Strong Coulomb blockade has also been reported at room temperature in a discontinuous ultrathin film of recrystallized amorphous silicon.⁹ In this work, we demonstrate Coulomb blockade in the conduction of heavily doped polycrystalline silicon nanowires and discuss mechanisms which explain the characteristics. Since standard CMOS materials are used throughout our fabrication process, a simple SET/CMOS integration scheme is practicable.

The polycrystalline silicon material was prepared as follows. Amorphous silicon either 50 or 70 nm thick was deposited at 550 °C on 10-nm-thick gate-quality oxide, grown thermally on a standard lightly doped (*p* type, $5 \times 10^{14} \text{ cm}^{-3}$) silicon substrate. The amorphous silicon was heavily doped *n* type by phosphorous implantation ($3 \times 10^{15} \text{ cm}^{-2}$ at 20 kV) activated by annealing at 850 °C for 30 min. This forms polycrystalline material with a grain size of $\sim 20 \text{ nm}$, confirmed by scanning-electron microscopy. The room temperature resistivity of the material was $\sim 2.5 \times 10^{-3} \Omega \text{ cm}$. Wires were defined in poly-methyl-methacrylate electron-beam resist, and etched into the polycrystalline silicon using a $\text{CF}_4/\text{SiCl}_4$ reactive-ion plasma. Approximately 40 nm of oxide was subsequently grown in

O_2 at a nominal 1000 °C to passivate the chip surface and reduce the wire cross section. Figure 1 shows a scanning electron micrograph of a polysilicon wire before and after oxidation; following oxidation, the active wire cross section is approximately 20 nm by 30 nm, roughly comparable with the mean grain size. This implies that the wire is likely to consist of a near-one-dimensional chain of polysilicon grains, with only one or at most a few grains in any given cross section. The two side gates can be used to modulate the wire potential.

The drain-source current–voltage characteristics at 4.2 K of a wire of active width $\sim 20 \text{ nm}$ and thickness $\sim 30 \text{ nm}$ are plotted as a function of side-gate bias in Fig. 2. The substrate was grounded during the measurement. A clear, multiple-step Coulomb staircase is seen, modulated periodically as the side-gate bias varies from -0.5 to -1.26 V . The steps are periodic for positive drain-source bias, with a period $\Delta V \approx 43 \text{ mV}$. Assuming a dominant charging island, this implies that the sum of the island capacitances is equal to $e/2\Delta V = 1.86 \text{ aF}$. The staircase persists up to 30 K. The central gap in the device characteristics cannot be reduced to zero using the side-gate voltage. The drain-source current as a function of side-gate bias from the same device is shown in Fig. 3(a). The measurements were taken over a period of an hour and the small discrepancy in current magnitude between Figs. 2 and 3(a) is probably due to a change in the distribution of trapped charge along the wire. Strong, reproducible current oscillations are observed; from -1.5 to 0.5 V , the oscillation period is 230 mV, but this decreases sharply to 50 mV at higher bias. The effective gate-island capacitances ($C_g = e/\Delta V$) are 0.7 and 3.2 aF, respectively. The two distinct oscillation frequencies are independent of the drain-source bias. We have seen the period change in all devices which show Coulomb blockade, though the oscillation periods are device dependent. The rapid switching around zero side-gate bias can be explained by switching of an offset charge in close proximity to the dominant charging island and is not evident in all devices. Results from a device with 30 nm by

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FIG. 1. Scanning electron micrograph at 45° tilt of a nanowire SET in 50-nm-thick polysilicon (a) before and (b) after oxidation. The wire is 60 nm wide and 1 μm long prior to oxidation, with a wire-to-side-gate separation of 70 nm. Following oxidation, the active wire cross section is approximately 20 nm by 30 nm.

30 nm active cross section are shown for comparison in Fig. 3(b); the overall behavior is very similar, with a double period of ~ 5 and ~ 1 V. It is clear that single-electron charging effects dominate the device characteristics, though other phenomena add to the behavioral complexity.

The characteristics of the polysilicon wires can be modulated using the side-gate bias to a certain extent; however, it is not possible to create a large enhancement or depletion effect in the wire. This contrasts sharply with the behavior of similar single-crystal nanowires, in which linear conduction, Coulomb blockade and pinchoff can be seen in the same device as a function of gate bias.⁶ Furthermore, wider wires or those fabricated in 70-nm-thick polysilicon showed no clear single-electron effects. The differences in electrical behavior between polycrystalline and crystalline silicon wires

FIG. 2. Current-voltage characteristic at 4.2 K of a polysilicon wire with an active wire cross section of approximately 20 nm by 30 nm. Side-gate bias interval is 40 mV, offset by 0.4 nA per curve. Arrows indicate steps in the current-voltage staircase.

of nominally identical geometry suggest a strong influence from polysilicon grain boundaries, which will contain a high concentration of electrically active defect states, segregated dopants, and other impurities.^{10,11} Large numbers of carrier-trapping states pin the Fermi level even for high doping levels,¹² creating a potential barrier at the grain boundary. Pinning of the Fermi level strongly attenuates gate action in polysilicon films¹³ and the defect states provide an electrostatic screening mechanism. These effects are likely in our small-grained polysilicon, which has a large grain boundary area per unit volume and probably a high concentration of segregated dopants and intergrain oxygen.

At low temperature, tunnelling becomes an important carrier transport mechanism in polysilicon. Assuming mid-gap pinning and an activated dopant concentration $\sim 3\text{--}5 \times 10^{19} \text{ cm}^{-3}$, a classical grain-boundary depletion width of

FIG. 3. (a) Drain-source current at 4.2 K as a function of side-gate bias at a fixed drain-source voltage of 50 mV for the polysilicon wire of Fig. 2. (b) Drain-source current at 4.2 K as a function of side-gate bias at a fixed drain-source voltage of 1 mV from a second device with active cross section approximately 30 nm by 30 nm.

~4 to 5 nm is expected. However, the average number of dopants in a cube of side 5 nm is less than ten. Statistical variation in dopant distribution should therefore strongly influence the width of the grain-boundary potential barrier. In a two- or three-dimensional highly doped polysilicon film, strong potential barriers are shorted out by low-resistance pathways. In our near-one-dimensional wire the number of pathways is drastically reduced and the wire's resistance is dominated by isolated islands, which cause the single-electron effects we observe. The likelihood of observing Coulomb blockade characteristics should drop off sharply with increasing wire width or thickness, in agreement with our observations.

We now consider the double-period oscillations in Fig. 3, which implies that the effective gate-island capacitance changes by a factor of four to five times at a slight positive bias and is almost invariant at other biases. Given the large size and fixed value of gate-wire separation, such a capacitance change may arise from changes in the effective interaction areas of the gate and the island. A change in the effective island size might be produced by a change in the depletion width at the grain boundary, but this would cause a large change in the tunnel resistance and hence in the wire current, which is not seen. It is also possible that adjacent grains begin to contribute to the effective island size; however, it should be noted that a four- to five-times increase in the gate capacitance implies a correspondingly large change in the effective island area. We have also considered the possibility that an inversion layer is created in the silicon substrate. However, our lightly doped substrate freezes out at low temperature and it is unlikely that a sufficient potential drop could be established.

Alternatively, the period change may be caused by different levels of attenuation of the side-gate potential, due to a change in the electrostatic screening at the grain boundary states for positive and negative applied voltage. The effect of the side-gate bias on a charging island would be moderated by changes in the occupancy of the grain-boundary traps, and the oscillation period for a given side-gate bias should reflect this. The effectiveness of the screening is directly related to the density of grain-boundary states at the Fermi level. Since we observe a sharp reduction in the screening as the gate bias sweeps from negative to positive bias, this implies a corresponding step in the interface density of states at

the Fermi level near zero bias. The density of states relation at a grain boundary is not straightforwardly predictable,¹⁰ but experimental evidence exists for discrete electronic levels at silicon grain boundaries.¹⁴ In our system, in addition to a continuum of grain boundary traps in the band gap, there may be a narrow band of states associated with a high density of impurity species, possibly phosphorus or oxygen. If this band consists of donor states, which are electrically neutral when filled, then charge balance implies that the Fermi level is pinned near the top of these states. This creates a step in the density of states at the Fermi level near zero bias, which is consistent with our observations. It is possible to estimate a capacitance associated with the screening effect. The reduction in the effective gate-island capacitance from 3.2 aF at positive bias to 0.7 aF at negative bias implies the introduction of an additional screening capacitance of 0.9 aF in series with the 3.2 aF gate-island capacitance.

In conclusion, we have characterized the electrical properties of highly doped polysilicon nanowires at low temperature. Single-electron charging effects were observed and attributed to islands isolated by dopant-related fluctuations in intergrain tunnel barriers. A double period was seen in the drain-source current oscillations as a function of side-gate bias. We speculate that this may be explained by electrostatic screening effects caused by the grain-boundary defect states.

¹M. Amman, K. Mullen, and E. Ben-Jacob, *J. Appl. Phys.* **65**, 339 (1989).

²K. Nakazato, R. J. Blaikie, J. R. A. Cleaver, and H. Ahmed, *Electron. Lett.* **29**, 384 (1993).

³D. Ali and H. Ahmed, *Appl. Phys. Lett.* **64**, 2119 (1994).

⁴Y. Takahashi, H. Namatsu, K. Kurihawa, K. Iwadate, M. Nagase, and K. Murase, *IEEE Trans. Electron Devices* **43**, 1213 (1996).

⁵H. Ishikuro, T. Fujii, T. Saraya, G. Hashiguchi, T. Hiramoto, and T. Ikoma, *Appl. Phys. Lett.* **68**, 3585 (1996).

⁶R. A. Smith and H. Ahmed, *J. Appl. Phys.* **81**, 2699 (1997).

⁷A. Ohata, H. Niiyama, T. Shibata, K. Nakajima, and A. Toriumi, *Jpn. J. Appl. Phys., Part 1* **34**, 4485 (1995).

⁸A. Nakajima, T. Futatsugi, K. Kosemura, T. Fukano, and N. Yokoyama, *Appl. Phys. Lett.* **70**, 1742 (1997).

⁹K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, *Appl. Phys. Lett.* **67**, 828 (1995).

¹⁰C. R. M. Grovenor, *J. Phys. C* **18**, 4079 (1985).

¹¹J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, *J. Appl. Phys.* **53**, 1193 (1982).

¹²G. Baccarani, B. Riccò, and G. Spadini, *J. Appl. Phys.* **49**, 5565 (1978).

¹³J.-P. Colinge, H. Morel, and J.-P. Chante, *IEEE Trans. Electron Devices* **ED-30**, 197 (1983).

¹⁴P. C. Srivastava, J. C. Bourgoin, F. Rabajo, and J. Mimila Arroyo, *J. Appl. Phys.* **53**, 8633 (1982).