Electrical and structural properties of solid phase crystallized polycrystalline silicon and their correlation to single-electron effects

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Single-electron transistors have been fabricated in solid phase crystallized polycrystalline silicon films deposited on SiO₂ layers grown on silicon substrates. The single-electron transistors consist of lateral side-gated nanowires. A Coulomb staircase is observed at 4.2 K, which is fully modulated by the side-gate voltage. Two-period conductance oscillations are observed in nanowires fabricated on 10-nm-thick buried oxide layers, while single-period oscillations are observed in nanowires fabricated on 40-nm-thick buried oxide layers. The two-period oscillations are attributed to the formation of a charge layer in the silicon substrate. The single-electron effects are also studied as a function of the nanowire dimensions and annealing or oxidation treatments. The effects are correlated to the structure of the polysilicon film, characterized using transmission electron microscopy, Raman spectroscopy, and electron spin resonance analysis. These measurements demonstrate the significance of single-electron charging effects on electron transport in nanometer-scale complementary metal-oxide semiconductor systems. © 2001 American Institute of Physics. [DOI: 10.1063/1.1331338]

I. INTRODUCTION

The reduction in the size of electronic devices for large scale integration may ultimately approach a limit where the presence or absence of a single electron determines the “on” and “off” states in the devices. A device which can operate at this limit is the single-electron transistor (SET), where it is possible to control the exact number of charging electrons on a nanoscale “island” isolated by tunnel barriers. The SET possesses the advantages of lower power consumption, better immunity from statistical charge fluctuation, and better scalability compared to conventional complementary metal-oxide-semiconductor (CMOS) devices.¹ The charging islands in the SET may be formed artificially by high resolution lithographic techniques² or “naturally,” where the islands are grown or deposited onto a substrate. One example of a material containing naturally formed islands is a polysilicon thin film consisting of nanoscale crystalline silicon grains. This material may contain islands of smaller and better controlled sizes compared to lithographically fabricated islands, e.g., Dutta *et al.*³ have deposited 8 nm ± 1 nm polysilicon islands.

Polysilicon may be deposited as amorphous silicon and then recrystallized by laser or electron-beam annealing, or by solid-phase crystallization.^{4–6} Alternatively, polysilicon may be directly deposited as grains.⁷ The structural characteristics of the polysilicon such as the grain size, defect state density, etc., depend on the specific deposition technique and directly influence the electrical characteristics. Recently, Ng *et al.*⁸ reported the observation of single-electron charging effects in electron-beam annealed recrystallized amorphous silicon nanowires. These effects were attributed to the trapping sites

found in the grain boundaries. Irvine *et al.*⁹ have performed a similar study on solid-phase crystallized polysilicon nanowires and have also observed single-electron charging effects. In addition, conduction in their nanowire devices could be controlled with lateral side gates and exhibited a double period in the single-electron conductance oscillations when measured as a function of gate bias.

In this paper, we report a detailed study of the electrical and structural characteristics of nanowires fabricated in solid-phase crystallized polysilicon thin films. Using a lateral side-gated nanowire SET structure, we have investigated the effect of varying the nanowire geometry, and the effect of thermal treatment of the nanowire in argon and oxygen atmospheres. We observe strong single-electron charging effects in these devices, where the Coulomb blockade region can be fully modulated by the side-gate voltage. We also show that oxidation effectively passivates the defect states in the polysilicon film. We have performed transmission electron microscopy (TEM), Raman spectroscopy, and electron spin resonance (ESR) analysis to characterize the structure of the grains and the grain boundaries in the polysilicon film, and we relate these observations to the electrical characteristics of the nanowires. We propose a model to explain the single-electron charging effects and the two-period conductance oscillations in the devices.

We note that the single-electron charging effects exist in nanowires fabricated in standard CMOS polysilicon material. This is of significance with respect to the ultimate scaling of CMOS devices. It is likely that with the scaling of the material thickness and the feature size of conventional CMOS devices deep into the nanometer regime, single-electron charging effects significantly influence electron transport in the devices. Our measurements explicitly demonstrate the

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FIG. 1. Scanning electron micrograph of the side-gate nanowire single-electron transistor fabricated in a solid-phase crystallized polysilicon film.

importance of single-electron charging effects in nanometer-scale CMOS systems.

II. EXPERIMENTAL METHOD

Our polysilicon material was prepared as follows: A 50-nm-thick amorphous silicon film was deposited at 550 °C by plasma enhanced chemical vapor deposition on a 10-nm-thick gate-quality silicon oxide layer grown on a crystalline silicon substrate (p doped, at $5 \times 10^{14} \text{ cm}^{-3}$). The amorphous silicon film was heavily doped to $5 \times 10^{19} \text{ cm}^{-3}$ using ion implantation of phosphorous at 20 kV and then crystallized into polysilicon using thermal annealing at 850 °C for 30 min. We believe that in this process, grain nucleation occurs primarily at the Si/SiO₂ interface.¹⁰ Thermal annealing also activates the dopants electrically. The sheet resistance of the material was measured to be 27 Ω/sq .

Lateral side-gated polysilicon nanowires of various geometry were defined in the polysilicon film using electron-beam lithography on polymethyl methacrylate resist and reactive ion etching in a 1:1 plasma of SiCl₄ and CF₄. Figure 1 shows a scanning electron micrograph of a device where the nanowire is 1 μm long and 40 nm wide. The side gate to nanowire separation is 120 nm. After the nanowires were defined, they were processed further using (1) thermal oxidation, (2) annealing, or (3) annealing followed by oxidation. Some devices were also fabricated without any of these thermal processes. Finally, aluminum was deposited to form ohmic contacts to the polysilicon film.

Our oxidation process was performed at 1000 °C for 15 min. This reduces the cross-sectional area of the nanowire and passivates the defect states on the surface and within the grain boundaries of the polysilicon film. We have determined the extent of oxidation in the nanowire by measuring the width of the nanowire prior to oxidation, after oxidation, and after removing the oxide layer using SILOX (Laporte proprietary chemical) wet etchant. The oxidation process removes ~ 10 nm in width of the polysilicon nanowire.

Our annealing process was performed in an argon atmosphere at 1000 °C for 15 min. This process modifies the de-

FIG. 2. Current-voltage characteristics of an oxidized nanowire fabricated on a 10-nm-thick buried oxide layer with varying side-gate voltage at 4.2 K. V_{ds} denotes drain-source voltage, V_{gs} denotes gate-source voltage, and I_{ds} denotes drain-source current.

fect state density at the grain boundaries, at the Si/SiO₂ interface, and along the reactive ion etched surfaces of the nanowire. The polysilicon grains also become larger, thereby increasing the crystalline volume fraction in the polysilicon layer.

We have fabricated oxidized nanowires with widths of 40 to 90 nm and lengths of 500 nm, 1 μm , and 1.5 μm . We have also fabricated annealed nanowires and annealed/oxidized nanowires of 1 μm length and 40–60 nm widths in order to characterize the dependence of the single-electron charging effects on defect density and grain size. To facilitate comparison of the thermally treated nanowires with thermally untreated nanowires, we have also fabricated thermally untreated nanowires of 1 μm length and 30–60 nm widths. Finally, to ascertain the effect of the substrate capacitance on the nanowire characteristics, we have fabricated oxidized nanowires of 1 μm length and 60 nm width on a 40-nm-thick (instead of a 10-nm-thick) gate quality buried oxide layer.

III. ELECTRICAL CHARACTERISTICS OF NANOWIRES

A. Two-period single-electron conductance oscillations in polysilicon nanowires

The drain-source electrical characteristics of an oxidized nanowire where the preoxidized width was 50 nm and length was 1.5 μm are shown in Fig. 2. These nanowires were fabricated on 10-nm-thick buried oxide substrates. Single-electron charging effects are observed as the drain-source voltage is swept from -0.04 to 0.04 V in 10 mV steps and the gate voltage is increased from -1.0 to 1.0 V in 10 mV steps. A zero-current Coulomb gap region is observed which oscillates in width with the gate bias, leading to trapezoidal shapes at the origin in the V_{ds} – V_{gs} plane. The period of oscillation changes abruptly at ~ 0.5 V, and a larger period is observed for negative gate bias. There is a corresponding

FIG. 3. (a) Two-period conductance oscillations at 4.2 K in I_{ds} in an oxidized nanowire of 1.5 μm length and 50 nm width, fabricated on a 10-nm-thick buried oxide layer. The oscillation transition point occurs at $V_{ds} \sim 0.5$ V. Details of line shape of conductance oscillations for (b) $V_{gs} < 0.5$ V and (c) $V_{gs} > 0.5$ V.

two-period oscillation in the drain-source current. Current steps are also visible in the I_{ds} - V_{ds} plane, which may be attributed to a Coulomb staircase.

Figure 3(a) shows the two-period oscillations in the drain-source current as the gate voltage is swept from -2 to 1 V for a series of drain-source voltages from -10 to 10 mV in steps of 2 mV. The larger oscillation period is ~ 500 mV while the smaller oscillation period is ~ 100 mV.

Similar two-period oscillations are observed whenever single-electron effects occur in oxidized polysilicon nanowires deposited on 10-nm-thick buried oxide substrates. Fig-

FIG. 4. Contours of constant I_{ds} at 4.2 K as a function of V_{gs} and V_{ds} in an oxidized nanowire fabricated on a 10-nm-thick buried oxide layer.

ures 3(b) and 3(c) show both the larger and smaller oscillation periods on a finer scale. We note that except for the period change, the line shape for $V_{gs} < 0.5$ V and $V_{gs} > 0.5$ V is the same and there exist finer peaks superimposed on each main peak in both regions of V_{gs} . The main peaks can be attributed to a dominant charging island, and the finer peaks can be attributed to an island with a smaller charging energy (i.e., larger sized) in series with the dominant island. The finer peaks suggest the presence of a multiple tunnel junction along the polysilicon nanowire.¹¹ The modulation of the Coulomb gap can also be seen in the constant-current contour plot of Fig. 4. The tilting of the trapezoidal Coulomb gap regions may be attributed to different values of the tunneling capacitances which isolate the dominant island.¹²

The temperature dependence of the oscillations in a 1- μm -long and 50-nm-wide oxidized nanowire is shown in Fig. 5. We observe that the oscillations become weaker as the temperature increases and at a temperature of 15 K, the Coulomb blockade effect is overcome and the oscillations disappear completely.

The voltage dependence of the oscillations in the same device is shown in Fig. 6. As the drain-source voltage increases from 1 to 30 mV, the oscillations become less distinct. There is a change in the gradient of the drain-source current/gate voltage characteristic at the same transition point where the change in oscillation period ($V_{gs} = 0.5$ V) occurs.

FIG. 5. Dependence of two-period oscillations on temperature. $V_{ds} = 1$ mV and the curves are offset by 0.5 nA per 1 K step.

FIG. 6. Dependence of two-period oscillations on V_{ds} at 4.2 K.

B. Effect of device dimensions on electrical characteristics

Table I summarizes the electrical results obtained from oxidized nanowires of length 0.5, 1, and 1.5 μm and width 50 and 60 nm. We also fabricated oxidized nanowires of 40 nm width but they did not conduct at 4.2 K. The oscillation periods in Table I are similar to those observed earlier by Irvine *et al.* and the oscillation transition point is ~ 0.5 V in all the devices. In addition, there was a relatively greater variation in the electrical characteristics of 0.5- μm -long nanowires. Some of these devices exhibited ohmic conduction, some did not conduct, while the three devices that exhibited single-electron effects were similar to the devices in Table I.

TABLE I. Conductance oscillation period and island to gate capacitance in various lengths and widths of nanowires. ΔV_{gl} is the larger oscillation period, ΔV_{gh} is the smaller oscillation period, and C_{gh} , C_{gl} refer to the corresponding island to gate capacitance.

Width (nm)	Length (μm)		
	0.5	1	1.5
50	$\Delta V_{gl}=200$ mV	$\Delta V_{gl}=300$ mV	$\Delta V_{gl}=500$ mV
	$C_{gl}=0.8$ aF	$C_{gl}=0.5$ aF	$C_{gl}=0.3$ aF
	$\Delta V_{gh}=50$ mV	$\Delta V_{gh}=70$ mV	$\Delta V_{gh}=100$ mV
	$C_{gh}=3.2$ aF	$C_{gh}=2.3$ aF	$C_{gh}=1.6$ aF
	$\Delta V_{gl}/\Delta V_{gh}=4$	$\Delta V_{gl}/\Delta V_{gh}=4.3$	$\Delta V_{gl}/\Delta V_{gh}=5$
60	$\Delta V_{gl}=100$ mV	$\Delta V_{gl}=200$ mV	$\Delta V_{gl}=300$ mV
	$C_{gl}=1.6$ aF	$C_{gl}=0.8$ aF	$C_{gl}=0.5$ aF
	$\Delta V_{gh}=20$ mV	$\Delta V_{gh}=40$ mV	$\Delta V_{gh}=80$ mV
	$C_{gh}=8.0$ aF	$C_{gh}=4.0$ aF	$C_{gh}=2.0$ aF
	$\Delta V_{gl}/\Delta V_{gh}=5$	$\Delta V_{gl}/\Delta V_{gh}=5$	$\Delta V_{gl}/\Delta V_{gh}=3.8$

Table I shows that both larger and smaller oscillation periods increase with nanowire length, e.g., the smaller oscillation period ΔV_{gh} in a 50-nm-wide nanowire increases from 50 mV for 0.5 μm length to 100 mV for 1.5 μm length. There is a corresponding decrease in the island to gate capacitance, $C_{gh}=e/\Delta V_{gh}$. Similar trends are observed for the 60-nm-wide nanowires. Table I also shows that the oscillation periods decrease when the nanowire width is increased from 50 to 60 nm. We also note that in all the devices the ratio of the large to small oscillation period $\Delta V_{gl}/\Delta V_{gh}$ is ~ 4 –5.

We have also fabricated 1 μm long oxidized nanowires of 70, 80, and 90 nm widths. Unlike the narrower nanowires, single-electron effects were not observed. It was found that these wider nanowires exhibited ohmic conduction, with resistances of 88, 42, and 34 k Ω , respectively.

C. Effect of thermal processing on electrical characteristics

Table II summarizes electrical results from oxidized, unoxidized, annealed, and annealed/oxidized nanowires of length 1 μm and width 40, 50, and 60 nm. We have also fabricated unoxidized nanowires of 30 nm width, but these devices did not conduct even at 300 K.

Neither the unoxidized nor the annealed nanowires show single-electron effects for 40, 50, and 60 nm widths. However, the nanowire resistance decreases with nanowire width (the nanowire height is unchanged) in both cases. The largest change in the nanowire resistance occurs when the nanowire width is increased from 40 to 50 nm. Annealing the nanowire increases the resistance twofold.

We observed two-period oscillations in annealed/oxidized nanowires, qualitatively similar to those observed in oxidized nanowires (see Sec. III B). However, these effects were observed in nanowires of narrower widths, i.e., 40 and 50 nm rather than 50 and 60 nm. The oscillation periods were also much shorter if the nanowires were annealed/oxidized, e.g., the smaller oscillation period in an oxidized 50-nm-wide nanowire reduces from 70 to 11 mV if the

TABLE II. Variation in nanowire characteristics with thermal treatment. The nanowire length was 1 μm and the measurements were taken at 4.2 K. ΔV_{gl} is the larger oscillation period, ΔV_{gh} is the smaller oscillation period and R is nanowire resistance.

Wire width (nm)	Oxidized	Unoxidized	Annealed	Annealed and oxidized
40	Nonconducting	Ohmic conduction $R = 93 \text{ k}\Omega$	Ohmic conduction $R = 214 \text{ k}\Omega$	Two period oscillations $\Delta V_{\text{gl}} = 50 \text{ mV}$ $\Delta V_{\text{gh}} = 10 \text{ mV}$
50	Two period oscillations $\Delta V_{\text{gl}} = 300 \text{ mV}$ $\Delta V_{\text{gh}} = 70 \text{ mV}$	Ohmic conduction $R = 43 \text{ k}\Omega$	Ohmic conduction $R = 84 \text{ k}\Omega$	Two period oscillations $\Delta V_{\text{gl}} = 60 \text{ mV}$ $\Delta V_{\text{gh}} = 11 \text{ mV}$
60	Two period oscillations $\Delta V_{\text{gl}} = 200 \text{ mV}$ $\Delta V_{\text{gh}} = 40 \text{ mV}$	Ohmic conduction $R = 36 \text{ k}\Omega$	Ohmic conduction $R = 83 \text{ k}\Omega$	Ohmic conduction $R = 48 \text{ k}\Omega$

nanowire is annealed prior to oxidation. In addition, the larger to smaller oscillation transition point shifts from ~ 0.5 to $\sim -0.2 \text{ V}$.

D. Effect of the 40-nm-thick buried oxide substrate on electrical characteristics

Figure 7 shows the gate oscillations in a 60-nm-wide and 1- μm -long oxidized nanowire fabricated on a 40-nm-thick buried oxide substrate. Measurements obtained from five other oxidized nanowires of the same dimensions exhibited similar electrical characteristics. In contrast to nanowires fabricated on 10-nm-thick buried oxide substrates (see Secs. III A–III C) there exists only one distinct oscillation period of 200 mV, instead of the two-period oscillations. We note that there exist finer peaks superimposed on the main oscillation peaks in a manner similar to Fig. 3. The oscillation period of 200 mV in Fig. 7 is similar to the larger period

observed in a 60-nm-wide and 1- μm -long oxidized nanowire fabricated on a 10-nm-thick buried oxide substrate (Table I).

IV. STRUCTURAL ANALYSIS OF THE POLYSILICON FILM

A. Electron spin resonance (ESR) analysis

ESR analysis¹³ of our polysilicon samples was performed at 300 K using a Bruker ER 200D spectrometer in the X wavelength range. As the polysilicon film in our samples was only 50 nm thick, the absorption spectra were taken over 50 accumulation sweeps, each with an accumulation time of 100 s. A magnetic field modulation of 5 G was applied with a gain of 4×10^5 .

Figure 8 shows the ESR first derivative of the absorption spectra obtained for the as-deposited polysilicon film, the annealed and oxidized film, the oxidized film, and the substrate. The spin density in these films, corresponding to the defect state density, was obtained by integrating the area under the absorption spectra and subtracting the integrated area for the substrate. For the as-deposited film, the spin density was $1.58 \times 10^{20} \text{ cm}^{-3}$ while for the annealed and oxidized film, the spin density was reduced to $6.6 \times 10^{19} \text{ cm}^{-3}$. Negligible spin density was detected in the oxidized film.

The Lande factor,¹⁴ $g = 2.0057 \pm 0.0005$, is the same for the as-deposited film and the annealed/oxidized film. The linewidth, $\Delta H = 8 \text{ G}$, is also the same for these films. The g value for silicon dangling bonds is 2.0049 to 2.0056,¹⁵ which compares well with our measured value, and the linewidth is $\sim 6.1\text{--}7.5 \text{ G}$, which is slightly smaller than our measured value. Due to the large field modulation used in our experiment, the linewidth is expected to broaden. We may conclude that silicon dangling bonds cause the signal observed in the ESR spectra.

We observe that the oxidation process passivates these dangling bonds effectively. However, when the film is annealed prior to oxidation, there remain a significant amount of defect states in the film, which are not completely passivated by the oxidation process.

FIG. 7. Conductance oscillations at 4.2 K in an oxidized nanowire fabricated on a 40-nm-thick buried oxide layer. V_{ds} is varied from 15 to 25 mV in steps of 1 mV.

FIG. 8. Electron spin resonance spectra of as-deposited, annealed/oxidized and oxidized polysilicon films. The spectra for the substrate is shown for comparison.

B. Transmission electron microscopy

TEM was performed using a Philips CM 300 FEG with an accelerating voltage of 300 kV. Figure 9 shows the dark field images before and after thermal treatments. A thermally untreated polysilicon film is shown in Fig. 9(a). The grains are irregular in shape and range from 5 to 50 nm in size. There is disorder structure and dislocations at the grain boundaries and also to some extent within the grains.

FIG. 9. TEM micrographs of (a) a thermally untreated polysilicon film, (b) an annealed film, (c) an oxidized film, and (d) an annealed and oxidized film.

In comparison to the thermally untreated film, the grains in the annealed polysilicon film are more columnar and uniform in size, with a mean diameter of 40 nm [Fig. 9(b)]. The smaller grains that are observed in the as-deposited polysilicon film are not apparent in the annealed polysilicon film. This may be due to the incorporation of smaller grains into larger grains. The dislocations observed in the as-deposited film have also disappeared.

An ~ 60 -nm-thick oxide layer is grown on the top surface of the polysilicon films in our oxidation process [Fig. 9(c)]. The thickness of the remaining polysilicon film is ~ 18 nm (~ 32 nm of polysilicon is consumed) and the thickness of the buried oxide remains at ~ 10 nm. The grains remain random in shape and the average grain size is ~ 18 nm. The grain boundary is about five atomic spacing in width and there are stacking faults at the grain boundaries induced by the oxidation process. There is also evidence of disorder at the grain boundaries which we associate with the formation of SiO_x .¹⁶

Finally, there is greater oxide growth in the annealed/oxidized film than in the oxidized film. The thermally grown top oxide is ~ 83 nm thick and the remaining polysilicon is ~ 14 nm thick [Fig. 9(d)]. The thickness of the buried oxide remains at ~ 10 nm. In this case a slightly greater amount of polysilicon (~ 36 nm) is consumed. The mean lateral grain size is comparable to that observed in the annealed polysilicon film but the mean vertical grain size is less than that in the oxidized polysilicon film. Only disorder structure is observed at the grain boundaries, which we associate with the formation of SiO_x .

C. Raman spectroscopy

The Raman spectroscopy was performed using a Renishaw Raman System 2000 microscope spectrometer. The excitation wavelength was 514.5 nm and the measurements were performed in a backscattering configuration at room temperature. The beam was collected through a $\times 50$ objective lens with a numerical aperture of 0.8. The beam diameter at focus is $\sim 1 \mu\text{m}$ on the sample surface. The power density was $\sim 0.01 \text{ W/cm}^2$ to avoid heating effects in the spectra.

Figure 10 shows the normalized Raman spectra of the as-deposited polysilicon film, oxidized film, annealed film, and the annealed/oxidized film. There exist strong peaks for all four types of films near 520 cm^{-1} . These peaks correspond to the transverse optical (TO) phonon mode of the crystalline silicon component of the polysilicon film.¹⁷ We note that in the as-deposited polysilicon film spectrum there exists a weak broad peak in the $490\text{--}505 \text{ cm}^{-1}$ range which is absent in the spectra of the other three thermally treated polysilicon films.

V. DISCUSSION OF RESULTS

A. Grains and grain boundaries

In Table II, for nanowires of the same width we observe that the annealed nanowires have a higher resistance than unoxidized nanowires. The ESR spectra of Fig. 8 indicates that annealing prior to oxidation decreases the passivating

FIG. 10. Raman spectra of as-deposited, annealed, oxidized, and annealed/oxidized polysilicon films. TO phonon peak position is seen to be shifted to larger wave numbers after the thermal treatments.

effect of the oxidation process in the polysilicon film. A significant amount of defect states remains in the annealed/oxidized film. It is also known that thermal annealing causes segregation of dopants to the grain boundaries and Si/SiO₂ interfaces.¹⁰ Therefore, the concentration of active dopants in the grains decreases and the electron scattering caused by the defect states increases. These effects cause an increase in the resistance of annealed nanowires. We observe that in the annealed/oxidized nanowires, the oscillation periods are smaller than in nanowires that were oxidized only. This may be attributed to a larger, lateral mean grain size in the annealed/oxidized film as compared to the oxidized film, which would imply a larger gate capacitance and a smaller gate oscillation period.

Figure 10 shows that the TO Raman peak of the four types of films do not coincide. The wave number of the TO peak corresponding to the as-deposited film (518 cm⁻¹) is slightly lower than the wave number of the peaks corresponding to the thermally treated polysilicon films (519–520 cm⁻¹). We can attribute this shift to a lower wave number to two possibilities: First, there may exist tensile strain in the as-deposited film and second, the grain size is smaller in the as-deposited film. The latter case is consistent with our observation of a relatively larger full width at half maximum (FWHM) of the TO peak in the as-deposited film.¹⁸

The broad peak at 490 cm⁻¹ of the as-deposited polysilicon film can be attributed to the transverse optical phonon mode of the amorphous silicon component of the polysilicon film.^{19,20} After thermal treatment this broad peak disappears. In the case of argon annealing, the formation of crystalline silicon grains from the amorphous silicon will reduce the intensity of this broad peak while oxidation will cause the formation of SiO_x, which will also reduce the intensity. As amorphous silicon (found in the grain boundaries) oxidizes more readily as compared to crystalline silicon we expect the formation of SiO_x to encapsulate the crystalline silicon grains.

The grain size as estimated from the FWHM of the TO peaks for the as-deposited film is ~8 nm while the grain size of the thermally treated polysilicon films is ~10 nm.²¹ From the TEM analysis, we observe that the mean grain size of the oxidized film is less than that of the as-deposited film. We can explain this discrepancy by attributing it to the larger amount of dislocation (which causes phonon scattering) observed in the as-deposited film [Fig. 9(a)] as compared to the oxidized films [Fig. 9(c)]. The larger the dislocation density the smaller the phonon correlation length and consequently, the smaller the spectral broadening.

B. Coulomb charging oscillations

The single-electron charging effects in our side-gated nanowire devices may be associated with charging islands formed by the polysilicon grains along the nanowires. These grains are isolated by the tunnel barriers created by SiO_x at the grain boundaries. However, not all grain boundaries may be associated with tunnel barriers, e.g., oxidation-induced stacking faults at grain boundaries [Fig. 9(c)] may not form good potential barriers. Hence, a charging island may contain more than one grain. We believe that the polysilicon grains form a one-dimensional chain of islands, creating a multiple tunnel junction (MTJ) device. Variation in the size of the grains implies that smaller peaks associated with larger grains are superimposed on the dominant peaks of the single-electron conductance oscillation (e.g., see Fig. 3). As the length of the nanowire decreases from 1.5 to 0.5 μm, the number of smaller peaks superimposed on each larger peak decreases from 5–4 for 1.5 μm length to 4–3 for 1 μm length to 2–1 for 0.5 μm length. This behavior may be associated with a decreasing number of tunnel junctions along the nanowires.¹¹

If the length L of an oxidized nanowire is increased, the gate capacitance C_g tends to decrease, and if the width W of the nanowire is increased, C_g tends to increase, i.e., $C_g \propto W/L$ (Table I). We explain this behavior by considering the effect of the nanowire dimensions on the polysilicon grains creating the MTJ. High resolution TEM analysis indicates that while the average grain size is ~20 nm, grains as small as ~5 nm may also exist in the polysilicon. Hence, the longer the nanowire, the higher the probability of smaller grains existing along the nanowire and the smaller the gate capacitance of the dominant island. The increase of C_g with W implies that an increase in the lateral area of the charging island increases the side-gate to island capacitance. Therefore, the electric field distribution between the side gates and the charging island must be considered in three dimensions and the increase in C_g is associated with fringing fields above and below the plane of the side gates and nanowire.

The total island capacitance may be estimated from the temperature at which the current oscillations disappear. The charging energy of the island can be related to the thermal energy by $e^2/2C_{eq} \approx 3kT$, where C_{eq} is the equivalent island capacitance.¹² Both the smaller and larger oscillation periods disappear at 15 K (Fig. 5). This implies that $C_{eq} \sim 2 \times 10^{-17}$ F.

C. Dopant enhanced oxidation

TEM measurements [Fig. 9(c)] of our polysilicon film demonstrate that the oxidation rate is anisotropic, and is greater along the height of the nanowire than along the width. This may be attributed to a dopant enhanced oxidation effect.¹⁰ Kimura *et al.*²² and Johannesssen *et al.*²³ have reported phosphorus dopant pile-up in thin polysilicon or crystalline layers at Si/SiO₂ interfaces on top of and under the silicon layer. The thickness of the pile-up layers reported by Kimura *et al.* was ~ 4 nm, and for a bulk doping concentration of $5 \times 10^{19} \text{ cm}^{-3}$, the pile-up region was even more heavily doped at $2 \times 10^{21} \text{ cm}^{-3}$. A larger doping concentration can increase the oxidation rate up to an order of magnitude.^{24,25} In our oxidized nanowires, polysilicon is consumed three times faster along the height of the nanowire than along the width. In annealed/oxidized polysilicon, additional dopants segregate at the grain boundaries and at the interfaces.²² This larger dopant segregation is caused by a greater number of defect states in the annealed/oxidized polysilicon, which further increases the pile-up region doping concentration and the corresponding oxidation rates. TEM measurements (Fig. 9) demonstrate that the top oxide layer thickness in the annealed/oxidized film is greater than that in the oxidized film by ~ 23 nm.

D. Model

We can construct a model for the two-period oscillations. Irvine *et al.* suggested three explanations for the two-period gate oscillations: the coupling of multiple islands, electrostatic screening by defect states, and the existence of an inversion layer in the silicon substrate. Figure 3(b) demonstrates that although the oscillation period changes as the gate voltage changes, the line shape remains the same for both negative and positive gate voltages. In addition, Fig. 5 shows that both periods of oscillation smear-out at 15 K. This implies that the same set of islands is responsible for the single-electron charging effects at both negative and positive gate voltages and the two-period effect is not due to the coupling of islands. In addition, ESR measurements indicate that an insignificant amount of defect states remain after oxidation (Fig. 8). It is therefore unlikely that the two-period effect occurs by means of a change in the screening associated with defect states existing at the grain boundaries or at the polysilicon/SiO₂ interfaces. Instead, we propose the explanation that the island capacitance changes due to the creation of an inversion layer in the crystalline Si substrate. Figure 7 shows that in a nanowire fabricated on a 40-nm-thick buried oxide layer, only a single period is observed in the conductance oscillations, which is similar to the period observed at negative gate voltages in a nanowire of the same dimensions but fabricated on a 10-nm-thick buried oxide layer (Table I). This suggests that the same gate capacitance exists in both cases. By comparison, in a nanowire fabricated on 10-nm-thick buried oxide, a positive side gate bias induces an inversion layer in the crystalline silicon at the buried oxide/substrate interface. This inversion layer lies under the side gates, and fringing fields can cause the inversion layer to extend into the gaps between the side gates and the

nanowire. The potential of this layer is proportional to the side-gate voltage, and the island to inversion layer capacitance contributes to the total island to gate capacitance, increasing the gating effect on the island and reducing the corresponding oscillation period. There is an associated increase in the transconductance of the device (Fig. 6). In nanowires fabricated on 40-nm-thick buried oxide, the island to inversion layer capacitance is likely to be less significant and the effective island to gate capacitance is only that associated with the two side gates.

When a negative side-gate voltage is applied, there is the possibility of the formation of an accumulation layer in the crystalline silicon at the buried oxide/substrate interface, which should contribute to the total gate capacitance in a manner similar to the inversion layer. However, our devices have ohmic contacts only to the heavily doped top polysilicon layer. The lightly doped *p*-type silicon substrate is connected to a metal ground contact but is unlikely to form an ohmic contact, especially at low temperature. A Schottky contact is more likely to be formed which is forward biased when a positive voltage is applied to the top polysilicon film. It is then possible to create an electric field across the buried oxide layer large enough to form an inversion layer at the buried oxide/substrate interface. If a negative voltage is applied to the top polysilicon film, the substrate-to-metal Schottky contact is reverse biased and it is not possible to create an accumulation layer at the substrate/buried oxide interface.

The threshold voltage for the creation of an inversion layer can change depending on any charges trapped near the silicon/oxide interfaces. We have discussed in Sec. VC the existence of a donor pile-up region in the polysilicon grains at the polysilicon/buried oxide interface. If a positive charge sheet²⁶ associated with this region exists in the grains, then it will alter the threshold voltage. In our oxidized nanowires, the transition point from the large period to the small period oscillation is ~ 0.5 V but in annealed/oxidized nanowires, the transition point is at approximately -0.2 V. We explain this effect in terms of an increase in the dopants that pile-up at the interface, increasing the positive charge at the interface. This would lower the threshold voltage from 0.5 to -0.2 V.

The inversion layer model can be used to estimate the island to gate capacitances for positive and negative gate voltages. TEM measurements show that the mean island size in the oxidized polysilicon is ~ 20 nm. Using a simple parallel plate capacitor model and assuming a cubical island, the island to side-gate capacitance for our device geometry is $C_{sg} = 0.2$ aF. Hence, at negative gate voltages we expect the island to gate capacitance to be ~ 0.2 aF, which is similar in magnitude to the values of C_{gl} in Table I.

At positive gate voltages, the capacitance between the island and the inversion layer becomes significant. Again, using a simple parallel plate capacitor model and a buried oxide layer thickness of ~ 10 nm, the island to inversion layer capacitance is $C_{i-inv} \sim 1.4$ aF. The total island to side-gate capacitance along the path formed by the side-gate, inversion layer and island is given by the series sum of the gate to inversion layer capacitance C_{g-inv} and C_{i-inv} . However, the much larger total area of the side gates implies that C_{g-inv}

is much greater than $C_{i\text{-inv}}$ and is therefore $\sim C_{i\text{-inv}}$. Hence, the total gate capacitance of the island at positive gate voltages is $C_{\text{sum}} = C_{\text{sg}} + C_{i\text{-inv}} = 1.6 \text{ aF}$, which is similar in magnitude to the values of C_{gh} in Table I. Finally, we note that for the 40-nm-thick buried oxide layer, $C_{i\text{-inv}} \sim 0.35 \text{ aF}$. In this case, the total gate capacitance of the island at positive gate voltages is $C_{\text{sum}} \sim 0.55 \text{ aF}$. Hence, we conclude that the effect of the inversion layer in the substrate is diminished for a thicker buried oxide layer, and if the inversion layer is created by fringing fields, then $C_{i\text{-inv}}$ may be even smaller.

VI. CONCLUSION

We have studied in detail the electrical characteristics of side-gated nanowire devices fabricated in standard CMOS polysilicon material. We have observed single-electron charging effects in oxidized and annealed/oxidized nanowires and the dependence of these effects on the physical geometry of the nanowire and thermal treatment of the material has been characterized. Nanowires fabricated on 10-nm-thick buried oxide substrates exhibit two distinct gate oscillation periods while nanowires fabricated on 40-nm-thick buried oxide substrates show only one distinct gate oscillation period. The two-period gate oscillation is found to be dependent on the length and width of the nanowire. For longer nanowires, MTJ effects are significant and in wider nanowires, the fringing fields of the side gates decrease the gate oscillation periods. We explain the two-period gate oscillations by considering the formation of a charge layer in the silicon substrate. These measurements demonstrate the significance of single-electron charging effects on electron transport in nanometer-scale CMOS systems.

We have also studied structural changes in thermally treated polysilicon films using ESR, Raman spectroscopy, and TEM analysis. We find that oxidation passivates the dangling bonds in the polysilicon film but annealing prior to oxidation decreases the effectiveness of the passivation. There exists anisotropic oxidation in the height and width of the polysilicon nanowires. We attribute this effect to dopant enhanced oxidation due to the existence of a dopant pile-up layer at the polysilicon layer/grown SiO_2 interface. The mean polysilicon grain size also decreases after oxidation. Annealing the polysilicon film increases the mean grain size and uniformity. In addition, it causes the grains to become more columnar. The electrical results in polysilicon nanowires are supported by these structural measurements.

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