A Mathematical Framework For Active Circuits Based On Port Equivalence Using Limit Variables

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Abstract— Infinity-variables (∞ -variables) have been used to allow symbolic description of any linear active element in an admittance matrix. This paper attempts a preliminary justification for such use of ∞ -variables. We develop the idea of port equivalence and show that ∞ -variables are a special case of limit-variables and can be used to imply limits in a set of matrix equations. We show that the presence of ∞ -variables in an admittance matrix implies the existence of matrix equivalences which lead to theorems that provide a means for analysis and synthesis of active circuits.

I. INTRODUCTION

Given a digital circuit, it is possible to analyse it using Boolean algebra in order to identify its logic function. Also, it is possible to synthesise a circuit from a logic specification. Until recently, no such framework existed for analogue circuits. The admittance matrix is potentially attractive as a framework because of the elegant way that it handles passive elements, but for ideal active elements, including the transistor and op-amp, there is a problem of infinite matrix elements [1], which has led to the modified nodal approach [2] or introduction of negative resistors [3], both of which increase the admittance matrix dimensions. In 2004, the problem was overcome without increasing the admittance matrix dimensions by introducing ∞ -variables (first referred to as linked infinity parameters) [4], a form of which had been used much earlier [5, 6, 7]. ∞ -variables have now been used to synthesise a wide variety of active circuits [8 - 13]. This paper develops some ideas underlying ∞ -variables in order to better justify their use.

II. MATRIX DESCRIPTION OF CIRCUITS

A. Matrix port-equivalence

Consider the example circuit in Fig 2.1. Replacing FETs M_1 and M_2 by transconductances G_{m1} and G_{m2} , we write the nodal admittance matrix (NAM) by inspection:

$$\begin{bmatrix} I_1 \\ I_2 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & G_{m2} & 0 & -G_{m2} \\ G_{m1} & 0 & -G_{m1} & 0 \\ -G_{m1} & 0 & G_1 + G_{m1} & 0 \\ 0 & -G_{m2} & 0 & G_2 + G_{m2} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \quad (1)$$

Partition lines separate variables at the port nodes, I_1 , I_2 , V_1 , V_2 , from variables at the non-port, or internal nodes, 3 and 4. Currents at internal nodes, I_3 and I_4 , are zero. We can obtain the 2-port description by reducing the matrix equations using Gaussian elimination:

$$\begin{bmatrix} I_1 \\ I_2 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & \frac{G_{m2}G_2}{G_{m2}+G_2} & 0 \\ G_{m1} & 0 & -G_{m1} \\ -G_{m1} & 0 & G_1+G_{m1} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & \frac{G_{m2}G_2}{G_{m2}+G_2} \\ \frac{G_{m1}G_1}{G_{m1}+G_1} & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (3)$$

The fact that the internal node currents I_3 and I_4 are zero means that the dependent currents are unaffected by these elimination operations which affect only the admittance matrix. Thus the voltage and current vectors in eqns (1) - (3) have a form that can always be inferred from the matrix partition lines and hence they do not need to be shown explicitly. Since reduction of both the 4×4 and 3×3 matrices leads to the same 2×2 port matrix, we can describe all three matrices as *port equivalent*. With this understanding we can write the following equivalence:

$$\begin{bmatrix} 0 & G_{m2} & 0 & -G_{m2} \\ G_{m1} & 0 & -G_{m1} & 0 \\ -G_{m1} & 0 & G_1+G_{m1} & 0 \\ 0 & -G_{m2} & 0 & G_2+G_{m2} \end{bmatrix} \equiv \begin{bmatrix} 0 & \frac{G_{m2}G_2}{G_{m2}+G_2} \\ G_{m1} & 0 \\ -G_{m1} & 0 \end{bmatrix} \equiv \begin{bmatrix} 0 & \frac{G_{m2}G_2}{G_{m2}+G_2} \\ \frac{G_{m1}G_1}{G_{m1}+G_1} & 0 \end{bmatrix} \quad (4)$$

Reversal of the reduction in eqn (4), i.e. matrix expansion, would constitute circuit synthesis, but there are effective barriers to synthesis, even for this simple example, in not knowing a priori the precise form of the initial port matrix (last matrix in eqn (4)) and the expansion operations themselves not being obvious. In order to simplify the expressions to enable synthesis to be possible, we consider analysis of the circuit with ideal transistors.

Fig 2.1 Transistor circuit for analysis

B. Limits of matrix equations

Consider the matrices in eqn (4) that describe the port behaviour of the circuit in Fig 2.1. Since the matrices are port-equivalent for any values of transistor gains G_{m1} and G_{m2} , port-equivalence must still apply when we let these gains tend to infinity. Setting $G_{m1}, G_{m2} \rightarrow \infty$ leads to:

$$\left[\begin{array}{cc|cc} 0 & G_{m2} & 0 & -G_{m2} \\ G_{m1} & 0 & -G_{m1} & 0 \\ \hline -G_{m1} & 0 & G_1 + G_{m1} & 0 \\ 0 & -G_{m2} & 0 & G_2 + G_{m2} \end{array} \right]_{G_{m1}, G_{m2} \rightarrow \infty} \quad (5)$$

$$\rightarrow \left[\begin{array}{cc|cc} 0 & G_2 & 0 & -G_{m1} \\ G_{m1} & 0 & -G_{m1} & 0 \\ \hline -G_{m1} & 0 & G_1 + G_{m1} & 0 \end{array} \right]_{G_{m1} \rightarrow \infty} \rightarrow \left[\begin{array}{cc} 0 & G_2 \\ G_1 & 0 \end{array} \right]$$

where we now use the ' $\rightarrow$ ' symbol instead of ' $\equiv$ '. Since the last matrix does not contain G_{m1} or G_{m2} and the centre matrix does not contain G_{m2} , conditions for these variables do not need to be stated. There is no problem in applying the limit to the last matrix in eqn (5), since it does not contain G_{m1} or G_{m2} , but there is a potential problem for the first matrix and centre matrix as some of their elements become infinite. However, the last matrix in eqn (5) implies that the relationships between the port variables I_1, I_2, V_1 and V_2 must be finite and since the first and second matrices must remain port-equivalent to the third matrix in the limit, the property of finite relationships between port variables must apply to all three matrices. Thus, when the elements of the matrix tend to infinity, the effect of this is to imply finite relationships between the port variables. Although we show only the matrices, we treat the limit as applied over the whole set of associated equations including the dependent and independent variables. Eqn (5)-right hand (RH) shows that, for ideal transistors, the 2-port circuit in Fig 2.1 is a negative impedance inverter.

C. Limit-variables

The limit matrices in eqn (5) for the case of ideal transistors were obtained as limits of corresponding matrices in eqn (4). However, it is convenient to work entirely with the limit matrices in eqn (5) without reference to eqn (4). In order to facilitate this, we introduce a special type of variable that implies a limit and which we call a *limit-variable*. For the case where elements of a matrix contain variable x and the matrix is a limit matrix with $x \rightarrow k$, we replace each instance of x by the limit-variable symbol k_x . This allows eqn (5) to be written as follows:

$$\left[\begin{array}{cc|cc} 0 & \infty'_{m2} & 0 & -\infty'_{m2} \\ \infty'_{m1} & 0 & -\infty'_{m1} & 0 \\ \hline -\infty'_{m1} & 0 & G_1 + \infty'_{m1} & 0 \\ 0 & -\infty'_{m2} & 0 & G_2 + \infty'_{m2} \end{array} \right] \rightarrow \left[\begin{array}{cc|cc} 0 & G_2 & 0 & -\infty'_{m1} \\ \infty'_{m1} & 0 & -\infty'_{m1} & 0 \\ \hline -\infty'_{m1} & 0 & G_1 + \infty'_{m1} & 0 \end{array} \right] \rightarrow \left[\begin{array}{cc} 0 & G_2 \\ G_1 & 0 \end{array} \right] \quad (6)$$

where the parameters ∞'_{mi} are infinity-variables, or ∞ -variables, and the apostrophe will be discussed later. Each matrix in eqn (6) may be derived from its predecessor by Gaussian elimination and taking limits where necessary,

e.g. in the second matrix, the y_{12} element may be derived as follows:

$$y_{12} = \infty'_{m2} - \frac{(-\infty'_{m2})^2}{G_2 + \infty'_{m2}} = \frac{\infty'_{m2} G_2}{G_2 + \infty'_{m2}} \rightarrow G_2 \quad (7)$$

where we have taken the limit. However, there is a much simpler and more direct relationship between the elements of the matrices in eqn (6). Between the first and second matrix, the element G_2 has moved from row 4 to row 1 and then from column 4 to column 2; the rows and columns it has moved between are the rows and columns occupied by the ∞ -variables $\pm\infty'_{m2}$. A similar statement applies to the movement of the element G_1 between the second and third matrix. This suggests that there might exist a theorem governing the movement of elements in the matrix. Before we consider this in the next section, we consider a generalisation of the ∞ -variable concept.

If the ∞ -variables ∞'_{mi} in the first matrix in eqn (6) are replaced by finite variables G_{mi} we obtain the LH matrix in eqn (4). Hence matrices with ∞ -variables can represent the non-ideal case (with finite values) as well as the ideal case where they imply limits on the matrix equations. Thus, the limit indicated by a limit-variable is best treated as a potential limit that may or may not be actualised. It is convenient to indicate actualisation of the limit by an apostrophe, e.g. ∞'_{mi} instead of ∞_{mi} , as in eqns (6) and (7).

Fig 3.1 Some simple 2-port circuits

III. THEOREM FOR MATRICES WITH ∞ -VARIABLES

Consider the 2-port example circuits containing an ideal short-circuit and a conductance G in Figs 3.1a and c. We can replace the ideal short-circuits by finite conductances as in Figs 3.1b and d, which allows us to write admittance matrices:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} g+G & -g \\ -g & g \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} g & -g \\ -g & g+G \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (8)$$

The two circuits in Figs 3.1a and c are indistinguishable at their ports and the ideal short-circuit is described by taking a limit with $g \rightarrow \infty$ in eqns (8) which can be implied using ∞ -variables. This leads to a matrix equivalence:

$$\begin{bmatrix} \infty'_1 + G & -\infty'_1 \\ -\infty'_1 & \infty'_1 \end{bmatrix} \equiv \begin{bmatrix} \infty'_1 & -\infty'_1 \\ -\infty'_1 & \infty'_1 + G \end{bmatrix} \quad (9)$$

Parameter G has effectively moved between the rows and columns occupied by the $\pm\infty'_1$ elements. Eqn (9) may be regarded as a theorem for matrices containing ∞ -variables. We can see that this theorem is sufficient to obtain the final matrix in eqn (6) from the first, where G_2 is moved from the 4,4 to the 1,2 position making use of parameters ∞'_{m2} and G_1 is moved from the 3,3 to the 2,1 position making use of parameters ∞'_{m1} .

Three theorems, one of which is a generalisation of eqn (9), will be discussed in section IV and are the *raison d'être* for the ∞ -variable approach. These theorems provide a straightforward yet powerful basis for the analysis and synthesis of circuits with ideal active elements.

In order to explore the nature of the equivalent matrices in eqn (9), we can write eqns (8) as follows:

$$\begin{aligned} I_1 &= (g+G)V_1 - gV_2 & I_1 &= g(V_1 - V_2) \\ I_2 &= -g(V_1 - V_2) & I_2 &= -gV_1 + (g+G)V_2 \end{aligned} \quad (10)$$

We can add the two equations:

$$I_1 + I_2 = GV_1 \quad I_1 + I_2 = GV_2 \quad (11)$$

Then the limit $g \rightarrow \infty$ may be imposed in eqn (10) by expressing voltage variable V_1 in terms of other variables:

$$\begin{aligned} V_1 &= \frac{1}{g+G}I_1 + \frac{g}{g+G}V_2 \xrightarrow{g \rightarrow \infty} V_2 & V_1 &= \frac{1}{g}I_1 + V_2 \xrightarrow{g \rightarrow \infty} V_2 \\ V_1 &= -\frac{1}{g}I_2 + V_2 \xrightarrow{g \rightarrow \infty} V_2 & V_1 &= -\frac{1}{g}I_2 + \frac{g+G}{g}V_2 \xrightarrow{g \rightarrow \infty} V_2 \end{aligned} \quad (12)$$

In the limit, each row of both matrices in eqn (9) imposes the same constraint $V_1 = V_2$. When this constraint is substituted into either expression in eqn (11), it yields the alternative one. Thus the existence of equivalent matrices is due to the constraint $V_1 = V_2$ involving only the independent variables (i.e. the voltages). We now generalise.

We consider a non-degenerate circuit with N ports all of which are accessible. Such a circuit may be described using Belevitch's formalism [14]:

$$[\mathbf{A} \mid \mathbf{B}] \begin{bmatrix} \underline{V} \\ \underline{I} \end{bmatrix} = 0 \quad (13)$$

where $\underline{V}$ and $\underline{I}$ are column vectors of the port voltages and currents, respectively, and $\mathbf{A}$ and $\mathbf{B}$ are $N \times N$ matrices with finite elements. Although $\mathbf{A}$ and $\mathbf{B}$ are not unique for a given circuit, eqn (13) represents an N -dimensional subspace within the $2N$ -dimensional vector space spanned by the port variables $\underline{V}$ and $\underline{I}$ which is unique.

It is usual to work with compact circuit descriptions of the form:

$$\underline{P} = \mathbf{M}\underline{Q} \quad (14)$$

where $\mathbf{M}$ is an $N \times N$ matrix which may be finite or include ∞ -variables and may be singular or non-singular, and $\underline{P}$ and $\underline{Q}$ are a sub-set and complementary sub-set, respectively, of the port voltages and currents. $\underline{P}$ and $\underline{Q}$ comprise the dependent and independent variables, respectively, and define a basis for description of the given circuit, e.g. the admittance basis, $\underline{I} = \mathbf{Y}\underline{V}$. Note that the N linear equations defined by this matrix equation are independent irrespective of whether $\mathbf{M}$ is singular or non-singular. We now consider two distinct cases:

- 1 If the circuit and the basis chosen lead to matrix $\mathbf{M}$ in eqn (14) with finite elements, then $\mathbf{M}$ is unique.
- 2 If the circuit and the basis lead to matrix $\mathbf{M}$ in eqn (14) containing ∞ -variables, then consider division of rows in eqn (14) containing an ∞ -variable by that ∞ -variable. In such rows, the dependent variable on the LHS will vanish and we will be left with a set of relationships involving only independent variables. Use of such rows to perform row operations will lead to alternative equation sets which are still consistent with the original basis and hence generate matrix equivalences.

Thus for a circuit and representation basis where the circuit port matrix contains ∞ -variables, then equivalent matrices describing the same port behaviour must exist.

IV. GENERAL THEOREMS

Theorems for matrices containing ∞ -variables should be as general as possible in order to maximise their scope. Since each of the circuits in Figs 3.1a and c consist of a conductance G and an ideal short-circuit, the admittance matrix description for the ideal short-circuit is obtained by removing the conductance G in eqn (9):

$$\begin{matrix} i & j \\ i \left[\begin{array}{cc} \infty_1 & -\infty_1 \\ -\infty_1 & \infty_1 \end{array} \right] & m \left[\begin{array}{cc} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{array} \right] \\ j \left[\begin{array}{cc} \infty_1 & -\infty_1 \\ -\infty_1 & \infty_1 \end{array} \right] & n \left[\begin{array}{cc} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{array} \right] \end{matrix} \quad (15)$$

where the short-circuit is connected between nodes i and j . If symmetry is relaxed, as in eqn (15)-RH, the matrix then describes the nullor, or ideal transistor or op-amp [4]. The elements in the two rows impose the same constraint ($V_i = V_j$), as do those in the two columns ($I_m = -I_n$). We can generalise the description by introducing row and column scaling factors α and β while preserving the consistency of the new constraints [4]:

$$\begin{matrix} i & j \\ m \left[\begin{array}{cc} \infty_i & -\beta\infty_i \\ -\alpha\infty_i & \alpha\beta\infty_i \end{array} \right] & \\ n \left[\begin{array}{cc} \infty_i & -\beta\infty_i \\ -\alpha\infty_i & \alpha\beta\infty_i \end{array} \right] & \end{matrix} \quad (16)$$

Three theorems for equivalent matrices based on eqn (16) have been found [4, 13]. The first is called the arbitrary element theorem [4]; a corollary is called the element shift theorem and it may be used to obtain the theorem in eqn (9). The second theorem [13] applies to two sets of elements of the type in eqn (16) and allows specific movements of the elements. The third theorem [13] applies also to two sets of ∞ -variable elements and allows a third set to be introduced. These theorems provide capability for circuit analysis and synthesis with ideal elements, as in [8 - 13].

V. ELEMENT REPRESENTATIONS

For two circuits that do not possess admittance matrices (in the usual sense), namely the ideal short-circuit and the nullor, we have shown that admittance matrices using ∞ -variables may be derived, as in eqn (15). Other elements that do not (in the usual sense) possess admittance matrices are three controlled sources, voltage-controlled voltage, current-controlled voltage and current-controlled current, and the impedance converter. Admittance matrix representations for these elements using ∞ -variables are derived in [4]. Equivalent forms obtained using the theorems delineate the ways in which the ideal elements may be realised in the non-ideal case [15].

VI. CIRCUIT SYNTHESIS

Circuit synthesis may be considered as analysis in reverse; the analysis in eqn (6) may be reversed as follows:

$$\begin{bmatrix} 0 & G_2 \\ G_1 & 0 \end{bmatrix} \rightarrow \left[\begin{array}{cc|cc} 0 & G_2 & 0 & 0 \\ \infty'_{m1} & 0 & -\infty'_{m1} & 0 \\ \hline -\infty'_{m1} & 0 & G_1 + \infty'_{m1} & 0 \end{array} \right] \rightarrow \left[\begin{array}{cc|cc} 0 & \infty'_{m2} & 0 & -\infty'_{m2} \\ \infty'_{m1} & 0 & -\infty'_{m1} & 0 \\ \hline -\infty'_{m1} & 0 & G_1 + \infty'_{m1} & 0 \\ 0 & -\infty'_{m2} & 0 & G_2 + \infty'_{m2} \end{array} \right] \quad (17)$$

The first matrix is a 2-port admittance matrix for the negative impedance inverter. To go to the centre matrix, we have added a blank row 3 and column 3, which is permissible as it corresponds to adding an isolated node:

$$\begin{bmatrix} 0 & G_2 \\ G_1 & 0 \end{bmatrix} \rightarrow \begin{bmatrix} 0 & G_2 & 0 \\ G_1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \rightarrow \begin{bmatrix} 0 & G_2 & 0 \\ G_1 + \infty_{m1} & 0 & -\infty_{m1} \\ -\infty_{m1} & 0 & \infty_{m1} \end{bmatrix} \quad (18)$$

It may be shown [8] that since the voltage at the isolated node is unobservable and its current is zero, we can introduce a set of ∞ -variables which link row 3 and column 3 to any other row and column; we have chosen row 2 and column 1 in the RH matrix in eqn (18), in which the theorem in eqn (9) allows us to move G_1 to the 3,3 position as in eqn (17)-centre. A similar operation to that in eqn (18) allows us to obtain eqn (17)-RH, which is a circuit NAM yielding the circuit in Fig 2.1.

Once a circuit has been synthesised, its NAM may be used as the basis for practical design; finite gain parameters for active elements may be introduced, as well as parasitic elements, and the matrix used to optimise the circuit parameters to meet the specifications [15].

Active circuit synthesis is a large topic and many examples exist, including active-RC building blocks [8], active-RC sections [9] and FET circuits [10-13]. Apart from ∞ -variables, the next most useful type of limit variable is the zero-variable (0-variable).

Fig 7.1 Example circuit a Original version b Modified version

VII. ZERO-VARIABLES

Consider the circuit consisting of an ideal short-circuit in Fig 7.1a, which has the following admittance matrix:

$$\mathbf{Y} = \begin{bmatrix} \infty_1 & -\infty_1 \\ -\infty_1 & \infty_1 \end{bmatrix} \quad (19)$$

Note that this matrix is both singular and contains ∞ -variables. Suppose that we wish to change to the impedance basis requiring inversion of the matrix:

$$\mathbf{Z} = \begin{bmatrix} \infty_1 & -\infty_1 \\ -\infty_1 & \infty_1 \end{bmatrix}^{-1} = \frac{1}{\infty_1^2 - \infty_1^2} \begin{bmatrix} \infty_1 & \infty_1 \\ \infty_1 & \infty_1 \end{bmatrix} = \frac{1}{0} \begin{bmatrix} \infty_1 & \infty_1 \\ \infty_1 & \infty_1 \end{bmatrix} \quad (20)$$

The reason for the singularity is that, in the circuit in Fig 7.1a, there is a topological incompatibility (current-source cut-set) between the circuit having no element connected to ground and the impedance basis where the parameters are defined with open-circuits and current sources at the ports. This problem can be overcome by introducing a conductance, as in Fig 7.1b, which approaches a limit of zero and whose admittance we denote by 0-variable, 0_2 . For this circuit the $\mathbf{Y}$ matrix may be inverted easily:

$$\begin{aligned} \mathbf{Z} &= \begin{bmatrix} \infty_1 & -\infty_1 \\ -\infty_1 & \infty_1 + 0_2 \end{bmatrix}^{-1} = \frac{1}{\infty_1 0_2} \begin{bmatrix} \infty_1 + 0_2 & \infty_1 \\ \infty_1 & \infty_1 \end{bmatrix} \\ &= \begin{bmatrix} 0_2^{-1} + 1/\infty_1 & 0_2^{-1} \\ 0_2^{-1} & 0_2^{-1} \end{bmatrix} \rightarrow \begin{bmatrix} 0_2^{-1} & 0_2^{-1} \\ 0_2^{-1} & 0_2^{-1} \end{bmatrix} = \begin{bmatrix} \infty_2 & \infty_2 \\ \infty_2 & \infty_2 \end{bmatrix} \end{aligned} \quad (21)$$

where we have replaced the limit conductance 0_2 by a limit resistance ∞_2 . This example illustrates how 0-variables may be used to overcome matrix singularity caused by topological incompatibility between a circuit and a chosen basis. This could be performed using perturbation and limits in the usual way, but the use of ∞ - and 0-variables provides a solution with circuit relevance and context.

A very important use of 0-variables is to handle zero pivots in matrices; examples are given in [4, 10 - 13]. The property that limit-variables may be used in algebra like regular variables is shared with hyper-real numbers [16].

VIII. CONCLUSIONS

We have attempted a justification for the use of ∞ -variables for analysis and synthesis of circuits containing ideal active elements. We considered the concept of matrix port equivalence and showed that ∞ -variables can be used to imply limits in the corresponding equation set. We showed that when a circuit is described using a basis that requires elements containing ∞ -variables, then equivalent matrices describing the same circuit exist, leading to theorems that permit circuit analysis and synthesis. Finally, zero-variables have a valuable role in dealing with topological matrix singularity and zero pivots.

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